

【DESCRIPTION】

【Invention Title】

**ETCHING COMPOSITION AND METHOD FOR MANUFACTURING
SEMICONDUCTOR DEVICE USING SAME**

5 **【Technical Field】**

[1] CROSS-REFERENCE TO RELATED APPLICATION

[2] This application claims the benefit of priority to Korean Patent Application No. 10-2023-0135825, filed in the Korean Intellectual Property Office on October 12, 2023, and Korean Patent Application No. 10-2024-0096375, filed in the Korean Intellectual Property
10 Office on July 22, 2024, the entire contents of which are incorporated herein by reference.

[3] Technical Field

[4] The present disclosure relates to an etching composition and a method for manufacturing a semiconductor device using the same, and more particularly to an etching composition to etch a nitride layer at a higher selectivity, and a method for manufacturing a
15 semiconductor device using the same.

【Background Art】

[5] Recently, as an information communication device is realized with multiple functions, a semiconductor device including a memory device has required to have a larger capacity and a higher integration degree. As a cell size of a memory is reduced for the higher
20 integration, the memory device has been complicated in the structure of operating circuits and wirings included in the memory device for the operation and the electrical connection of the memory device. A nitride layer and an oxide layer, which are representative insulating layers in the manufacturing process of a highly downscaled semiconductor device, may be individually used or alternately stacked on each other. To configure a complex or fine
25 structure, for example, a three-dimension structure of an electronic device, the nitride layer

needs to be selectively etched and to have various-shaped patterns. In particular, an etching composition is required to sufficiently ensure an etch selectivity of the nitride layer over the oxide layer, while preventing unnecessary particles from being produced or preventing undesired by-products from being abnormally grown from the surface of the oxide layer, during an etching process for the nitride layer.

[6] In a semiconductor device (integrated circuit), an oxide layer, such as a silicon oxide layer (SiO_2) and a nitride layer, such as a silicon nitride layer (SiN_x) are representative insulating layers. At least one of the oxide layer or the nitride layer is individually or alternately stacked to form a stack structure. Such an oxide layer or nitride layer is used as a hard mask to form a conductive pattern such as a metal interconnection.

[7] According to a wet process for removing the nitride layer, in general, the mixture of phosphoric acid and deionized water has been used as an etching composition. In this case, the deionized water is added to prevent the etch rate of the nitride layer from being reduced or to prevent the etch selectivity of the nitride layer over the oxide layer from being changed. When the nitride layer is removed through a wet etching process, the failure may be made due to the fine change in an amount of the deionized water when the nitride layer is removed through a wet etching process. In addition, as the etch selectivity of the nitride layer over the oxide layer is reduced, the nitride layer may not be etched to be a desirable degree.

[8] Accordingly, there have been developed technologies for adding an additive to an etching composition to improve the effect of the etching composition only including phosphoric acid and deionized water, particularly, the etch selectivity of the nitride layer over the oxide layer based on the etching composition. However, even through the improved technologies, the additive has been used in a lower content of less than 3 wt%, based on the total weight of the etchant. In addition, when the additive is used in the content of at least about 3 wt% which is excessive, the additive material serves as impurities, so the etch rate of

the nitride layer is not sufficiently ensured, or the selectivity of the nitride layer over the oxide layer is not sufficiently satisfied. Accordingly, as a significant small amount of additive is used, the above improvement resulting from the use of the additive may not be sufficiently exhibited.

5 **[9]** In addition, an etching process may be performed at a higher temperature of more than 150°C. In this case, when a temperature for etching is out of a specific range due to the additive for the etch selectivity, the etch performance may not be sufficiently ensured or an abnormal growth may be made.

10 **[10]** Accordingly, a technical problem to be solved is to find out a composition of an etching composition which is available without any problem under a higher-temperature wet etching process, sufficiently exhibits an excellent improvement effect resulting from the use of an additive`, and has the higher basic selectivity of the nitride layer over the oxide layer.

【Disclosure】

15 **【Technical Problem】**

[11] An aspect of the present disclosure provides an etching composition capable of preventing an abnormal growth even in a higher-temperature wet etching process, of improving the etch selectivity of the nitride layer over the oxide layer, and of preventing bubbles immediately after the etching composition is prepared such that efficiency of the etching process is prevented from being degraded or etching facilities is prevented from being damaged, such that an APHA value is less than 1.5 which hardly exhibits a color, thereby providing easy handling when applying the etching composition to an etching process.

25 **[12]** In addition, another aspect of the present disclosure provides a method for manufacturing a semiconductor device, capable of improving an etch selectivity of a nitride

layer over an oxide layer, without causing a problem such as production of bubbles of an etching composition, during an etching process of the nitride layer having various shapes to realize an electronic device having a complex and fine structure, such that the stability and the reliability of the etching process for the nitride layer is ensured, and of improving the productivity of the manufacturing process of a semiconductor device.

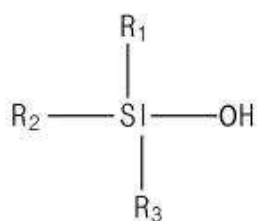
【Technical Solution】

[13] An aspect of the present disclosure provides an etching composition and a method for manufacturing a semiconductor device using the same.

[14] More specifically, (1) the present disclosure provides an etching composition including an inorganic acid, a silanol-based compound; and a solvent as a remainder, in which a content of the silanol-based compound ranges from 0.1 parts by weight to less than 10 parts by weight, based on a total weight of the etching composition, and an APHA value is less than 1.5.

[15] (2) The present disclosure provides an etching composition in which the silanol-based compound is a silanol-based compound represented by following Chemical Formula 1 or a condensate of the silanol-based compound, in (1),

[16] [Chemical Formula 1]



[17] in Chemical Formula 1,

[18] R₁ is selected from the group consisting of an aminoalkyl group having 1 to 20 carbon atoms, an alkoxy group having 1 to 20 carbon atoms, an acetyloxy group, and a haloalkyl acetyloxy group having 1 to 20 carbon atoms, and R₂ and R₃ are hydroxy groups.

- [19] (3) The present disclosure provides an etching composition in which the silanol-based compound is 3-aminopropylsilanetriol or a condensate of the silanol-based compound, in (1) or (2)
- [20] (4) The present disclosure provides an etching composition in which the
5 silanol-based compound has a CAS value of at most 68400-07-7 any one of (1) to (3).
- [21] (5) The present disclosure provides an etching composition in which the inorganic acid ranges from 50 parts by weight to 85 parts by weight, based on 100 parts by weight of a whole etching composition, in any one of (1) to (4).
- [22] (6) The present disclosure provides an etching composition in which the inorganic
10 acid includes at least one selected from the group consisting of sulfuric acid, nitric acid, phosphoric acid, silicic acid, hydrofluoric acid, boric acid, hydrochloric acid, and perchloric acid, in any one of (1) to (5).
- [23] (7) The present disclosure provides an etching composition in which the etching composition further includes an ammonium-based compound, in any one of (1) to (6).
- [24] (8) The present disclosure provides an etching composition in which the
15 ammonium-based compound includes at least one selected from the group consisting of ammonium chloride, ammonium phosphate, ammonium acetate, ammonium sulfate, ammonium formate, and metal amine complex salt, in any one of (1) to (7).
- [25] (9) The present disclosure provides an etching composition in which the etching
20 composition is used to etch the silicon nitride layer, in any one of (1) to (8).
- [26] (10) The present disclosure provides an etching composition in which an etch selectivity of a silicon nitride layer over a silicon oxide layer of the etching composition is at least 30, in any one of (1) to (9).
- [27] (11) The present disclosure provides an etching composition in which an absolute
25 value of variation of an etch rate of the nitride layer is at most 20% while the etching process

is performed until a silicon ion is in a range from 100 ppm to 1,500 ppm, in any one of (1) to (10).

[28] (12) The present disclosure provides an etching composition in which a height of bubbles on a surface of the etching composition is at most 0.5 cm, immediately after the etching composition is formed, in any one of (1) to (11).

[29] (13) The present disclosure provides an etching composition in which an etch rate of the nitride layer ranges from 40 to 80 Å/min at an etching process temperature of 165°C, in any one of (1) to (12).

[30] (14) The present disclosure provides an etching composition in which an etch rate of the silicon oxide layer is 1 Å/min at an etching process temperature of 165°C., in any one of (1) to (13).

[31] (15) The present disclosure provides a method for manufacturing a semiconductor device, which includes forming a structure by stacking an insulating layer and a sacrificial layer on a substrate, and forming a space region by performing an etching process using the etching composition according to any one of (1) to (14) to remove the sacrificial layer.

[32] (16) The present disclosure provides a method for manufacturing a semiconductor device, in which the sacrificial layer includes a silicon nitride, and the insulating layer includes a silicon oxide layer, in (15).

[33] (17) The present disclosure provides a method for manufacturing a semiconductor device, in which the sacrificial layer has an etch rate higher than an etch rate of the insulating layer, in the etching process, in (15) or (16).

[34] (18) The present disclosure provides a method for manufacturing a semiconductor device, in which the space region includes: a gate region interposed between insulating layers and a trench connected to the gate region, in any one of (15) to (17).

[35] (19) The present disclosure provides a method for manufacturing a semiconductor

device, which includes forming openings formed through the stack structure, and forming a semiconductor pattern spaced apart from the trench in the openings, in which the forming of the semiconductor pattern is performed before forming the trench, in any one of (15) to (18).

【Advantageous Effects】

5 **[36]** According to the present disclosure, the etch composition may increase the etch selectivity of the nitride layer to adjust the etch rate of the oxide layer. Accordingly, the height (EFH) of the effective oxide layer may be easily adjusted.

[37] In addition, according to the present disclosure, the etching composition may improve the reliability of the semiconductor device by preventing the oxide layer quality
10 from being degraded when the nitride layer is removed, preventing the electrical characteristic from being degraded due to the etching of the oxide layer, and preventing particles from being produced.

[38] In addition, according to the present disclosure, the etching composition may have an APHA value of less than 1.5 which hardly exhibits a color. Accordingly, the etching
15 composition may be easily handled when the etching process is applied.

[39] In addition, according to the present disclosure, the etching composition may selectively etch only the nitride layer, based on the higher etch selectivity of the oxide layer over the nitride layer, even if the nitride layer and the oxide layer are alternately stacked or mixed, when the nitride layer is etched. Accordingly, according to the present disclosure, the
20 etching composition may more improve the etch selectivity of the nitride layer over the oxide layer without causing the above problem while etching the nitride layer having variously-shaped pattern to configure the electronic device having the complex and fine structure. Accordingly, the etching composition may ensure the stability and the reliability during the etching process of the nitride layer and prevent the oxide layer, which is exposed
25 to the etching composition together with the nitride layer, from being degraded or prevent the

electrical characteristic of the oxide layer from being degraded, thereby improving the productivity in the manufacturing process of the semiconductor device and improving the reliability of the semiconductor device.

[40] Therefore, according to the present disclosure, the etching composition may be usefully employed for the manufacturing process (e.g., a device isolation process of the flash memory device, a pipe channel forming process of a 3D flash memory device, and a diode forming process of a phase-change memory) of the semiconductor device, which requires the selective removal of the nitride layer, thereby contributing to improve the efficiency of the manufacturing process of the semiconductor device.

[41] In addition, according to the present disclosure, the etching composition may contain a specific amount of additives for improving the etch selectivity of the nitride layer and for enduring the high-temperature process, thereby providing the etching composition having the higher process utilization. In particular, the abnormal growth and the production of particles during the etching process may be prevented due to a specific amount of additive included into the etching composition. In addition, according to the present disclosure, the etching composition has no bubbles immediately after prepared. Accordingly, the etching composition may be applied to the etching process without degrading the efficiency of the etching process or causing the damage to the etching equipment.

[42] The effects of the present disclosure are not limited to the above effects. The effects should be interpreted as including all inferable effects from the configuration of the present disclosure set forth in claims.

【Description of Drawings】

[43] FIG. 1 illustrates a plan view of a semiconductor device according to examples of the present disclosure;

[44] FIGS. 2 to 8 are views for describing a method for manufacturing a semiconductor

device according to examples of the present disclosure; and

[45] FIG. 9 is an enlarged view illustrating region A of FIG. 8.

【Mode for Invention】

[46] Hereinafter, the present disclosure will be described in detail. However, the present
5 disclosure may be realized in various forms. The present disclosure is not limited by
examples described herein. The present disclosure is defined by claims to be described
below.

[47] In addition, the terms used herein to describe examples of the present disclosure is
not intended to limit the scope of the present disclosure. The singular forms are intended to
10 include the plural forms unless the context clearly indicates otherwise. When a certain part
“includes” a certain component throughout the whole specification, the certain part does not
exclude other components, but may further include other components if there is a specific
opposite description.

[48] In the present disclosure, “silicon nitride layer,” “silicon nitride,” and “ Si_xN_y ” refer
15 not only to pure silicon nitride but also to impure silicon nitride which includes hydrogen,
carbon, and/or oxygen impurities in a crystal structure (here, each of x and y is independently
a positive integer).

[49] In the present disclosure, a “silicon oxide layer” and a “silicon oxide” refer to a thin
film including a silicon oxide (SiO_x), for example, SiO_2 , or a “thermal oxide” (ThO_x). The
20 silicon oxide may be disposed on a substrate through any manner such as deposition through
chemical vapor deposition from TEOS or another source, or thermal deposition. The silicon
oxide may generally include other materials or impurities at a low level that is commercially
useful. The silicon oxide may be present as a part of a microelectronic device, for example, as
an insulating layer which is a feature of the microelectronic device.

25 [50] In the present disclosure, “removing at least a portion of a silicon nitride material”

corresponds to “removing at least a portion, which is exposed, of the silicon nitride layer. For example, “removing the at least the portion of the silicon nitride material includes anisotropically removing a silicon nitride layer which covers and protects a gate electrode to form Si_3N_4 . A composition according to the present disclosure may be more generally used for substantially removing the silicon nitride over polysilicon and/or a silicon oxide layer. In this condition, the wording “substantially removing” may refer to that at least 90%, at least 95%, or at least 99% of a silicon nitride material is removed using the composition according to the present disclosure. In this case, “%” may correspond to at least one of all factors, such as a volume, a weight, or a mole which may serve as a basis for a percentage.

10 **[51]** In the present disclosure, the expression “substituted or unsubstituted” may refer to that at least one hydrogen atom and/or a lone pair of electrons are substituted or unsubstituted with at least one substituent selected from the group consisting of a deuterium atom, a halogen atom, a boron atom, a cyano group, a nitro group, an amino group, a silyl group, a phosphine oxide group, a phosphine sulfide group, a carboxy group, an alkyl group, an alkenyl group, an alkoxy group, an aryl group, and a heterocyclic group. Specifically, the expression “substituted or unsubstituted” may refer to that at least one hydrogen atom and/or a lone pair of electrons are substituted or unsubstituted with at least one substituent selected from the group consisting of a deuterium atom, an alkyl group, an amino group, a silyl group, and an alkoxy group. In addition, the substituent in the above example may be substituted or
15 unsubstituted. For example, the methylamino group and the aminoalkylamino group may be interpreted as an amino group.

[52] In the present disclosure, a halogen atom may be, for example, a fluorine atom, a chlorine atom, a bromine atom, or an iodine atom.

[53] In the present disclosure, an alkyl group may be a linear-type alkyl group, a
25 branch-type alkyl group, or a cyclic-type alkyl group. For example, the alkyl group may

include a methyl group, an ethyl group, an n-propyl group, an isopropyl group, an n-butyl group, a t-butyl group, an i-butyl group, a 2-ethylbutyl group, a 3,3-dimethylbutyl group, an n-pentyl group, an i-pentyl group, a neopentyl group, a t-pentyl group, a cyclopentyl group, a 1-methylpentyl group, a 3-methylpentyl group, a 2-ethylpentyl group, or a 4-methyl-2-pentyl group, an n-hexyl group, a 1-methylhexyl group, a 2-ethylhexyl group, a 2-butylhexyl group, a cyclohexyl group, a 4-methylcyclohexyl group, a 4-t-butylcyclohexyl group, an n-heptyl group, a 1-methylheptyl group, a 2,2-dimethylheptyl group, a 2-ethylheptyl group, a 2-butylheptyl group, an n-octyl group, a t-octyl group, a 2-ethyloctyl group, a 2-butyloctyl group, a 2-hexyloctyl group, a 3,7-dimethyloctyl group, a cyclooctyl group, an n-nonyl group, or an n-decyl group, but the present disclosure is not limited thereto.

[54] In the present disclosure, an amino group may include an alkylamino group and an arylamino group. For example, the amino group may include a methylamino group, an ethylamino group, a dimethylamino group, a diethylamino group, and/or an ethylmethylamino group, but the present disclosure is not limited thereto.

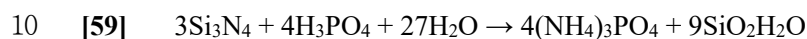
[55] In the present disclosure, an alkoxy group may include an alkyl alkoxy group and an aryl alkoxy group. For example, the alkoxy group may include a methoxy group, an ethoxy group, a propoxy group, a butoxy group, a pentyloxy group, a hexyloxy group, a heptyloxy group, an octyloxy group, a nonyloxy group, or a decyloxy group, but the present disclosure is not limited thereto.

[56] **Etching composition**

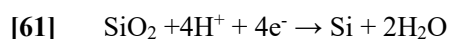
[57] An etching composition may be used to etch a silicon-containing material. In detail, the etching composition may be used to etch a silicon nitride layer or a silicon oxide layer serving as an insulating layer. For example, etching of the silicon nitride layer by using the etching composition including a phosphoric acid as an inorganic acid may be performed as in following Reaction Equation 1. The etching of the silicon oxide layer by using the same

etching composition may be performed as in following Reaction Equation 2. However, an etch rate of the silicon nitride layer serving as a first insulating layer may be higher than an etch rate of the silicon oxide layer serving as a second insulating layer, in an etching process using the etching composition. In the present disclosure, the etching of the silicon nitride layer may refer to the removing of a silicon nitride, and the etching of the silicon oxide layer may refer to the moving of a silicon oxide. The silicon nitride may be expressed as Si_xN_y . The silicon oxide may be expressed as Si_xO_y , (herein, each of 'x' and 'y' is independently a positive integer).

[58] [Reaction Equation 1]



[60] [Reaction Equation 2]



[62] Referring to Reaction Equation 1, a phosphoric acid may react with a silicon nitride to remove the silicon nitride. The phosphoric acid serving as the inorganic acid may be contained in an amount ranging from 50 parts by weight to 85 parts by weight, based on 100 parts by weight of the total etching composition. When a smaller amount of inorganic acid is contained, the silicon nitride layer may not be easily removed. When the inorganic acid is contained in an amount greater than necessary, the inorganic acid may adversely affect the etching equipment. In addition, when the amount of the inorganic acid used is not appropriate, etching by-products may be formed during the etching process.

[63] Referring to Reaction Equation 2, the phosphoric acid may provide hydrogen ions such that the hydrogen ions react with silicon oxide. When the phosphoric acid is contained in an excessive amount in the etching composition, a reaction rate between the hydrogen ions and the silicon oxide may increase, as the content of hydrogen ions is increasingly provided from the phosphoric acid. In this case, during the etching process, the selectivity of the silicon

nitride layer over the silicon oxide layer may not be sufficiently increased.

[64] Hereinafter, the etching composition provided according to the present disclosure will be described in detail.

[65] The present disclosure provides an etching composition including an inorganic acid,
5 a silanol-based compound, and a solvent as a remainder, in which the content of the silanol-based compound, based on the total weight of the whole etching composition, ranges from 0.1 parts by weight to less than 10 parts by weight, and the APHA value is less than 1.5.

[66] According to an embodiment of the present disclosure, the inorganic acid included in the etching composition allows the etching composition to have a pH (e.g., the pH ranging
10 from 2 to 6) representing acidity to etch an etching target (e.g., an insulating layer).

[67] The inorganic acid may be at least one selected from the group consisting of sulfuric acid, nitric acid, phosphoric acid, silicic acid, hydrofluoric acid, boric acid, hydrochloric acid, and perchloric acid. Specifically, the inorganic acid may be phosphoric acid. When the phosphoric acid is used as the inorganic acid, and when the etching target is an oxide layer
15 and a nitride layer, the etch selectivity of the nitride layer over the oxide layer may be increased. In addition, when the phosphoric acid is used as the inorganic acid, a sufficient amount of hydrogen ions may be provided into the etching composition to accelerate the etching.

[68] In addition, when the inorganic acid is phosphoric acid, the etching composition may
20 further include sulfuric acid as an additive. The sulfuric acid may increase a boiling point of the etching composition including the phosphoric acid as the inorganic acid to help etch the nitride layer.

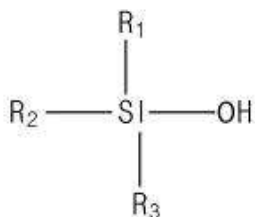
[69] According to an embodiment of the present disclosure, the inorganic acid may be contained in an amount ranging from 50 parts by weight to 85 parts by weight, based on 100
25 parts by weight of the total etching composition. Specifically, the inorganic acid may be

contained in an amount of at least 50 parts by weight, at least 51 parts by weight, at least 52 parts by weight, at least 53 parts by weight, at least 54 parts by weight, at least 55 parts by weight, at least 56 parts by weight, at least 57 parts by weight, at least 58 parts by weight, or at least 59 parts by weight, and at most 85 parts by weight, at most 84 parts by weight, at most 83 parts by weight, at most 82 parts by weight, at most 81 parts by weight, at most 80 parts by weight, at most 79 parts by weight, at most 78 parts by weight, or at most 77 parts by weight, based on 100 parts by weight of the total etching composition. When the etching composition includes the inorganic acid in the above amount, the etching (removal) selectivity of the nitride layer may be further improved to prevent particles from being produced.

[70] Meanwhile, a silanol-based compound contained in the etching composition corresponds to an additive which is contained in the etching composition described above. Accordingly, the silanol-based compound may be contained in the etching composition to increase the etch selectivity of the nitride layer and to prevent particles from being produced while controlling the abnormal growth of the particles. Si-based compounds having various structures are well known as additives to be contained in the etching composition. Among them, the silanol-based compound having the structure of Si-OH in a molecular structure may better perform a function of the additive.

[71] In particular, the silanol-based compound may be a silanol-based compound represented by following Chemical Formula 1 or a condensate of the silanol-based compound:

[72] [Chemical Formula 1]



[73] in Chemical Formula 1,

[74] R_1 is selected from the group consisting of an aminoalkyl group having 1 to 20 carbon atoms, an alkoxy group having 1 to 20 carbon atoms, an acetyloxy group, and a haloalkyl acetyloxy group having 1 to 20 carbon atoms, and R_2 and R_3 are hydroxy groups.

5 [75] In particular, it is known that a Si-based compound, in which each of R_2 and R_3 in the structure of Chemical Formula 1 is an alkoxy group instead of a hydroxy group, is particularly suitable as the additive of the etching composition. However, when the material is employed for the etching composition, a color may be changed or particles may be produced to disturb the etching process or to produce a large amount of bubbles immediately
10 after the etching composition is formed, thereby damaging etching equipment and degrading the efficiency of the etching process. According to the present disclosure, the etching composition may realize excellent performance and stability without causing the above-described problem, by using the silanol-based compound represented by Chemical Formula 1 or the condensate thereof as the additive, instead of the Si-based compound having
15 the above-described alkoxy group.

[76] Meanwhile, according to the present disclosure, in the silanol-based compound used in the etching composition, the condensate of the silanol-based compound refers to a compound formed by condensation or bonding of at least two silanol-based compounds. For example, the silanol-based compound represented by Chemical Formula 1 has three Si-OH
20 bonds. Accordingly, the Si-OH structure of one molecule may react with the Si-OH structure of another molecule to form a bonding structure. Compounds having various structures which may be formed through such a process may be referred to as the condensate.

[77] In particular, although the specific principle thereof may not be clearly confirmed, the etching composition according to the present disclosure includes the silanol-based
25 compound or the condensate thereof. Accordingly, the APHA value measured for the etching

composition may be less than 1.5, which is significantly low. Accordingly, when the APHA value of the etching composition is low as described above, the etching composition may hardly exhibit a color, such that the etching process may be smoothly performed. More specifically, the color of the etching composition may be substantially transparent, which
5 hardly shows a color, due to the lower APHA value. In this case, when a color is changed due to particles produced during the etching process or the side reaction made during the process, the color change may be immediately recognized and may be handled. As the result is utilized for setting the process condition, the process condition may be optimized to prevent the side reaction from being made. However, when the etching composition has a color, the
10 color change may be handled later, and the fine color change may not be handled. Accordingly, the problems caused during the process may not be recognized. In particular, when the etching composition has a color, as the process proceeds, a color may be deposited on a part of a device. The above problem may be more accelerated.

[78] According to an embodiment of the present disclosure, preferably, the silanol-based
15 compound may be an aminoalkylsilanetriol or a condensate thereof. Specifically, the silanol-based compound may be 3-aminopropylsilanetriol or a condensate thereof. More specifically, the silanol-based compound may have CAS No. 68400-07-7. The silanol-based compound may exhibit the significantly improved effect in terms of, especially, the selectivity of the nitride layer over the oxide layer while the APHA value of the etching
20 composition is maintained to be less than 1.5.

[79] According to an embodiment of the present disclosure, the etching composition according to the present disclosure may have the APHA value of less than 1.5, and preferably, the APHA value of at most 1.45, at most 1.4, at most 1.3, at most 1.2, at most 1.1, at most 1.0, at most 0.9, at most 0.8, at most 0.7, at most 0.6, at most 0.5, at most 0.4, at most
25 0.3, at most 0.2, at most 0.1, or 0. According to an embodiment of the present disclosure, the

etching composition has the lower APHA value as described above. Accordingly, the etching process is not prevented from being disturbed, as a color is hardly exhibited. When the etching composition has the higher APHA value, the etching composition may be discolored and may serve as an interference factor in measurement using an instrument such as a spectrophotometric concentration meter. Meanwhile, the APHA value may be measured in compliance with the ASTM-D1209.

[80] According to an embodiment of the present disclosure, the silanol-based compound may be, based on 100 parts by weight of the whole etching composition, at least 0.1 part by weight, at least 0.5 part by weight, at least 1 part by weight, at least 1.5 parts by weight, at least 2 parts by weight, at least 3 parts by weight, more than 3 parts by weight, at least 3.5 parts by weight, at least 4 parts by weight, at least 4.5 parts by weight, at least 5 parts by weight, at least 5.5 parts by weight, or at least 6 parts by weight, and may be less than 10 parts by weight, at most 9.5 parts by weight, at most 9 parts by weight, at most 8.5 parts by weight, at most 8 parts by weight, at most 7.5 parts by weight, or at most 7 parts by weight.

When the silanol-based compound exceeds the above range, the silanol-based compound may serve as foreign substances. As the content of the silanol-based compound is increased, the content of the inorganic acid may be decreased, such that the etch rate is degraded. When the silanol-based compound is less than the above range, the etching composition may not be utilized in a higher-temperature process, the abnormal growth may not be sufficiently prevented, the etch selectivity may not be ensured, and the bubble may not be prevented from being produced. The content of the silanol-based compound is different from the content of a silanol-based compound in a typical etching composition for the nigrade layer, which is about at most 3 wt% based on the whole content of the etching composition even if the silanol-based compound is contained in the typical etching composition. In contrast, according to the present disclosure, the etching composition contains the silanol-based

compound in the content greater than the content of the silanol-based compound in the conventional etching composition, and preferably, is used in the content ranging from 3 parts by weight to less than 10 parts by weight, based on 100 parts by weight of the etching composition, thereby maintaining the balance between the etch rate and the etch selectivity while stabilizing the etching composition and suppressing the abnormal growth and the production of bubbles of the etching composition under a higher-temperature process.

[81] In addition, according to an embodiment of the present disclosure, the etching composition may include a solvent. Specifically, the solvent may be water or deionized water (DIW). The content of the solvent may be the content of a remainder obtained by excluding the content of the inorganic acid, the content of the silanol-based compound, and, the content of the additive when the additive is added, from the entire etching composition.

[82] According to an embodiment of the present disclosure, the etching composition may further include an ammonium-based compound. The ammonium-based compound may refer to a compound which forms ammonium (NH_4^+) when dissolved in the solvent, particularly in water. The ammonium-based compound may include, for example, at least one selected from ammonia, ammonium chloride, ammonium phosphate, ammonium acetate, ammonium sulfate, ammonium formate, and a metal amine complex salt. The metal amine complex salt may be a metal complex salt including at least one ammonia (NH_3) ligand. When the etching process of the silicon nitride layer is performed for a long time, silicon ions may be excessively formed by $\text{SiO}_2\text{H}_2\text{O}$, which is a product of Reaction Equation 1. The excessively formed silicon ions may cause abnormal growth of the silicon oxide layer. When the ammonium-based compound is included in the etching composition and forms ammonium (NH_4^+), the formed ammonium may react with a precursor of the silicon ions (e.g., SiO_2) to remove the precursor of the silicon ions. Accordingly, abnormal growth of the silicon oxide layer may be prevented. In addition, the ammonium-based compound may maintain a

constant etch rate as a function of the etching time.

[83] The ammonium-based compound may be contained in an amount ranging from 0.01 parts by weight to 10 parts by weight, based on 100 parts by weight of the entire etching composition. When the etching composition further includes an ammonium-based compound, and the ammonium-based compound is contained in a content less than the range, the abnormal growth of the silicon oxide layer may not be prevented or the etch selectivity of the silicon nitride layer over the silicon oxide layer may not be prevented from being changed over time, which is different from the purpose of further including the ammonium-based compound. In addition, when the ammonium-based compound includes in an excess amount, the etch rate of the silicon nitride layer and the silicon oxide layer may be changed over time, which is different from the purpose of further including the ammonium-based compound.

[84] In addition, according to an embodiment of the present disclosure, the etching composition may further include an arbitrary additive typically well-known to improve etching performance. The additive may be a surfactant, a metal ion sequestering agent, or a corrosion inhibitor.

[85] As described above, according to the present disclosure, the etching composition may further selectively include an additive, or an ammonium-based compound, in addition to the inorganic acid and the silane-based compound. Accordingly, the remarkably higher etch selectivity of the nitride layer over the oxide layer may be exhibited. In addition, the etching composition may prevent damage to the quality of the oxide layer from being damaged or prevent electrical characteristics from being deteriorated due to etching of the oxide layer during the etching process of the nitride layer and may minimize production of particles. Accordingly, according to the present disclosure, the etching composition may be usefully employed for the etching process, when the semiconductor device is manufactured.

[86] According to an embodiment of the present disclosure, the etching composition may

be used to etch the silicon nitride. In this case, an etch selectivity of a silicon nitride layer over a silicon oxide layer may be at least 30, at least 35, at least 40, at least 45, at least 50, at least 55, at least 60, at least 65, or at least 70, and at most 1,000, at most 700, at most 500, at most 300, or at most 200. When the selectivity of the silicon nitride layer over the silicon
5 oxide layer is within the above-described range, the nitride layer may be etched with a sufficiently high selectivity, and the etch rate of the nitride layer may also be sufficiently secured.

[87] According to an embodiment of the present disclosure, for the etching composition according to the present disclosure, the etching process is performed until the silicon ion is in
10 the range from 100 ppm to 1,500 ppm, while the absolute value of the variation of the etch rate may be at most 20%, at most 19%, or at most 18%. This refers to that the etching composition according to the present disclosure shows relatively uniform etch rate of the nitride layer at various concentrations of silicon ions. While the etching process is performed, when the absolute value of the variation of the etch rate of the nitride layer is in the
15 above-described range, especially, the etching composition may exhibit the excellent stability.

[88] According to an embodiment of the present disclosure, immediately after the etching composition according to the present disclosure is formed, the etching composition may be at
most 0.5 cm, at most 0.4 cm, at most 0.3 cm, at most 0.2 cm, less than 0.2 cm, at most 0.15
20 cm, or at most 0.1 cm in the height of bubbles on the surface of the etching composition. According to the present disclosure, immediately after the etching composition is formed, the bubbles are hardly formed on the surface of the etching composition. When the height of the bubbles on the surface of the etching composition is in the above range, immediately after the etching composition is formed, the etching process may be smoothly formed without the
25 degradation in efficiency of the etching process or the damage to the etching equipment.

[89] According to an embodiment of the present disclosure, for the etching composition, the etch rate of the silicon nitride layer may range from 40 Å/min to 80 Å/min at the etching process temperature of 165°C. Preferably, the etch rate of the silicon nitride layer may be at least 40 Å/min, at least 45 Å/min, at least 50 Å/min, or at least 55 Å/min, and at most 80 Å/min or at most 75 Å/min. In addition, according to the present disclosure, the etching composition may have an etch rate of the silicon oxide layer of at most 1 Å/min at an etching process temperature of 165°C, and preferably may be at most 1 Å/min and at least 0.0001 Å/min, at least 0.01 Å/min, at least 0.1 Å/min, at least 0.2 Å/min, at least 0.3 Å/min, or at least 0.4 Å/min.

10 [90] **Method for manufacturing semiconductor device**

[91] The present disclosure provides a method for manufacturing a semiconductor device using the etching composition described above.

[92] More specifically, the present disclosure provides a method for manufacturing a semiconductor device, which includes the steps for forming a structure by stacking an insulating layer and a sacrificial layer on a substrate, and forming a space region by performing an etching process using the etching composition to remove the sacrificial layer.

[93] The description about the etching composition according to the present disclosure will be identically applied to the description about the method for manufacturing the semiconductor device according to the present disclosure.

20 [94] Hereinafter, the method for manufacturing the semiconductor device according to the present disclosure will be described in detail.

[95] The term “space” used in a “space region” or a “space part” employed in the present disclosure is collectively referred to as a space formed by removing the sacrificial layer in the etching process of the semiconductor device. For example, the “space” may include, but is not limited to, a trench, a channel, a gate, or a spacer.

[96] In addition, the term “deposition part” used in the present disclosure may refer to a part including a portion formed by depositing a conductive material or an insulating material in the space region or the space part described above. The term “deposition part” may be patterned and configured.

5 [97] FIG. 1 is a plan view of a semiconductor device according to embodiments of the present disclosure. FIGS. 2 to 8 are views to describe a method for manufacturing a semiconductor device according to embodiments, which correspond to sections taken along line I-I' of FIG. 1. Hereinafter, the description, which has been made above, will be omitted to avoid the redundancy.

10 [98] According to the present disclosure, referring to FIGS. 1 and 2, a stack structure 200 may be formed on a substrate 100. The substrate 100 may be a bulk silicon substrate, a silicon-on-insulator (SOI) substrate, a germanium on insulator (GOI) substrate, a silicon-germanium substrate, or an epitaxial thin film substrate obtained by performed a selective epitaxial growth (SEG). A first direction D1 and a second direction D2 may be
15 parallel to a top surface 100a of the substrate 100. The second direction D2 may cross the first direction D1. A third direction D3 may be perpendicular to the top surface 100a of the substrate 100.

[99] According to an embodiment of the present disclosure, the stack structure 200 may include sacrificial layers SC and insulating layers IL. Forming the stack structure 200 may
20 include forming the stack structure 200 by alternately and repeatedly the sacrificial layers SC and the insulating layers IL on the substrate 100. Each of the sacrificial layers SC may be interposed between the insulating layers IL. The sacrificial layer SC may have an etch selectivity relative to the insulating layer IL. The sacrificial layer SC may include, for example, silicon nitride (e.g., Si_xN_y). The insulating layers IL may include a silicon oxide
25 (e.g., Si_xO_y). The insulating layers IL may be formed of tetraethoxysilane (TEOS), and

tetraethoxysilane may be expressed as $C_2H_5O_4Si$.

[100] According to an embodiment of the present disclosure, the sacrificial layers SC may have thicknesses substantially equal to each other. Otherwise, a lowermost sacrificial layer SC and an uppermost sacrificial layer SC among the sacrificial layers SC may be thicker than
5 sacrificial layers SC interposed between the lowermost sacrificial layer SC and the uppermost sacrificial layer SC. In addition, the insulating layers IL may have thicknesses equal to each other, and at least two of the insulating layers IL may be different from each other. The lowermost insulating layer IL among the insulating layers IL may have thicknesses thinner than of thicknesses of the sacrificial layers SC and the insulating layers IL formed on the
10 lowermost insulating layer IL. The lowermost insulating layer IL among the insulating layers IL may be a silicon oxide layer formed through a thermal oxidation process. In this specification, the thickness of a certain component may refer to a distance of the certain component in the third direction D3.

[101] According to the present disclosure, referring to FIGS. 1 and 3, openings 210 and
15 vertical structures 300 may be formed in the stack structure 200. The forming of the openings 210 may include forming a mask pattern (not illustrated) defining the positions of the openings 210 on the stack structure 200 when viewed in a plan view and etching the stack structure 200 by using the mask pattern serving as an etching mask. The stack structure 200 may be etched through an anisotropic etching process.

[102] According to an embodiment of the present disclosure, the openings 210 may be
20 formed through the stack structure 200. Sidewalls of the openings 210 may expose the sacrificial layers SC and the insulating layers IL. The openings 210 may expose the substrate 100. The top surface 100a of the substrate 100 may be over-etched while the openings 210 are formed. In this case, the top surface 100a, which is exposed through the openings 210, of
25 the substrate 100 may be recessed to a specific depth.

[103] According to the present disclosure, the etching composition may be used to uniformly etch surfaces, which are exposed through the openings 201, of the sacrificial layers SC and the insulating layers IL.

[104] To uniformly etch the surfaces, which are exposed from an upper portion to a lower portion of the openings 201, of the sacrificial layers SC and the insulating layers IL, the etching composition according to the present disclosure has an etch rate ranging from 20 Å/min to 55 Å/min with respect to the sacrificial layers SC at an etching process temperature of 165°C.

[105] When the etch rate deviates from the range under the etching process temperature, the surfaces, which are exposed from the upper portion to the lower portion of the openings 201, of the sacrificial layers SC and the insulating layers IL may not be uniformly etched.

[106] According to an embodiment of the present disclosure, each of the openings 201 may be provided in the form of a cylindrical hole or a rectangular parallelepiped hole. Lower portions of the openings 210 may have widths narrower than those of upper portions of the openings 210. As illustrated in FIG. 1, the openings 210 may form columns parallel to the second direction D2 when viewed in a plan view. The openings 210 between two adjacent columns may be arranged in a zigzag pattern in the second direction D2. The openings 210 may form an array aligned in the first direction D1 and the second direction D2, which is different from FIG. 1. For example, the openings 210 in two adjacent columns may be aligned in the first direction D1 to form an array.

[107] According to an embodiment of the present disclosure, first dielectric patterns 310 may be formed in the openings 210. The first dielectric patterns 310 may cover the sidewalls of the openings 210. The first dielectric patterns 310 may expose the top surface 100a of the substrate 100. The first dielectric pattern 310 may include a single insulating layer or multiple insulating layers. The first dielectric pattern 310 may serve as a part of a data storage layer of

a charge trap flash memory transistor. The first dielectric pattern 310 will be described below with reference to FIG. 9 according to embodiments.

[108] According to an embodiment of the present disclosure, the semiconductor patterns 320 may be formed in the openings 210. The semiconductor patterns 320 may include, for example, silicon (Si), germanium (Ge), or the mixture thereof. The semiconductor patterns 320 may have a crystal structure including at least one of single crystal, amorphous, and polycrystalline. The semiconductor patterns 320 may further include a doped impurity. As another example, the semiconductor patterns 320 may be an intrinsic semiconductor in an undoped state. The semiconductor patterns 320 may be formed using a thermal chemical vapor deposition (Thermal CVD), a plasma enhanced chemical vapor deposition (Plasma enhanced CVD), or an atomic layer deposition (ALD) technique.

[109] According to an embodiment of the present disclosure, the semiconductor patterns 320 may be formed on the sidewalls of the openings 210 to cover the first dielectric patterns 310. The semiconductor patterns 320 may extend onto the substrate 100 to make contact with a portion of the top surface 100a, which is exposed through the opening 210, of the substrate 100. Each of the semiconductor patterns 320 may be formed in a pipe shape, a hollow cylindrical shape, or a cup shape in a relevant one of the openings 210. The semiconductor patterns 320 may define empty regions 321 at central portions of the openings 210.

[110] According to an embodiment of the present disclosure, a buried insulating pattern 330 may each be buried in the empty regions 321. The buried insulating patterns 330 may be formed of an insulating material having excellent gap-fill characteristics. For example, the buried insulating patterns 330 may be formed of, for example, a high-density plasma oxide layer, a spin-on-glass (SOG) layer, an ALD oxide layer, and/or a CVD oxide layer.

[111] According to an embodiment of the present disclosure, pads 340 may be formed on the vertical structures 300. The pads 340 may be formed of a conductive material such as a

semiconductor material doped with an impurity or a conductive material such as a metal. A bottom surface of each of the pads 340 may be disposed at a level higher than a level for the top surface of the uppermost sacrificial layer SC. A lower capping layer 510 may be formed on a top surface of each of the vertical structures 300 and the stack structure 200. The lower
5 capping layer 510 may include an insulating material such as a silicon oxide, a silicon nitride, and/or a silicon oxynitride.

[112] Referring to FIG. 4 of the present disclosure, trenches 600 may be formed through the stack structure 200 and the lower capping layer 510. The forming of the openings 600 may include forming a mask pattern (not illustrated) defining the positions of the openings
10 600 on the stack structure 200 when viewed in a plan view and etching the stack structure 200 by using the mask pattern serving as an etching mask. The etching of the stack structure 200 may be performed through an anisotropic etching process.

[113] According to an embodiment of the present disclosure, the trenches 600 may be formed between the vertical structures 300 adjacent to each other. The trenches 600 may be
15 spaced apart from the vertical structures 300 to expose sidewalls of the sacrificial layers SC and sidewalls of the insulating layers IL. The upper portions of the trenches 600 may have widths wider than widths of lower portions of the trenches 600. The trenches 600 may expose the top surface 100a of the substrate 100. During forming the trenches 600, the top surface 100a of the substrate 100 exposed through the trenches 600 may be recessed to a specific
20 depth through an over-etching manner. As illustrated in FIG. 1, the trenches 600 may have long axes parallel to the second direction D2 when viewed in a plan view. The trenches 600 may be spaced apart from each other in the first direction D1.

[114] Referring to FIG. 5 according to the present disclosure, the sacrificial layers SC may be etched to form gate regions 250. The gate regions 250 may be voids and may be regions
25 for forming gate electrode patterns 450 in FIG. 7. The gate regions 250 may be formed

between the insulating layers IL and may be connected to the trenches 600. The gate regions 250 may expose portions of the sidewalls 300c of the vertical structures 300. Thicknesses of the gate regions 250 may be substantially equal to thicknesses of the removed sacrificial layers SC. The etching of the sacrificial layers SC may be performed through an etching
5 process using an etching composition. The etching process may be a wet etching process.

[115] According to an embodiment of the present disclosure, the etching composition may be an etching composition according to the present disclosure described above. Since the sacrificial layers SC include silicon nitride, the sacrificial layers SC may be etched by phosphoric acid as expressed in Reaction Equation 1.

10 **[116]** According to an embodiment of the present disclosure, for example, the etching composition may be supplied onto the substrate 100 at a temperature ranging from 150°C to 200°C, specifically, from 155°C to 170°C. Under the temperature condition, the inorganic acid may further etch silicon oxide as well as the sacrificial layers SC. The insulating layers IL may include silicon oxide. According to embodiments, the etching composition may
15 include a silanol-based compound, such that etching of the insulating layers IL by the inorganic acid may be prevented or reduced. For example, in the etching process, oxygen of the silanol-based compound may be bonded to surfaces of the insulating layers IL to protect the insulating layers IL. Accordingly, during the etching process, the insulating layers IL may exhibit a low etch rate. Oxygen atoms of the silanol-based compound may not make the
20 interaction (e.g., hydrogen bonding) with surfaces of the sacrificial layers SC. Accordingly, etch selectivity of the sacrificial layers SC over the insulating layers IL may be increased. When the silanol-based compound is unstable, by-products may be formed, and the by-products may form particles. The by-products and/or the particles may cause defects during the manufacturing process of a semiconductor device. For example, the by-products
25 and/or the particles may be adsorbed onto the insulating layers IL. Since the bonding between

a silicon atom and an oxygen atom in the silanol-based compound is stable, the by-product in the etching process may be prevented from being formed. As the sacrificial layers SC are etched, silicon ions (e.g., $\text{SiO}_2\text{H}_2\text{O}$) may be formed. An ammonium-based compound may remove the silicon ions produced during etching of the sacrificial layer SC. Accordingly, the abnormal growth of the insulating layers IL by the silicon ions may be prevented/reduced.

[117] According to an embodiment of the present disclosure, the etching composition may be applied onto the substrate 100 through a coating manner, a dipping manner, a spraying manner, or an injecting manner during the etching process. When the etching composition is applied through a deposition manner, a batch-type device may be used during the etching process. When the etching composition is sprayed onto the substrate 100, a single wafer type device may be used during the etching process. After the etching process, a cleaning process and a drying process using the ultrapure water may be performed on the substrate 100. The ultrapure water may refer to water having an impurity of at most 100 ppb.

[118] According to the present disclosure, referring to FIG. 6, a second dielectric pattern 410 and a gate conductive film 451 may be formed on the stack structure 200 and inside the tranches 600. The second dielectric pattern 410 may be substantially and conformally formed on the stack structure 200 and inside the tranches 600. The second dielectric pattern 410 may extend into the trenches 600 and the gate regions 250. The second dielectric pattern 410 may conformally cover the top surface of the uppermost insulating layer IL of the insulating layers IL, sidewalls, which are exposed through the trenches 600, of the insulating layers IL, top surfaces and bottom surfaces, which are exposed through the gate regions 250, of the insulating layers IL, sidewalls 300c, which are exposed through the gate regions 250, of the vertical structures 300, and the top surface 100a of the substrate 100. The second dielectric pattern 410 may be formed through a deposition process. As the deposition manner and the deposition condition are adjusted, the second dielectric pattern 410 may be formed to have

excellent step coverage. For example, the deposition process for the second dielectric pattern 410 may be performed through a chemical vapor deposition manner or an atomic layer deposition manner. The second dielectric pattern 410 may include a single layer or a plurality of layers. The second dielectric pattern 410 may serve as a part of a data storage layer DS of a charge trap flash memory transistor. For example, the second dielectric pattern 410 according to embodiments may be described below with reference to FIG. 9. The gate conductive layer 451 may be formed on the second dielectric pattern 410. The gate conductive layer 451 may be buried in at least a part of each of the trenches 600 and the gate region 250. Unlike illustrated, the gate conductive layer 461 may be fully buried in each of the trenches 600.

Although not illustrated, as the barrier metal layer and the metal layer are sequentially deposited, the gate conductive layer 451 may be formed. The barrier metal layer may include a metal nitride such as titanium nitride (TiN), tantalum nitride (TaN), or tungsten nitride (WN). The metal layer may include tungsten (W), aluminum (Al), titanium (Ti), tantalum (Ta), cobalt (Co), or copper (Cu).

[119] According to the present disclosure, referring to FIGS. 1 and 7, as the gate conductive layer 451 is patterned, gate electrode patterns 459 may be formed in the gate regions 250, respectively. The gate conductive layer 451 may be patterned through the etching process. In this case, the second dielectric pattern 410 may be further etched. During the etching process for the gate conductive layer 451, the gate conductive layer 451 may be removed from the substrate 100. The gate conductive layer 451 may be etched until the insulating layers IL are removed from the sidewalls of the insulating layers IL and the sidewalls of the insulating layers IL are exposed. Accordingly, the gate electrode patterns 450 and the second dielectric pattern 410 may be localized at the gate regions 250, and the gate structures 400 may be formed. Each of the gate structures 400 may be formed two trenches 600 adjacent to each other. The sidewalls of the gate structure 400 may be exposed to the

tranches 600. The gate structures 400 may expose the top surface 100a of the substrate 100 inside the trenches 600. The top surface 100a, which is exposed, of the substrate 100 may be further etched. As illustrated in FIG. 1, the gate structures 400 may have major axes parallel to the second direction D2, when viewed in a plan view. The gate structures 400 may be spaced apart from each other in the first direction D1.

[120] According to an embodiment of the present disclosure, each of the gate structures 400 may include the gate electrode patterns 450, the second dielectric pattern 410, and the insulating layers IL stacked on each other. In each gate structure 400, the gate electrode pattern 450 may be interposed between the insulating layers IL. The gate electrode patterns may be used for a string select line, a ground select line, and word lines. For example, the uppermost portion (or the uppermost gate electrode pattern) and the lowermost portion (or the lowermost gate electrode pattern) of the gate electrode patterns 450 stacked on each other may be used as the string select line and the ground select line, respectively. The gate electrode patterns 450 intermediate between the uppermost gate electrode pattern 450 and the lowermost gate electrode pattern 450 may be used as word lines.

[121] According to an embodiment of the present disclosure, in the gate structures 400, the second dielectric pattern 410 may be interposed between the gate electrode patterns 450 and the insulating layers IL and between the vertical structure 300 and the insulating layers IL.

[122] According to an embodiment of the present disclosure, common source regions CSR may be formed in portions, which are exposed to the trenches 600, of the substrate 100. The common source regions CSR may be spaced apart from each other in the second direction D2. The common source regions CSR may be formed through an ion implanting process in which the gate structures 400 are employed as an ion mask. The common source regions CSR may be partially overlapped with a lower portion of the gate structures 400 when viewed in a plan view, as impurities are spread. The common source regions CSR may have a conductive

type different from a conductive type of the substrate 100. For example, the common source regions CSR may be performed, after the tranches in FIG. 4 are formed.

[123] According to the present disclosure, referring to FIGS. 1 and 8, each spacer 550 and each common source plug CSP may be formed in a relevant one of the tranches 600. The
5 spacers 500 may cover the sidewalls of the gate structures 400. The spacers 500 may include insulating materials. The spacers 550 may be formed of a silicon oxide, a silicon nitride, a silicon oxynitride, or a low-k material. The forming of the spacers 550 may include covering the gate structures 400 by depositing a spacer film (not illustrated) having a uniform thickness on the substrate 100 to cover the gate structures 400, and exposing the common
10 source regions CSR by performing an etch-back process for the spacer layer.

[124] According to an embodiment of the present disclosure, the common source plugs CSP may be formed on spacers 550 and may be buried in the trenches 600. The common source plugs CPS may make contact with the common source regions CSR, respectively. The forming of the common source plug CSP may include depositing a barrier metal layer (not
15 illustrated) to cover the sidewalls of the spacers 550 and depositing a metal layer (not illustrated) on the barrier metal layer. For example, the barrier metal layer may include at least one selected from tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), tungsten (W), tungsten nitride (WN), and a combination thereof. The metal layer may include tungsten (W), aluminum (Al), titanium (Ti), tantalum (Ta), cobalt (Co), or copper
20 (Cu) As illustrated in FIG. 1, when viewed in a plan view, the main axes of the common source plugs CPS may extend in parallel to the second direction D2.

[125] According to an embodiment of the present disclosure, as an upper capping layer 520 is formed on a lower capping layer 510, the upper capping layer 520 may cover the top surface of the common source plug CSP. The upper capping layer 520 may include an
25 insulating material.

[126] According to an embodiment of the present disclosure, bit line contact plugs 530 may be formed in the upper capping layer 520. The bit line contact plugs 530 may make contact with pads 340, respectively, through the upper capping layer 520 and the lower capping layer 510. The bit line contact plugs 530 may be electrically connected to the vertical structures 300 (e.g., the semiconductor patterns 320) through the pads 340. Bit lines BL may be formed on the upper capping layer 520 to be connected to the bit line contact plugs 530. As illustrated in FIG. 1, the bit lines BL may extend in the first direction D1 when viewed in a plan view. The bit line contact plugs 530 and the bit lines BL may include a conductive material such as metal. Accordingly, the semiconductor device 1 may be completely manufactured. The semiconductor device 1 may be a three-dimensional memory device.

[127] FIG. 9 is a view to describe insulating patterns of the semiconductor device according to embodiments of the present disclosure, and illustrates an enlarged view of region A of FIG. 8. In the following description made with reference to FIG. 9, a singular insulating layer, a singular gate electrode pattern, and a singular vertical structure will be described for simplification.

[128] According to the present disclosure, referring to FIGS. 8 and 9, a first dielectric pattern 310 may include a tunnel insulating layer 311, a charge storage layer 312, and a first blocking insulating layer 313. The tunnel insulating layer 311 may extend along the vertical structure. The charge storage layer 312 and the first blocking insulating layer 313 may be stacked on the tunnel insulating layer 311. The tunnel insulating layer 311 may be formed of a material having a dielectric constant lower than a dielectric constant of the first blocking insulating layer 313. For example, the tunnel insulating layer 311 may include at least one selected from the group consisting of an oxide material, a nitride material, and an oxide nitride material. Alternatively, the tunnel insulating layer 311 may include a high-k material. The high-k material refers to an insulating material which has a dielectric constant higher

than a dielectric constant of silicon oxide and may include a zirconium oxide, an aluminum oxide, and/or a hafnium oxide. The charge storage layer 312 may be interposed between the tunnel insulating layer 311 and the first blocking insulating layer 313. The charge storage layer 312 may include at least one of a charge trap insulating layer, a floating gate electrode,
5 or conductive nano dots. The first blocking insulating layer 313 may include the high-k material.

[129] According to an embodiment of the present disclosure, the second dielectric pattern 410 may include a second blocking insulating layer. The second blocking insulating layer may be interposed between the gate electrode pattern 450 and the first dielectric pattern 310
10 and between the gate electrode pattern 450 and the insulating layer IL. The second blocking insulating layer may include a high-k material. For example, the first blocking insulating layer 313 may include a high-k material, and the second blocking insulating layer may be a material having a dielectric constant smaller than a dielectric constant of the first blocking insulating layer 313. As another example, the second blocking insulating layer may be one of
15 high-k materials, and the first blocking insulating layer 313 may be a material having a dielectric constant smaller than the dielectric constant of the second blocking insulating layer.

[130] According to an embodiment of the present disclosure, the first dielectric pattern 310 and the second dielectric pattern 410 may function as data storage layers. The data stored in the data storage layer may be changed using Fowler–Nordheim tunneling, and the
20 Fowler–Nordheim tunneling may be induced by a voltage difference between the vertical structure 300 and the gate electrode pattern 450.

[131] According to an embodiment of the present disclosure, the second dielectric pattern 410 may not be formed, which is different from those of the drawings. As another example, the first blocking insulating layer 313 may not be formed.

25 **[132]** Hereinafter, examples of the present disclosure will be described in detail so that

those skilled in the art to which the present disclosure pertains may readily reproduce the present disclosure. However, the present disclosure may be implemented in various forms, and is limited to examples described herein.

[133] Examples 1 to 7: Preparing of etching composition

5 **[134]** An etching composition was prepared in the form of a composition described in following Table 1. Specifically, an 85 wt% aqueous solution was used for phosphoric acid, and the content of the phosphoric acid in each etching composition was adjusted. The etching composition additionally included water in addition to the phosphoric acid aqueous solution. As the silanol-based compound, a compound having CAS No. 68400-07-7 was contained in
10 the content described in Table 1 to prepare the etching composition as illustrated in Table 1.

[135] Comparative examples 1 and 12: Preparation of Etching Composition

[136] In Comparative Example 1, only a phosphoric acid aqueous solution (85 wt% phosphoric acid aqueous solution) used in preparing the Example was used as the etching composition without using the silanol-based compound. In each of Comparative Examples 2
15 to 8, the etching composition was prepared by containing, as the silanol-based compound, a compound having CAS No. 58160-99-9 in the content described in following Table 1. In each of Comparative Examples 9 to 12, the etching composition was prepared by containing a different type of silicon additive in the content described in following Table 1, instead of the silanol-based compound.

20 **[137]** The compositions according to the Examples and the Comparative Examples were shown as shown in following Table 1. Meanwhile, in following Table 1, the APHA value was measured in compliance with ASTM-D1209.

[Table 1]

	Phosphoric acid	Type of additive	Additive	Solvent (water)	APHA value
--	-----------------	------------------	----------	-----------------	------------

	Content [wt%]		Content [wt%]	Content [wt%]	
Example 1	84.575	CAS 68400-07-7	0.5	14.925	0
Example 2	84.15	CAS 68400-07-7	1	14.85	0
Example 3	82.025	CAS 68400-07-7	3.5	14.475	0
Example 4	80.75	CAS 68400-07-7	5	14.25	0
Example 5	79.475	CAS 68400-07-7	6.5	14.025	0
Example 6	78.2	CAS 68400-07-7	8	13.8	0
Example 7	76.925	CAS 68400-07-7	9.5	13.575	0
Comparative Example 1	85	-	-	15	0
Comparative Example 2	84.575	CAS 58160-99-9	0.5	14.925	1.5
Comparative Example 3	84.15	CAS 58160-99-9	1	14.85	2.9
Comparative Example 4	82.025	CAS 58160-99-9	3.5	14.475	14.2
Comparative Example 5	80.75	CAS 58160-99-9	5	14.25	17.8
Comparative Example 6	79.475	CAS 58160-99-9	6.5	14.025	24.5
Comparative Example 7	78.2	CAS 58160-99-9	8	13.8	27.5
Comparative Example 8	76.925	CAS 58160-99-9	9.5	13.575	33.4
Comparative	80.75	MTES	5	14.25	Measurement fail

Example 9					
Comparative Example 10	79.05	TEOS	7	13.95	Measurement fail
Comparative Example 11	79.9	APTMS	6	14.1	2.6
Comparative Example 12	77.35	APTMS	9	13.65	1.6

- MTES: methyltriethoxysilane
- TEOS: tetraethoxysilane
- APTMS: 3-aminopropyltrimethoxysilane

5 [138] As confirmed through Table 1, even if the silanol-based compound is used as the additive, the APHA value of the etching composition may vary significantly depending on the type of the silanol-based compound used. In particular, as the content of the additive increases, the difference in the APHA value of the etching composition was confirmed to become larger. This refers to that the APHA value of the etching composition may vary

10 depending on the additive contained in the etching composition. Meanwhile, in each of Comparative Examples 9 and 10, the etching composition could not measure the APHA value. The APHA value could be measured only in a liquid state which was transparent without turbidity. However, the etching composition of Comparative Examples 9 and 10 exhibited an opaque characteristic, such that the APHA value could not be measured.

15 [139] **Experimental example 1: Measurement of Etch rate and Selectivity**

[140] The nitride and the oxide layer were etched using the etching composition prepared according to each of the Examples and the Comparative Examples, at the process temperature of 165°C. The etch rate of each of the nitride layer and the oxide layer was measured using

the ellipsometer (SEMG-1000, NANO VIEW), which is a device for measuring a thin-film thickness, and the result is shown in following Table 2. Specifically, each rate in following Table 2 is a numeric value calculated by etching each layer for 300 seconds and dividing the difference between a layer thickness before etching the layer and a layer thickness after etching the layer by an etching time (minute).

[Table 2]

	Phosphoric acid Content [wt%]	Type of additive	Additive Content [wt%]	Solvent (water) Content [wt%]	SIN (Å/min)	TEOS (Å/min)	Selectivity
Example 1	84.575	CAS 68400-07-7	0.5	14.925	75.04	2.01	37.33
Example 2	84.15	CAS 68400-07-7	1	14.85	73.15	1.57	46.59
Example 3	82.025	CAS 68400-07-7	3.5	14.475	70.01	0.95	73.69
Example 4	80.75	CAS 68400-07-7	5	14.25	68.71	0.74	92.85
Example 5	79.475	CAS 68400-07-7	6.5	14.025	63.4	0.63	100.63
Example 6	78.2	CAS 68400-07-7	8	13.8	60.31	0.41	147.10
Example 7	76.925	CAS 68400-07-7	9.5	13.575	58.32	0.38	153.47
Comparative Example 1	85	-	-	15	80.6	3.02	26.69
Comparative Example 9	80.75	MTES	5	14.25	72.65	0.21	345.95
Comparative Example 10	79.05	TEOS	7	13.95	62.65	0	-
Comparative Example 11	79.9	APTMS	6	14.1	70.15	0.15	467.67

Comparative Example 12	77.35	APTMS	9	13.65	67.01	0.07	957.29
---------------------------	-------	-------	---	-------	-------	------	--------

[141] According to Table 2, it may be confirmed that the etch rate selectivity of the nitride and oxide layer according to Examples corresponding to the etching composition of the present disclosure had a higher value of at least 30, and even the etch rate of the nitride layer was higher.

5 [142] **Experimental example 2: Analysis of abnormal growth suppression level of etching composition**

[143] The etching process was performed as illustrated in Experimental Example 1 using the etching composition according to Examples. Thereafter, a solution was collected from a silicon oxide layer, and an etch rate when the concentration of the silicon ion in the solution was 100 ppm, 300 ppm, 500 ppm, 1,000 ppm, and 1,500 ppm, and an etch rate after the etchant was filtered were measured (hereinafter, this is referred to as a dummy etch rate). In addition, the results were shown in Tables 3 to 6. Accordingly, whether the abnormal growth was suppressed even in the long-term etching process, and whether the etching stability was present may be determined.

15 [Table 3]

	Other aditives	Dummy	Phosphoric acid Content [wt%]	Additive Content [wt%]	Solvent (water) Content [wt%]	(Before filtering) SIN (Å/min)	(Before filtering) TEOS (Å/min)	(After filtering) SIN (Å/min)	(After filtering) TEOS (Å/min)
Comparative Example 1	N-phosphoric acid	100	85	-	15	75.26	0.15	78.26	1.26
Example 1	-	100	84.575	0.5	14.925	71.35	1.38	71.27	1.3

Example 2			84.15	1	14.85	70.55	1.04	70.23	1.01
Example 3			82.025	3.5	14.475	69.36	0.96	69.08	0.98
Example 4			80.75	5	14.25	68.45	0.7	68.23	0.69
Example 5			79.475	6.5	14.025	63.26	0.64	66.11	0.66
Example 6			78.2	8	13.8	59.89	0.45	59.41	0.44
Example 7			76.925	9.5	13.575	58.36	0.38	58.13	0.35
Example 1		300	84.575	0.5	14.925	64.59	-0.05	67.97	0.83
Example 2			84.15	1	14.85	62.01	0.01	61.85	0.02
Example 3			82.025	3.5	14.475	68.06	0.02	68.03	0.02
Example 4			80.75	5	14.25	65.82	0.01	65.14	0.01
Example 5			79.475	6.5	14.025	60.75	0.04	65.23	0.03
Example 6			78.2	8	13.8	58.33	0.04	58.16	0.04
Example 7			76.925	9.5	13.575	56.1	0.07	56.58	0.06
Example 1		500	84.575	0.5	14.925	58.44	-0.07	64.52	0.02
Example 2			84.15	1	14.85	61.33	-0.03	63.56	0.03
Example 3			82.025	3.5	14.475	65.4	0.01	65.08	0.01
Example 4			80.75	5	14.25	59.02	0.02	59.11	0.02
Example 5			79.475	6.5	14.025	57.52	0.02	57.83	0.02
Example 6			78.2	8	13.8	56.02	0.02	56.41	0.02
Example 7			76.925	9.5	13.575	55	0.02	55.05	0.02

[Table 4]

	Other additives	Dummy	Phosphoric acid Content [wt%]	Additive Content [wt%]	Solvent (water) Content [wt%]	(Before filtering) SIN (Å/min)	(Before filtering) TEOS (Å/min)	(After filtering) SIN (Å/min)	(After filtering) TEOS (Å/min)
--	--------------------	-------	--	------------------------------	--	---	--	--	---

Comparative Example 1	N-phosphoric acid	100	85	-	15	75.26	0.15	78.26	1.26
Example 1	-	1000	84.575	0.5	14.925	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Example 2			84.15	1	14.85	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Example 3			82.025	3.5	14.475	60.6	0	60.14	0
Example 4			80.75	5	14.25	51.22	0	51.05	0
Example 5			79.475	6.5	14.025	48.2	0	48.16	0
Example 6			78.2	8	13.8	45.22	0	45.23	0
Example 7			76.925	9.5	13.575	44.96	0	45.06	0
Example 1		1500	84.575	0.5	14.925	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Example 2			84.15	1	14.85	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Example 3			82.025	3.5	14.475	52.03	-0.04	52.09	-0.06
Example 4			80.75	5	14.25	46.51	-0.02	46.38	-0.01
Example 5			79.475	6.5	14.025	44.03	-0.02	44.07	-0.01
Example 6			78.2	8	13.8	40.03	-0.01	40.13	0
Example 7			76.925	9.5	13.575	38.96	-0.01	38.59	0

[Table 5]

	Other additives	Dummy	Phosphoric acid Content [wt%]	Additive Content [wt%]	Solvent (water) Content [wt%]	(Before filtering) SIN (Å/min)	(Before filtering) TEOS (Å/min)	(After filtering) SIN (Å/min)	(After filtering) TEOS (Å/min)
--	-----------------	-------	-------------------------------	------------------------	-------------------------------	--------------------------------	---------------------------------	-------------------------------	--------------------------------

Comparative Example 1	N-phosphoric acid	100	85	-	15	75.26	0.15	78.26	1.26
Comparative Example 9		100	80.75	MTES 5	14.25	52.10	0.03	52.07	0.02
Comparative Example 10			79.05	TEOS 7	13.95	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Comparative Example 11			79.9	APTMS 6	14.1	56.26	0.05	55.59	0.05
Comparative Example 12			77.35	APTMS 9	13.65	55.10	0.04	55.66	0.04
Comparative Example 9		300	80.75	MTES 5	14.25	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Comparative Example 10			79.05	TEOS 7	13.95	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Comparative Example 11			79.9	APTMS 6	14.1	54.79	-0.02	55.01	0.02
Comparative Example 12			77.35	APTMS 9	13.65	53.28	-0.04	55.52	0.02
Comparative Example 9		500	76.5	MTES 5	18.5	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Comparative Example 10			72.25	TEOS 7	20.75	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Comparative Example 11			79.9	APTMS 6	14.1	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Comparative			77.35	APTMS 9	13.65	Measurement	Measurement	Measurement	Measurement

Example 12						fail	fail	fail	ent fail
------------	--	--	--	--	--	------	------	------	----------

[Table 6]

	Other additives	Dummy	Phosphoric acid Content [wt%]	APST Content [wt%]	Solvent (water) Content [wt%]	(Before filtering) SIN (Å/min)	(Before filtering) TEOS (Å/min)	(After filtering) SIN (Å/min)	(After filtering) TEOS (Å/min)
Comparative Example 1	N-phosphoric acid	100	85	-	15	75.26	0.15	78.26	1.26
Comparative Example 9		1000	76.5	MTES 5	18.5	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Comparative Example 10			72.25	TEOS 7	20.75	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Comparative Example 11			79.9	APTMS 6	14.1	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Comparative Example 12			77.35	APTMS 9	13.65	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Comparative Example 9		1500	76.5	MTES 5	18.5	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Comparative Example 10			72.25	TEOS 7	20.75	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Comparative Example 11			79.9	APTMS 6	14.1	Measurement fail	Measurement fail	Measurement fail	Measurement fail
Comparative Example 12			77.35	APTMS 9	13.65	Measurement fail	Measurement fail	Measurement fail	Measurement fail

[144] Referring to Tables 3 to 6, regarding the etch rate and the etch selectivity of the

silicon oxide layer before and after filtering according to the Examples, as the concentration of the silicon ions was increased, the etch rates of the nitride layer and the oxide layer were reduced while the change in the etch rate before and after filtering was reduced. Specifically, it may be confirmed that the selectivity was maintained in the same level, even if the process
5 was performed until the concentration of the silicon ions became 1,500 ppm for the etching composition according to each of Examples.

[145] Meanwhile, it may be confirmed that the results of the measurement fail were shown under the condition that the concentration of the silicon ions ranged from 100 ppm to 500 ppm, even though a difference was slightly made depending on the type of additives, in
10 Comparative Examples 9 to 12 in which additives having a structure different from a structure according to the present disclosure were used in an amount similar to an amount according to the present disclosure. In addition, it may be confirmed that the etching composition contained the silanol-based compound in the content required according to the present disclosure, to exhibit the effect for suppressing the abnormal growth.

15 [146] It may be confirmed that the etching composition according to each of Examples 3 to 7 having the content of the silanol-based compound, which is in a specific level or more, among Examples of the present disclosure, exhibited a value of at most 0.1% in the change of selectivity before and after filtering, and the change in the etch rate of the nitride layer, even at the higher concentration of at least 10,00 ppm. In addition, it may be confirmed that the
20 absolute value of the change in the etch rate of the nitride layer showed at most 20% until the silicon ion was increased from 100 ppm to 1,500 ppm.

[147] **Experimental Example 3: Suppressing color change and particles of the etching composition**

[148] After performing the etching process using the etching composition according to
25 each of the Examples and the Comparative Examples, the effect for suppressing the color

change of the etching composition and the particles of the etching composition was analyzed.

The results are shown in following Table 7.

[Table 7]

	Phosphoric acid Content [wt%]	Type of additive	Additive Content [wt%]	Solvent (water) Content [wt%]	Color change	Production of particles
Example 1	84.575	CAS 68400-07-7	0.5	14.925	X	X
Example 2	84.15	CAS 68400-07-7	1	14.85	X	X
Example 3	82.025	CAS 68400-07-7	3.5	14.475	X	X
Example 4	80.75	CAS 68400-07-7	5	14.25	X	X
Example 5	79.475	CAS 68400-07-7	6.5	14.025	X	X
Example 6	78.2	CAS 68400-07-7	8	13.8	X	X
Example 7	76.925	CAS 68400-07-7	9.5	13.575	X	X
Comparative Example 1	85	-	-	15	X	O
Comparative Example 9	80.75	MTES	5	14.25	X	O
Comparative Example 10	79.05	TEOS	7	13.95	O	O
Comparative Example 11	79.9	APTMS	6	14.1	O	X
Comparative Example 12	77.35	APTMS	9	13.65	O	O

[149] Referring to Table 7, it may be confirmed that the color change and the production of
5 the particles were suppressed in all Examples.

[150] Meanwhile, in Comparative Example 1 in which the additive was not employed, or Comparative Examples 9 to 12 in which another type of additives was employed instead of the silanol-based compound, an inferior effect was exhibited in terms of at least one of a color change and the production of particles, as compared to the Examples.

5 [151] **Experimental Example 4: Analysis of production level of bubbles of etching composition**

[152] The production level of bubbles of an etching composition was confirmed through a Bubble pour manner. The flow was performed with N₂ [0.5 L/min]. The etching composition was formed and then contained in a vessel, and the height of the bubbles was measured.

10 Thereafter, after 60 seconds, the height of bubbles were measured after the bubbles were collapsed, thereby measuring the characteristics of the bubbles. The results are shown in following Table 8.

[Table 8]

	Phosphoric acid Content [wt%]	Type of additive	Additive Content [wt%]	Solvent (water) Content [wt%]	Bubble height (cm) After forming	Bubble height (cm) After 60 seconds
Example 1	84.575	CAS 68400-07-7	0.5	14.925	0.1	0
Example 2	84.15	CAS 68400-07-7	1	14.85	0.1	0
Example 3	82.025	CAS 68400-07-7	3.5	14.475	0.2	0
Example 4	80.75	CAS 68400-07-7	5	14.25	0.2	0
Example 5	79.475	CAS 68400-07-7	6.5	14.025	0.2	0
Example 6	78.2	CAS 68400-07-7	8	13.8	0.2	0
Example 7	76.925	CAS 68400-07-7	9.5	13.575	0.2	0
Comparative Example 1	85	-	-	15	0	0

Comparative Example 9	80.75	MTES	5	14.25	7	0
Comparative Example 10	79.05	TEOS	7	13.95	5	0
Comparative Example 11	79.9	APTMS	6	14.1	10	0.5
Comparative Example 12	77.35	APTMS	9	13.65	12	0.7

[153] Referring to Table 8, it may be confirmed that the etching composition according to each of Examples 1 to 5 containing the silanol-based compound according to the present disclosure hardly showed the production of bubbles even immediately after the etching composition was prepared as in Comparative Example 1 containing only a phosphoric acid aqueous solution.

[154] Meanwhile, in Comparative Examples 9 to 12 employing other types of additives instead of a silanol-based compound used in the etching composition according to the present disclosure, a significantly large amount of bubbles was produced, as compared to the etching compositions according to the Examples.

[155] This refers to that the present disclosure solved the bubble production issues caused in the etching composition containing the typical silicon additives at an initial stage for forming the etching composition or in a procedure for transferring the etching composition before the etching composition was introduced into the preparation process. Such bubbles may lower the efficiency of the etching process or cause the damage to the etching equipment. Accordingly, the etching composition should be formed without producing bubbles from the stage for forming the etching composition.

[156] The above description has been made only for the illustrative purpose, and those

skilled in the art should understand that various modifications are possible without departing from the technical scope of the present disclosure or without changing the subject matter of the present disclosure. Therefore, those skilled in the art should understand that the technical examples are provided for the illustrative purpose in all aspects and the present disclosure is
5 not limited thereto. For example, components described in a singular form may be reproduced while being distributed. Similarly, components described in a distribution form may be reproduced in a combination form.

[157] The scope of the present disclosure falls into the scope of the appended claims instead of the detailed description, those skilled in the art should interpret that all variations
10 or modifications derived from the meaning and the range of claims, and equivalents of the claims are included in the scope of the present disclosure.

【CLAIMS】

【Claim 1】 An etching composition comprising:

an inorganic acid;

a silanol-based compound; and

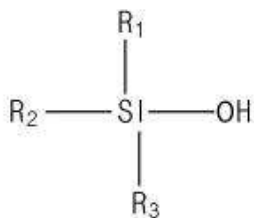
5 a solvent as a remainder,

wherein a content of the silanol-based compound ranges from 0.1 parts by weight to less than 10 parts by weight, based on a total weight of the etching composition, and

wherein an APHA value is less than 1.5.

10 **【Claim 2】** The etching composition of claim 1, wherein the silanol-based compound is a silanol-based compound represented by following Chemical Formula 1 or a condensate of the silanol-based compound.

[Chemical Formula 1]



in which, in Chemical Formula 1,

15 R_1 is selected from the group consisting of an aminoalkyl group having 1 to 20 carbon atoms, an alkoxy group having 1 to 20 carbon atoms, an acetyloxy group, and a haloalkyl acetyloxy group having 1 to 20 carbon atoms, and R_2 and R_3 are hydroxy groups.

【Claim 3】 The etching composition of claim 1, wherein the silanol-based compound is
20 3-aminopropylsilanetriol or a condensate of the silanol-based compound.

【Claim 4】 The etching composition of claim 1, wherein a CAS number of the silanol-based compound is 68400-07-7.

【Claim 5】 The etching composition of claim 1, wherein the inorganic acid ranges from 50 parts by weight to 85 parts by weight, based on 100 parts by weight of a whole etching composition.

【Claim 6】 The etching composition of claim 1, wherein the inorganic acid includes:
at least one selected from the group consisting of sulfuric acid, nitric acid,
phosphoric acid, silicic acid, hydrofluoric acid, boric acid, hydrochloric acid, and perchloric acid.

【Claim 7】 The etching composition of claim 1, wherein the etching composition further includes:
an ammonium-based compound.

【Claim 8】 The etching composition of claim 7, wherein the ammonium-based compound includes:
at least one selected from the group consisting of ammonium chloride, ammonium phosphate, ammonium acetate, ammonium sulfate, ammonium formate, and a metal amine complex salt.

【Claim 9】 The etching composition of claim 1, wherein the etching composition is used to etch a silicon nitride layer.

【Claim 10】 The etching composition of claim 1, wherein an etch selectivity of a silicon nitride layer over a silicon oxide layer of the etching composition is at least 30.

5 【Claim 11】 The etching composition of claim 1, wherein an absolute value of variation of an etch rate of the nitride layer is at most 20% while the etching process is performed until a silicon ion is in a range from 100 ppm to 1,500 ppm.

10 【Claim 12】 The etching composition of claim 1, wherein a height of bubbles on a surface of the etching composition is at most 0.5 cm, immediately after the etching composition is formed.

【Claim 13】 The etching composition of claim 1, wherein an etch rate of the silicon nitride layer ranges from 40 to 80 Å/min at an etching process temperature of 165°C.

15 【Claim 14】 The etching composition of claim 1, wherein an etch rate of the silicon oxide layer is 1 Å/min at an etching process temperature of 165°C.

20 【Claim 15】 A method for manufacturing a semiconductor device, the method comprising:
forming a structure by stacking an insulating layer and a sacrificial layer on a substrate; and

forming a space region by performing an etching process using the etching composition according to Claim 1 to remove the sacrificial layer.

25 【Claim 16】 The method of claim 15, wherein the sacrificial layer includes:
a silicon nitride, and

wherein the insulating layer includes:

a silicon oxide layer.

5 **【Claim 17】** The method of claim 15, wherein the sacrificial layer has an etch rate higher than an etch rate of the insulating layer, in the etching process.

【Claim 18】 The method of claim 15, wherein the space region includes:

a gate region interposed between insulating layers and a trench connected to the gate region.

10

【Claim 19】 The method of claim 18, further comprising:

forming openings formed through the stack structure; and

forming a semiconductor pattern spaced apart from the trench in the openings,

wherein the forming of the semiconductor pattern is performed before forming the

15 trench.