CLAIMS

1. A standard cell template, comprising:

a first well region and a second well region, arranged along a first direction;

a first gate pattern, located in the first well region and extending along the first direction, and configured for defining a first gate;

a second gate pattern, located in the second well region and extending along the first direction, and configured for defining a second gate; and

a gate electrical connection pattern, located between the first gate pattern and the second gate pattern, and configured for defining a gate electrical connection structure; wherein the gate electrical connection structure is arranged on the same layer as the first gate and the second gate, to electrically connect the first gate and/or the second gate;

wherein the gate electrical connection pattern comprises:

at least two electrical connection patterns which are arranged at interval; each of the electrical connection patterns extends along a second direction, the second direction is different from the first direction, and each of the electrical connection patterns is configured to define an electrical connection structure.

2. The standard cell template according to claim 1, wherein the at least two electrical connection patterns which are arranged at interval comprises:

a first electrical connection pattern, located in the first well region, and configured for defining a first electrical connection structure to electrically connect the first gate; and

a second electrical connection pattern, located in the second well region, and configured for defining a second electrical connection structure to electrically connect the second gate.

3. The standard cell template according to claim 1, wherein the gate electrical connection pattern further comprises:

a first auxiliary pattern, connecting the first gate pattern and an electrical connection pattern facing toward the first gate pattern, and configured for defining a first auxiliary electrical connection structure to electrically connect the first gate and the electrical connection structure facing toward the first gate; and

a second auxiliary pattern, connecting the second gate pattern and an electrical connection pattern facing toward the second gate pattern, and configured for defining a second auxiliary electrical connection structure to electrically connect the second gate and the electrical connection structure facing toward the second gate.

4. The standard cell template according to claim 1, wherein the gate electrical connection pattern further comprises:

a third auxiliary pattern, located between adjacent electrical connection patterns, and configured for defining a third auxiliary electrical connection structure to electrically connect the adjacent electrical connection structures.

5. The standard cell template according to claim 1, wherein the gate electrical connection pattern is further located on a side of the first gate pattern away from the second gate pattern and on a side of the second gate pattern away from the first gate pattern.

6. The standard cell template according to claim 1, further comprising:

a metal layer pattern, wherein the metal layer pattern spans the gate electrical connection pattern, the first gate pattern and/or the second gate pattern, and is configured for defining a metal layer; and the metal layer is located on an upper layer of the first gate and an upper layer of the second gate, to electrically connect the first gate and/or the second gate.

7. The standard cell template according to claim 1, wherein the first well region comprises a first metal oxide semiconductor (MOS) region, and the first gate pattern spans the first MOS region;

the second well region comprises a second MOS region, and the second gate pattern spans the second MOS region; and

the standard cell template further comprises an intermediate region, the intermediate region is located between the first MOS region and the second MOS region, wherein the gate electrical connection pattern is located in the intermediate region.

8. The standard cell template according to claim 7, wherein the first well region has a first

boundary facing toward the second well region, and the first boundary is located in a middle of the intermediate region.

9. The standard cell template according to claim 1, further comprising:

a first power pattern, configured for defining a first power line, the first power line being configured to connect a first power supply; and

a second power pattern, configured for defining a second power line, the second power line being configured to connect a second power supply, wherein a voltage of the first power supply is greater than a voltage of the second power supply;

wherein, in the first direction, a width of the first power pattern is greater than a width of the second power pattern.

10. The standard cell template according to claim 1, further comprising:

a power pattern, configured for defining a power line, the power line being configured to connect a power supply;

a signal pattern, configured for defining a signal line, the signal line being configured to connect a signal;

a first gating pattern, configured for defining a first gating switch, the first gating switch being configured for electrical connection or disconnection of the power line; and

a second gating pattern, configured for defining a second gating switch, the second gating switch being configured for electrical connection or disconnection of the signal line;

wherein the signal pattern, the first gating pattern, and the second gating pattern are located on the same side of the power pattern.

11. A semiconductor structure, comprising:

a substrate, wherein the substrate is provided with a first well and a second well, the first well and the second well are arranged along a first direction;

a first gate, located on the substrate where the first well is located, and extending along the first direction;

a second gate, located on the substrate where the second well is located, and extending along

the first direction; and

a gate electrical connection structure, located on the substrate, and arranged on the same layer as the first gate and the second gate to electrically connect the first gate and/or the second gate;

wherein the gate electrical connection structure comprises:

at least two electrical connection structures, wherein each of the electrical connection structures extends along a second direction, the second direction is different from the first direction.

12. The semiconductor structure according to claim 11, wherein the at least two electrical connection structures comprise:

a first electrical connection structure, located on the substrate where the first well is located; and

a second electrical connection structure, located on the substrate where the second well is located.

13. The semiconductor structure according to claim 11, wherein the gate electrical connection structure further comprises:

a first auxiliary electrical connection structure, located between the first gate and an electrical connection structure facing toward the first gate to electrically connect the first gate and the electrical connection structure facing toward the first gate; and

a second auxiliary electrical connection structure, located between the second gate and an electrical connection structure facing toward the second gate to electrically connect the second gate and the electrical connection structure facing toward the second gate.

14. The semiconductor structure according to claim 11, wherein the gate electrical connection structure further comprises: a third auxiliary electrical connection structure, located between adjacent electrical connection structures to electrically connect the adjacent electrical connection structures.