ABSTRACT

SELF-INTEGRATED VERTICAL MIM CAPACITOR IN THE DUAL DAMASCENE PROCESS

A method for fabricating an increased capacitance metal-insulator-metal capacitor using an integrated copper dual damascene process is described. A first dual damascene opening and a pair of second dual damascene openings are provided in a first dielectric layer overlying a substrate. The first and second dual damascene openings are filled with a first copper layer wherein the filled first dual damascene opening forms a logic interconnect and the filled pair of second dual damascene openings forms a pair of capacitor electrodes. The first dielectric layer is etched away between the pair of capacitor electrodes leaving a space between the pair of capacitor electrodes. The space between the pair of capacitor electrodes is filled with a high dielectric constant material to complete fabrication of a vertical MIM capacitor in the fabrication of an integrated circuit device. The fabrication of the capacitor can begin at any metal layer. The process of the invention can be extended to form a parallel capacitor, a series capacitor, stacked capacitors, and so on.

FIGURE 15