GATE ELECTRODE FOR A SEMICONDUCTOR FIN DEVICE

A method for forming a gate electrode for a multiple gate transistor provides a doped, planarized gate electrode material which may be patterned using conventional methods to produce a gate electrode that straddles the active area of the multiple gate transistor and has a constant transistor gate length. The method includes forming a layer of gate electrode material having a non-planar top surface, over a semiconductor fin. The method further includes planarizing and doping the gate electrode material, without doping the source/drain active areas, then patterning the gate electrode material. Planarization of the gate electrode material may take place prior to the introduction and activation of dopant impurities or it may follow the introduction and activation of dopant impurities. After the gate electrode is patterned, dopant impurities are selectively introduced to the semiconductor fin to form source/drain regions.

(FIG. 4)