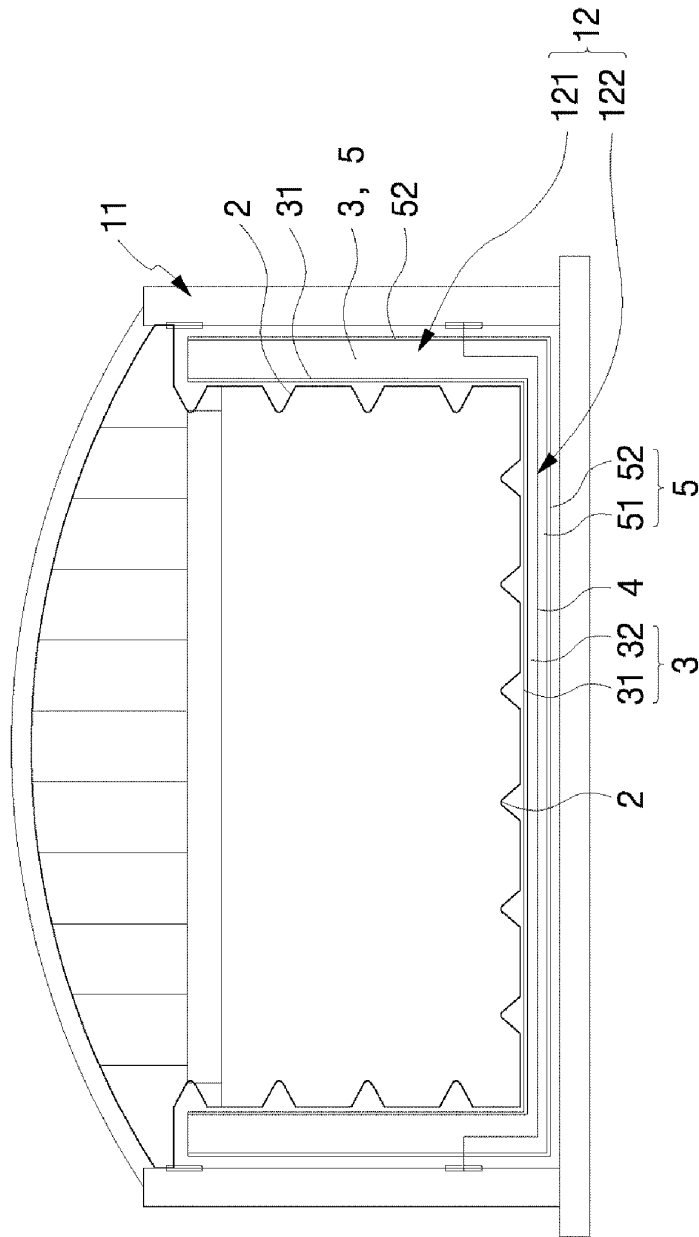
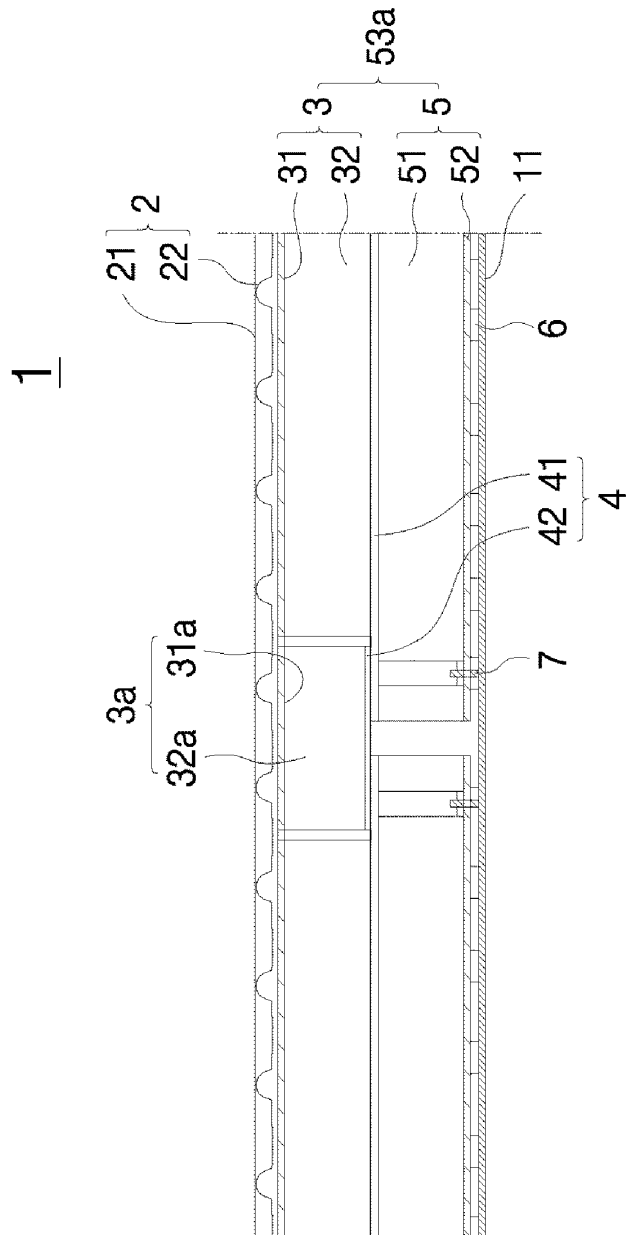


[圖1]

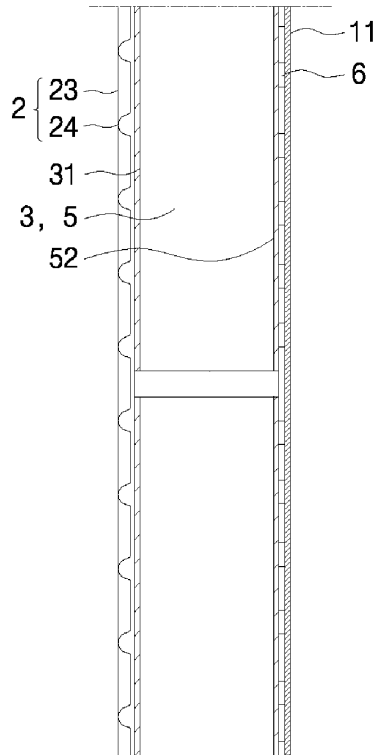
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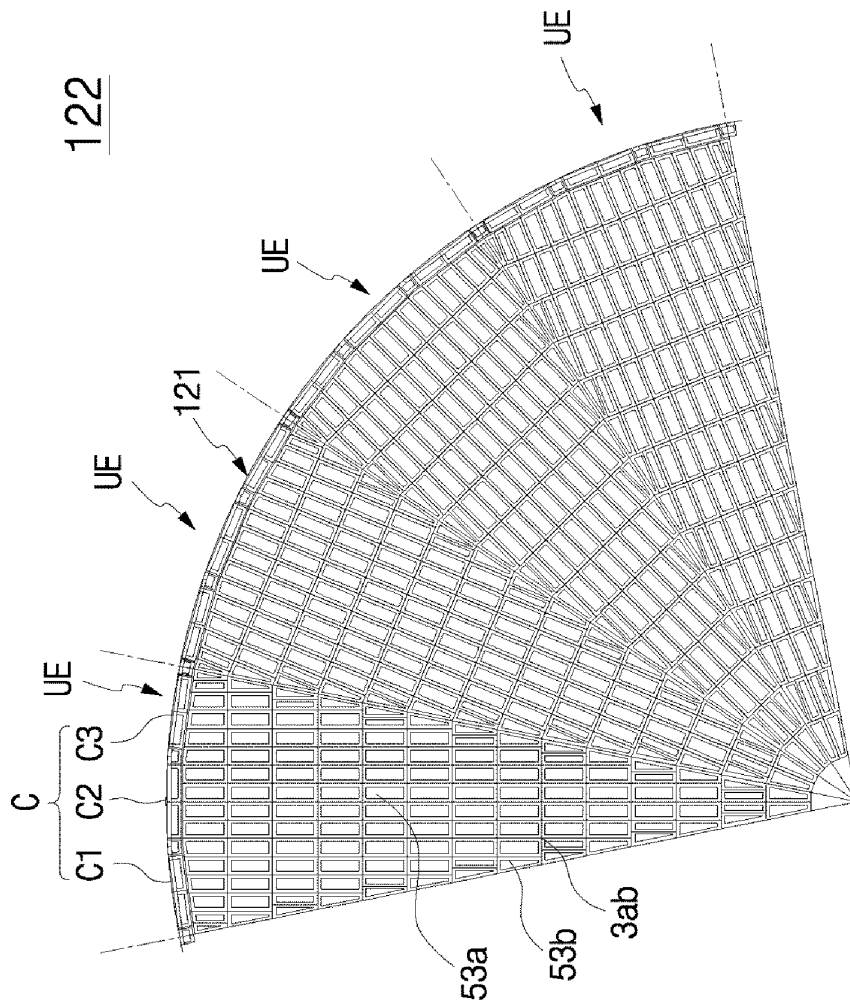
[도2]



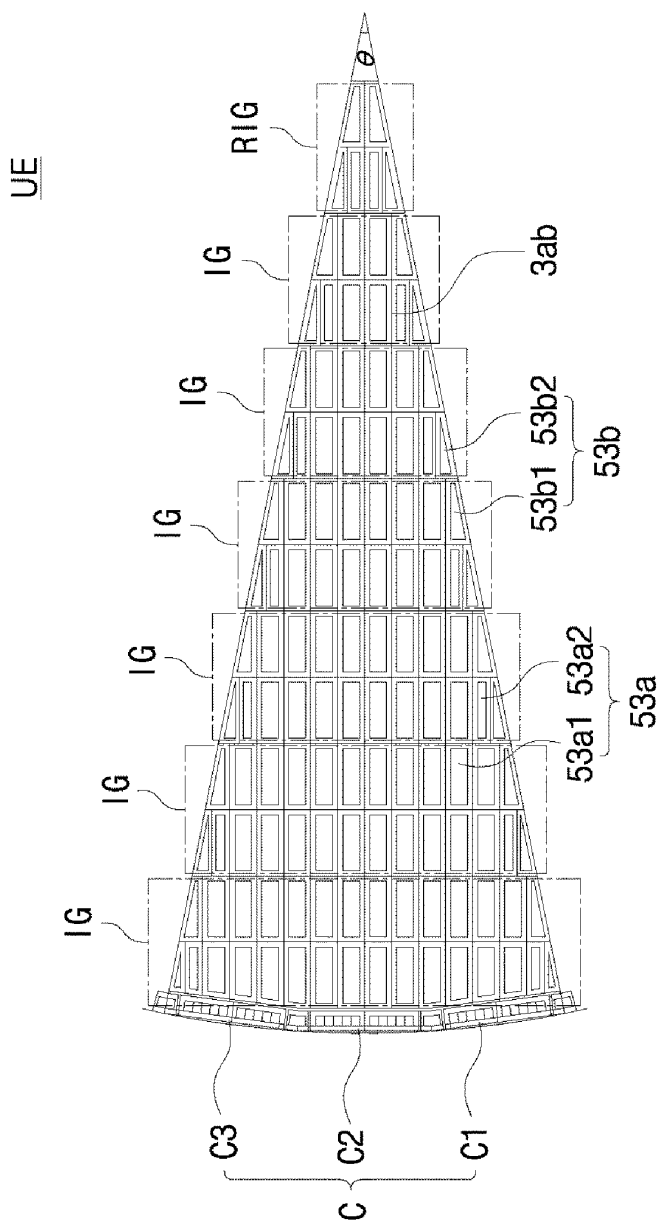
[도3]

1

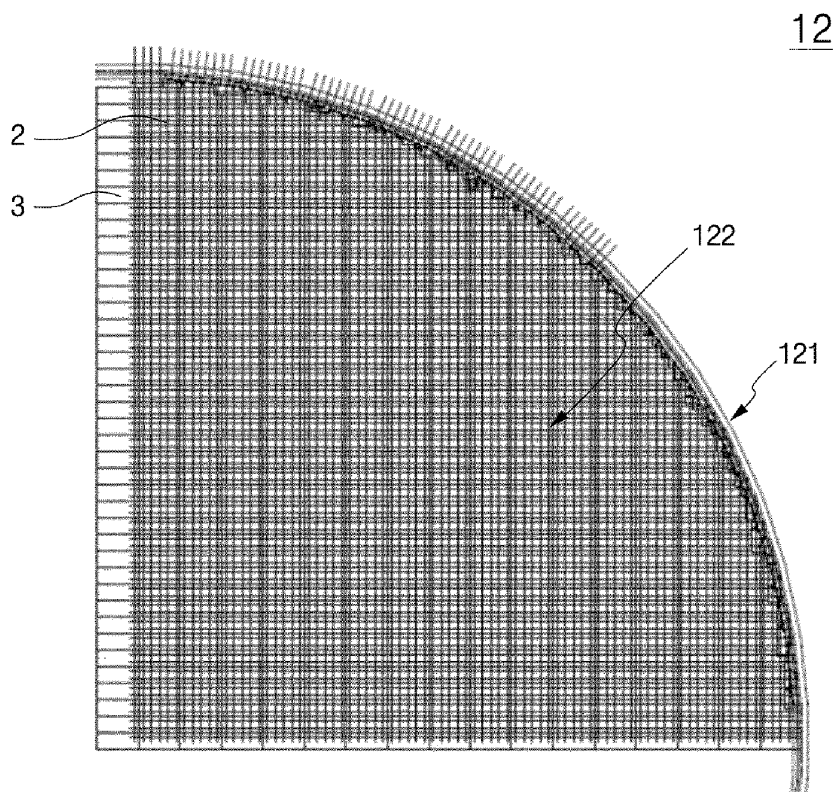
[도4]



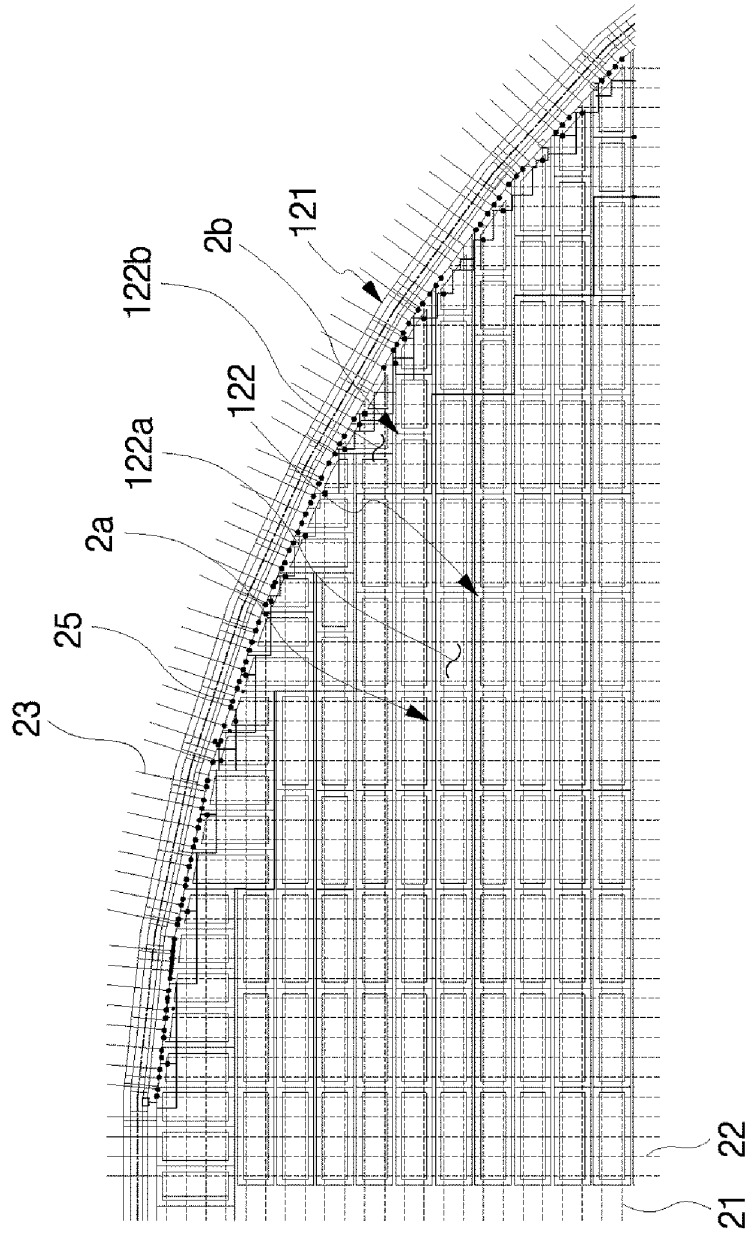
[E5]



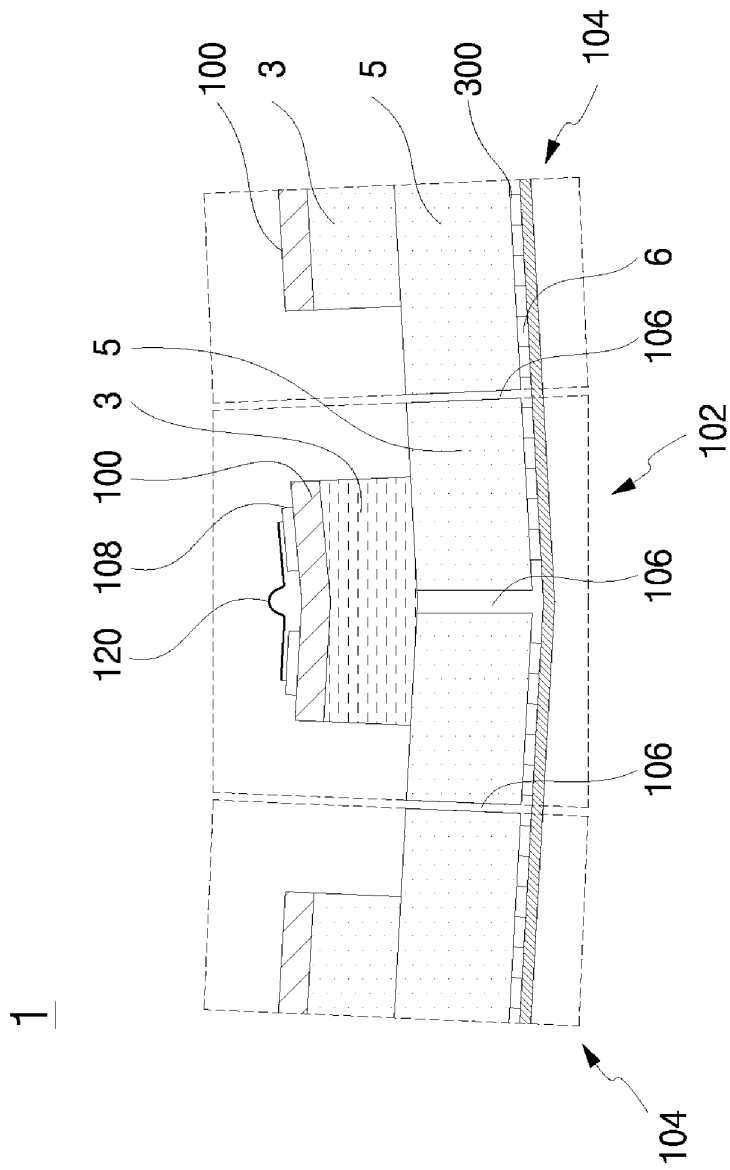
[도6]



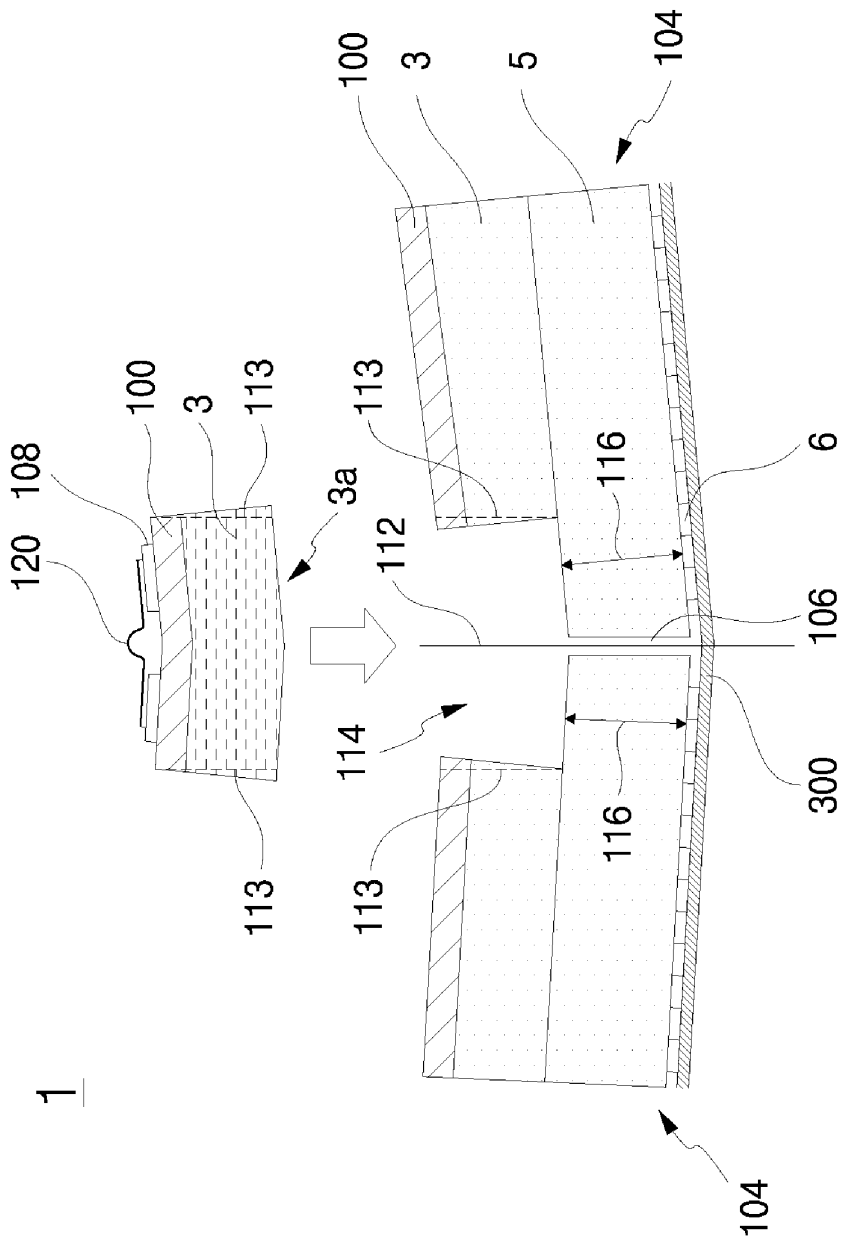
[도7]

12

[도8]

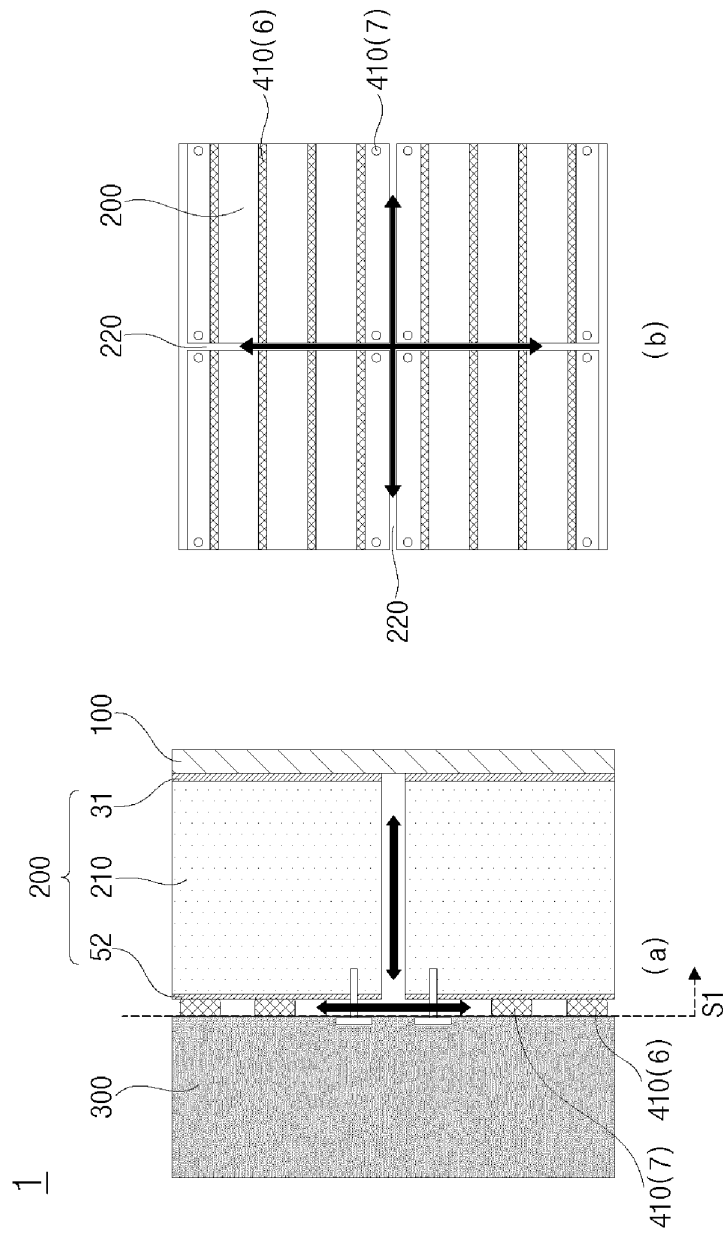


[도9]

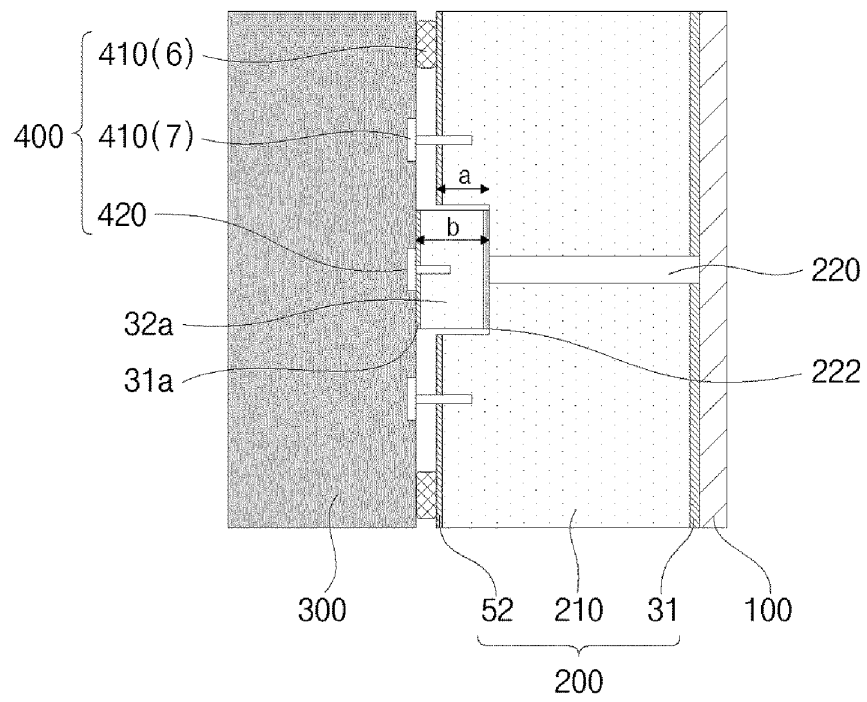




[도11]

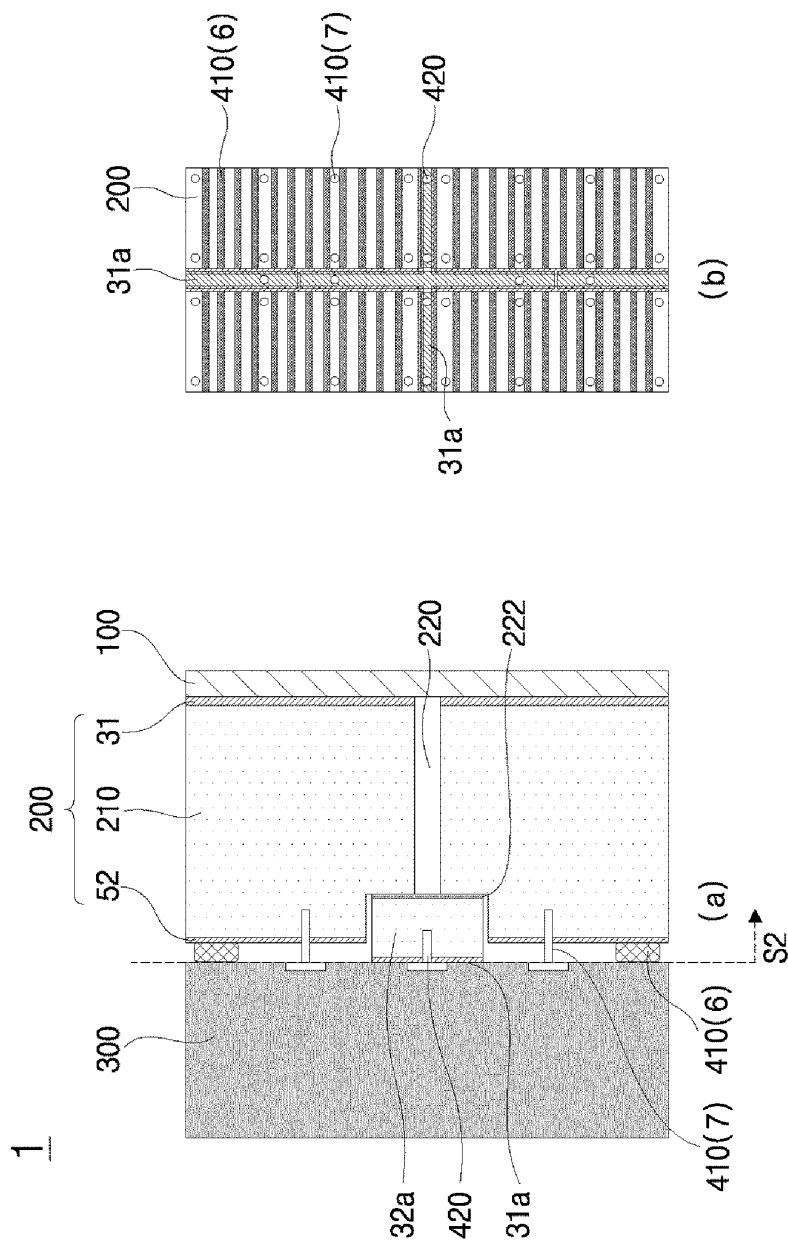


[도12]

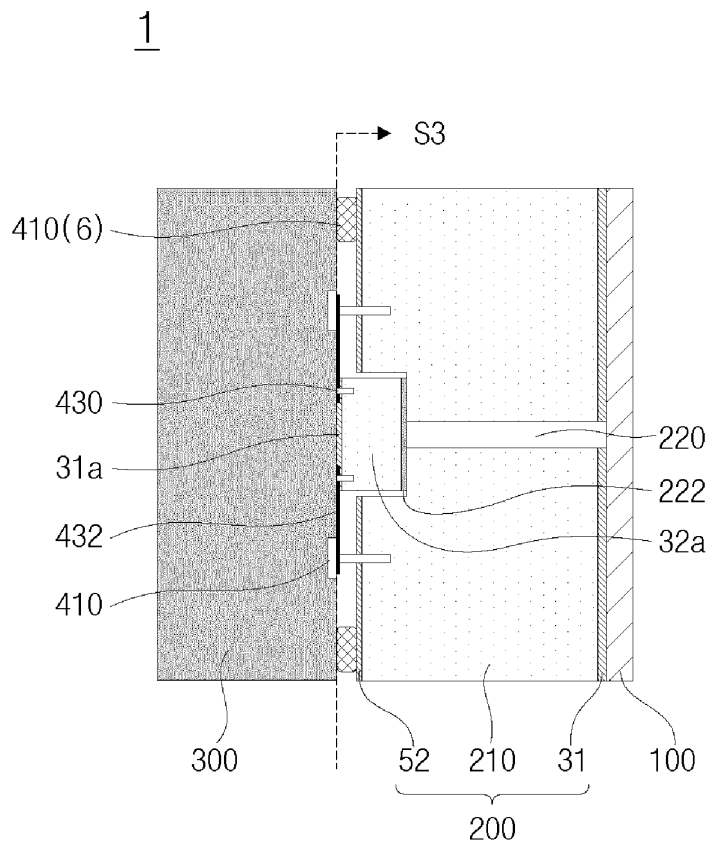




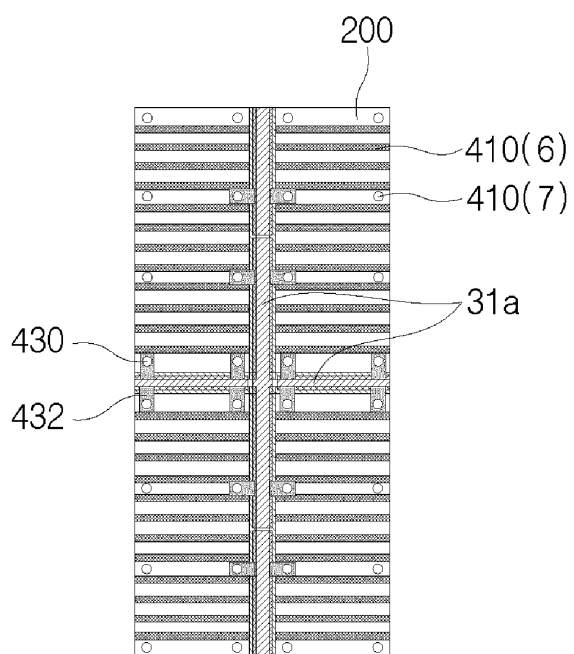
[도14]



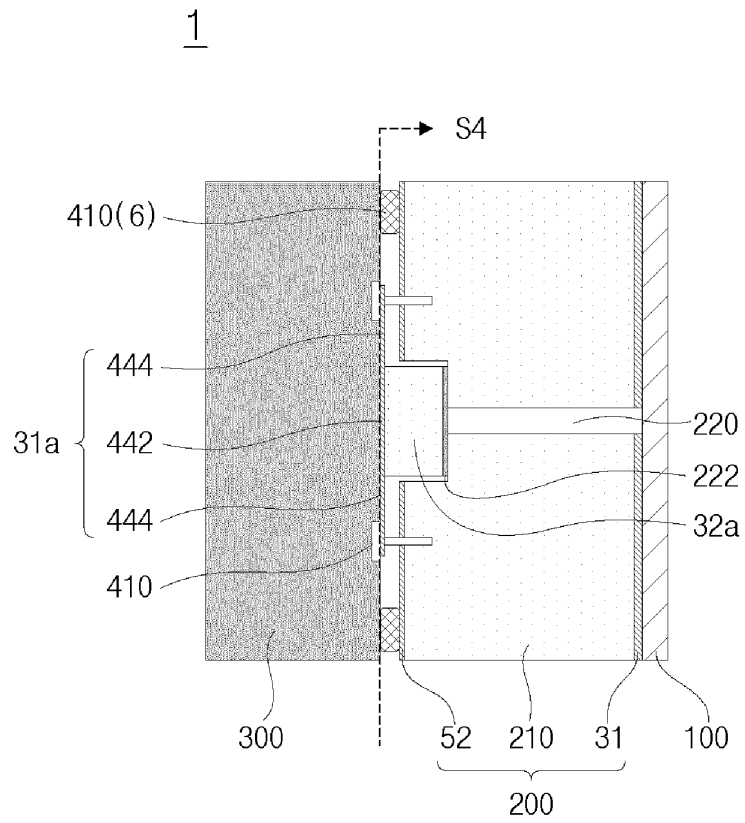
[도15]



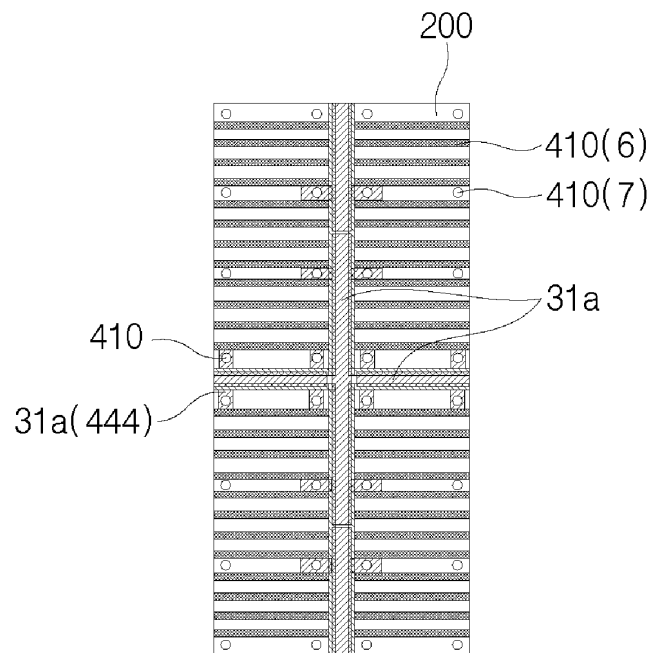
[도16]



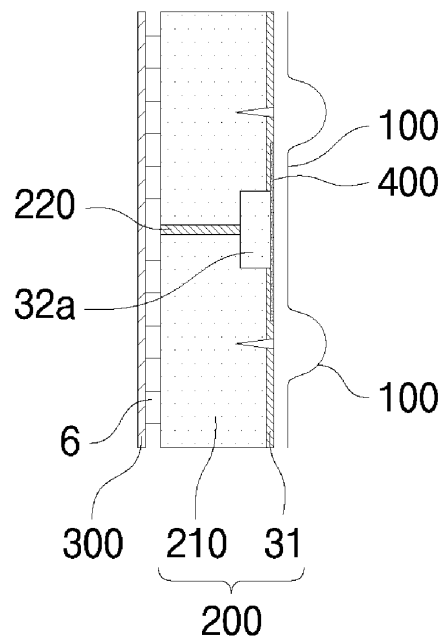
[도17]



[도18]

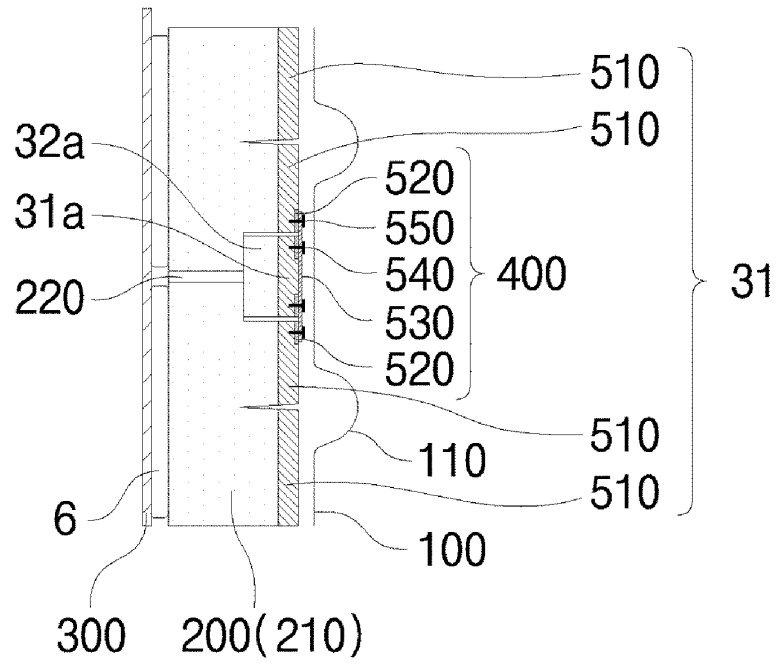


[도19]

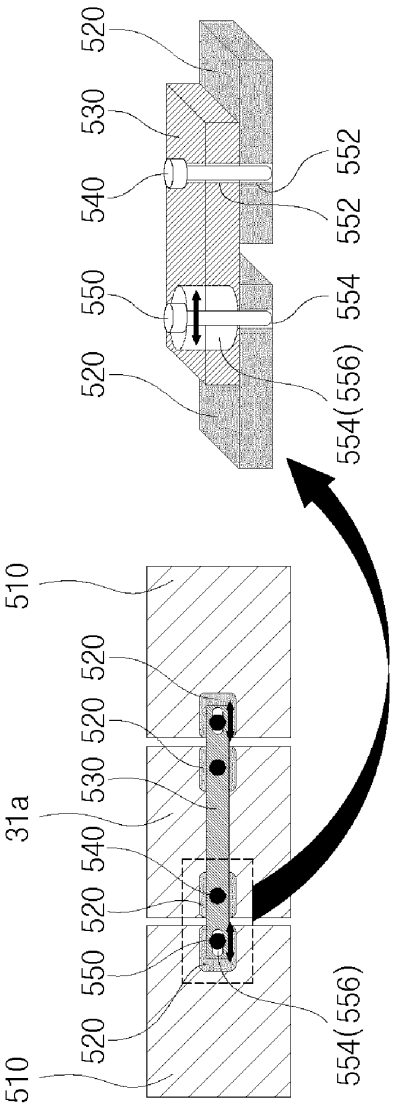
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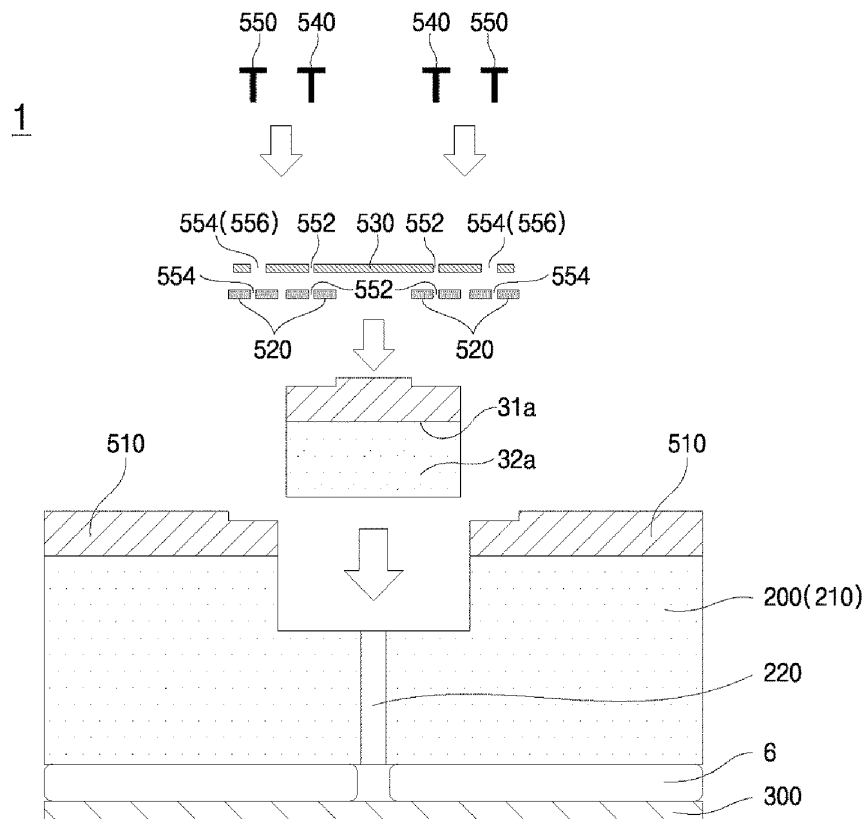
[도21]

1

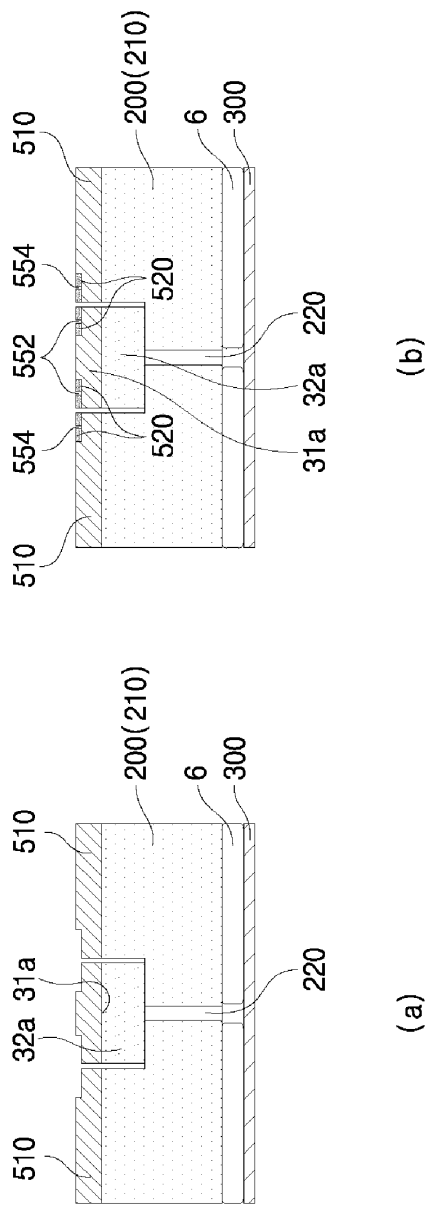
[도22]



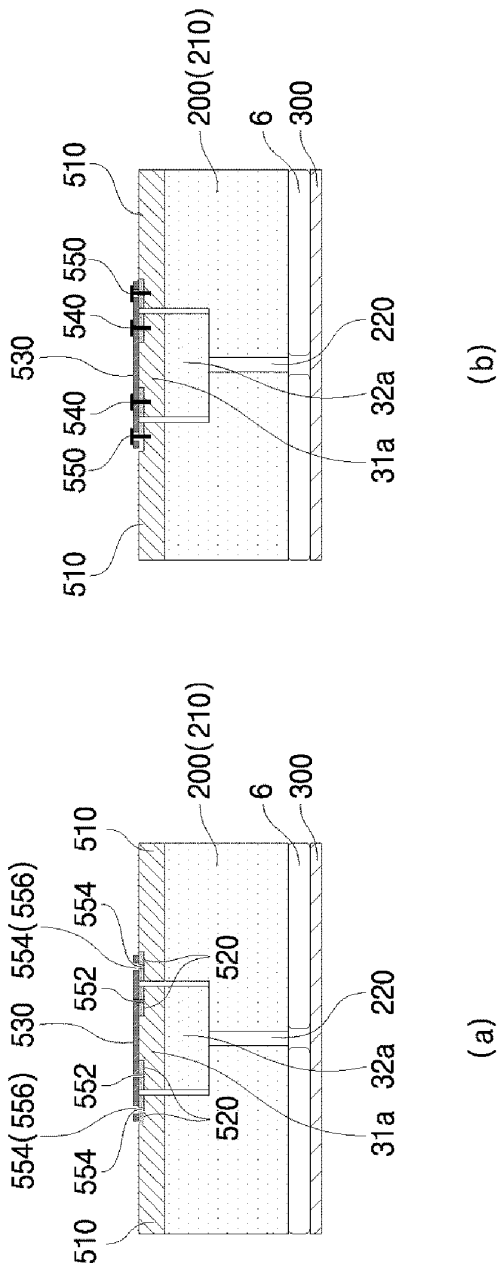
[도 23]



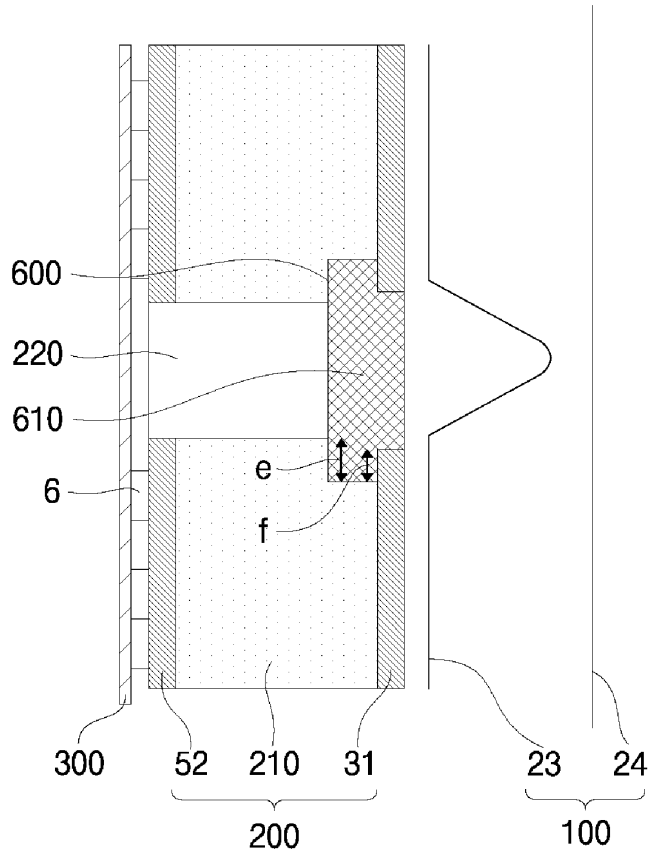
[도 24]



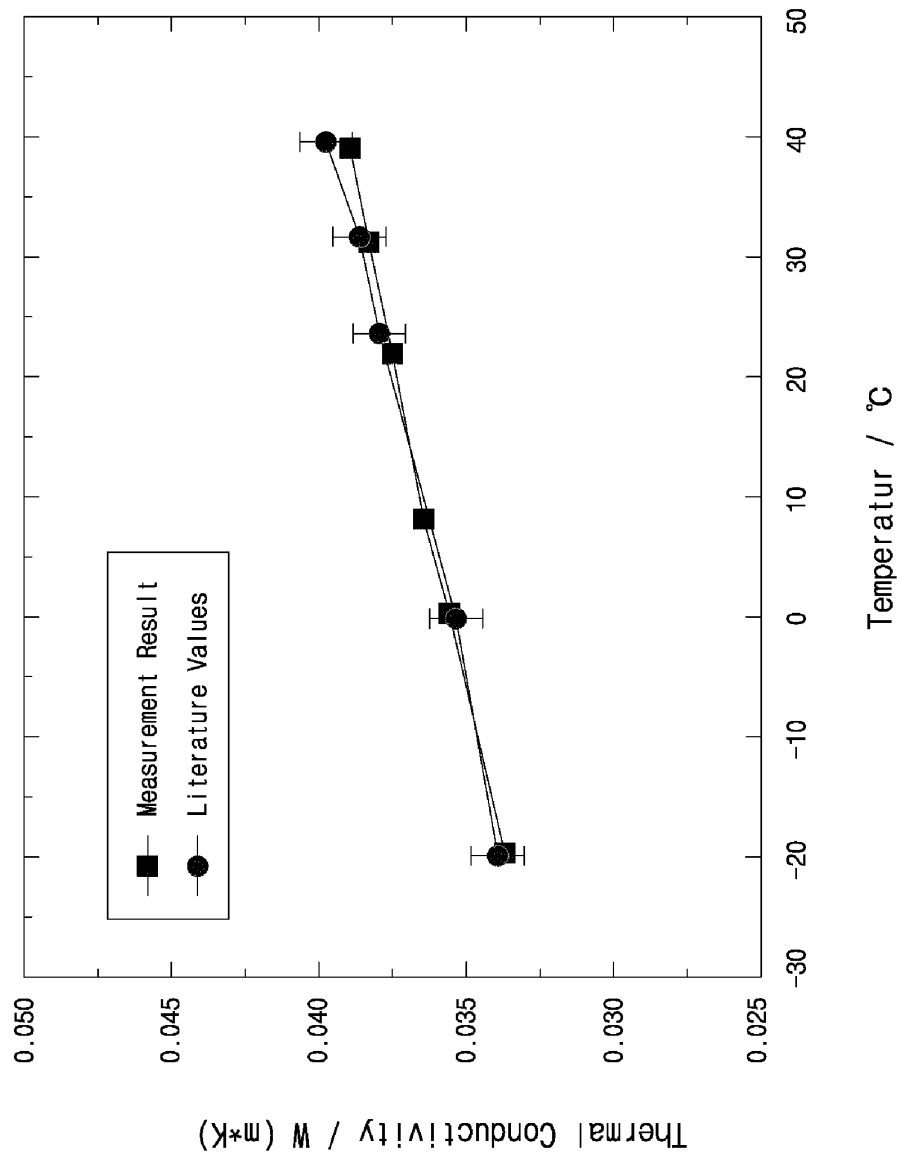
[도 25]



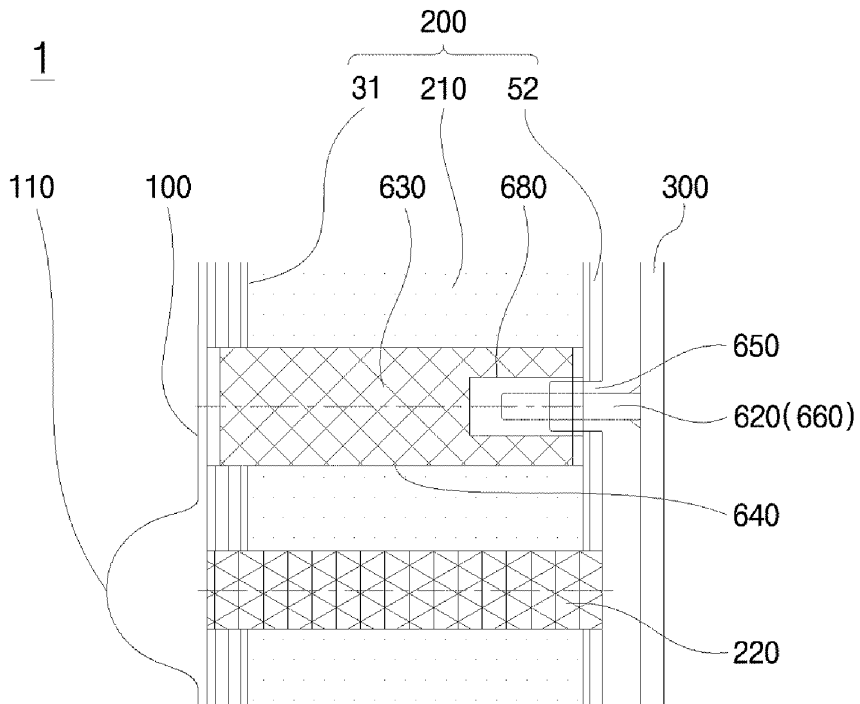
[도26]

1

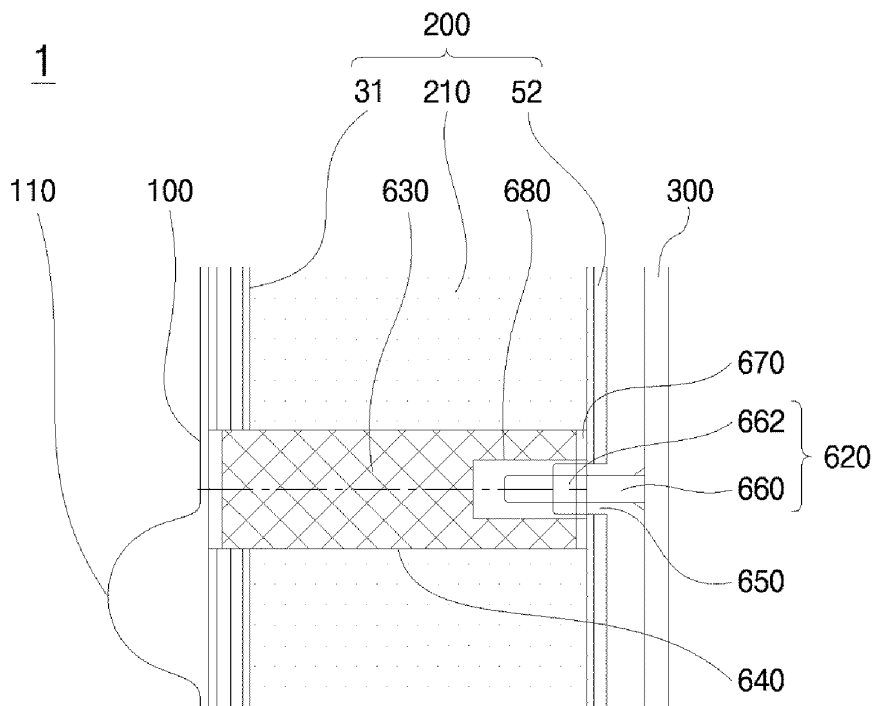
[도27]



[도28]



[도29]



[도30]

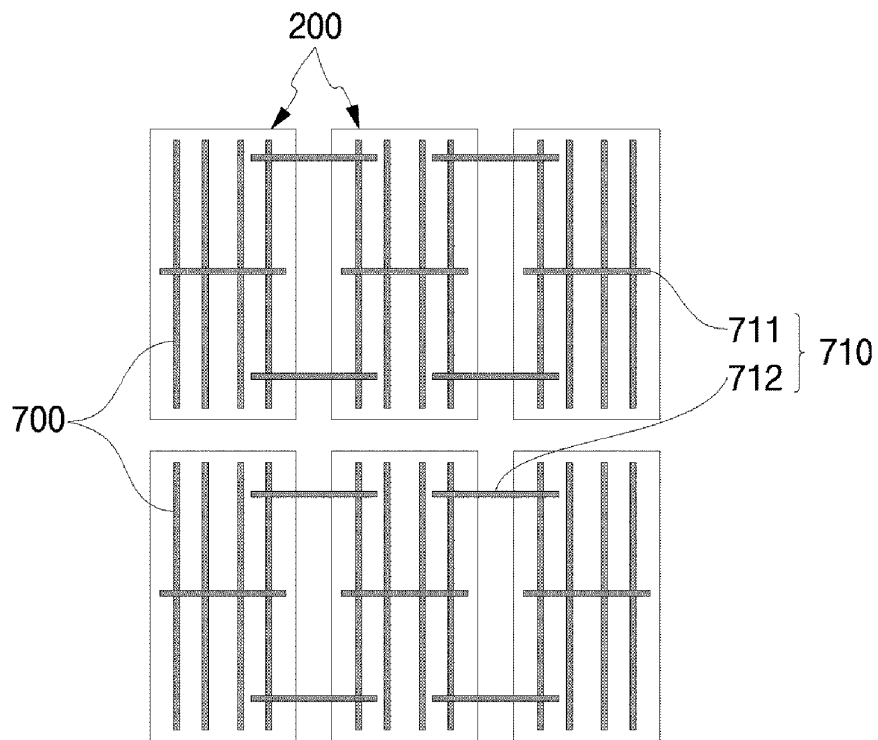
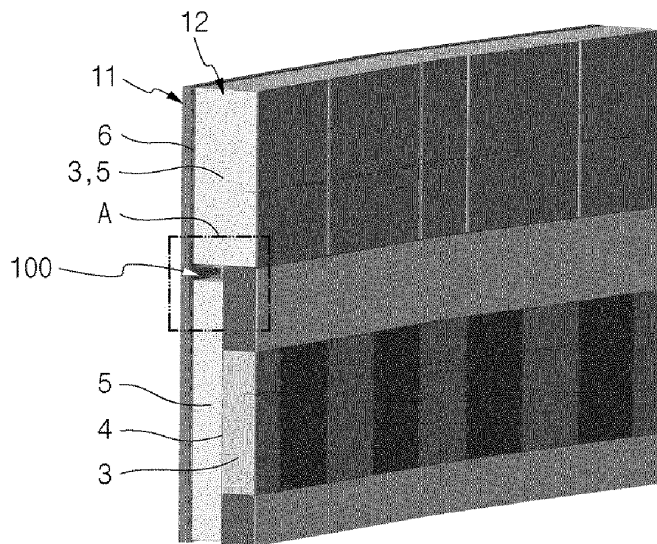
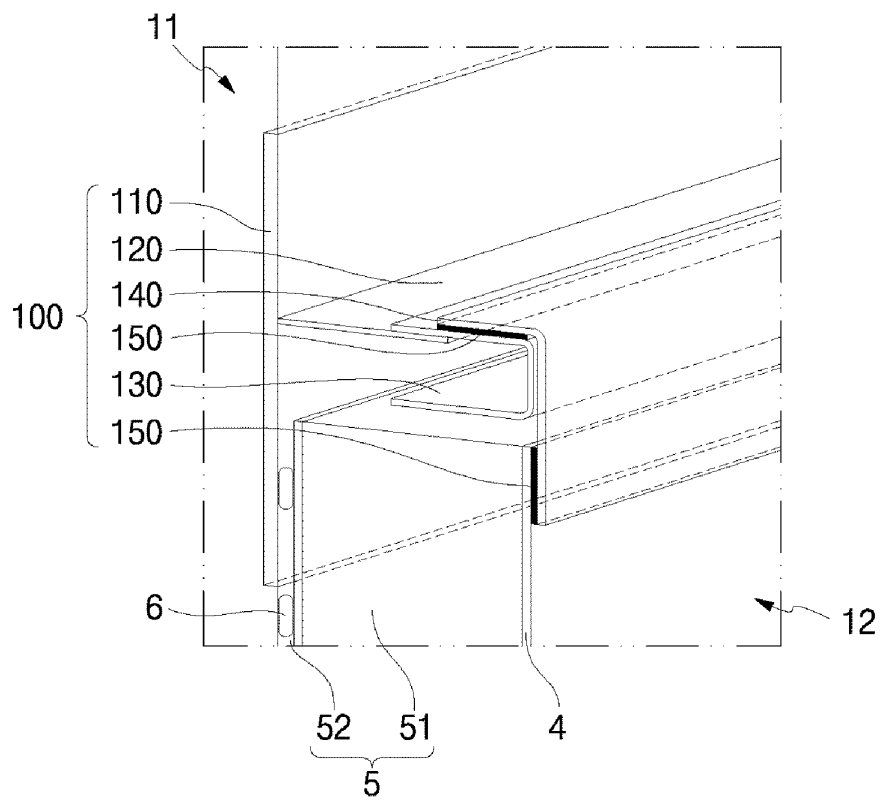


Fig. 1 consists of two cross-sectional views, (a) and (b), of a semiconductor device. Both views show a substrate 100 with a series of wavy lines representing a surface. Above the substrate, there are several layers: a first layer 23, a second layer 24, a third layer 31, a fourth layer 210, a fifth layer 52, and a sixth layer 300. A central region 800 contains a structure 810. In view (a), structure 810 has a top layer 820 and a bottom layer 220. A side layer SP is also shown. In view (b), the structure 810 is different, with a top layer 820 and a bottom layer 220, but the side layer SP is not present. The layers are labeled with numbers 1, 23, 24, 31, 210, 52, 300, 800, 810, 820, and 220. The labels 1, 23, 24, 31, 210, 52, and 300 are grouped together with a bracket labeled 100. The labels 800, 810, 820, and 220 are grouped together with a bracket labeled 1.

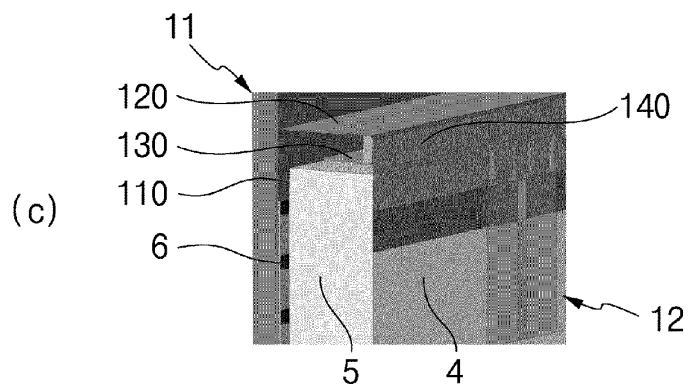
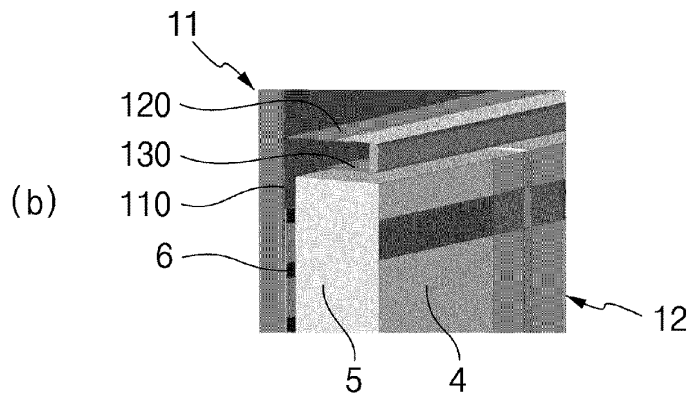
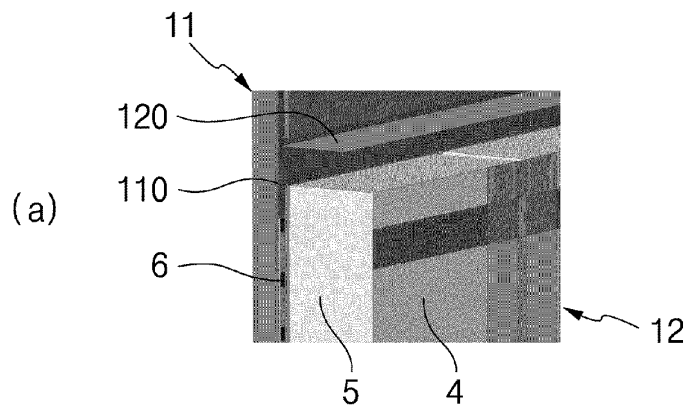
[도32]

1

[도33]

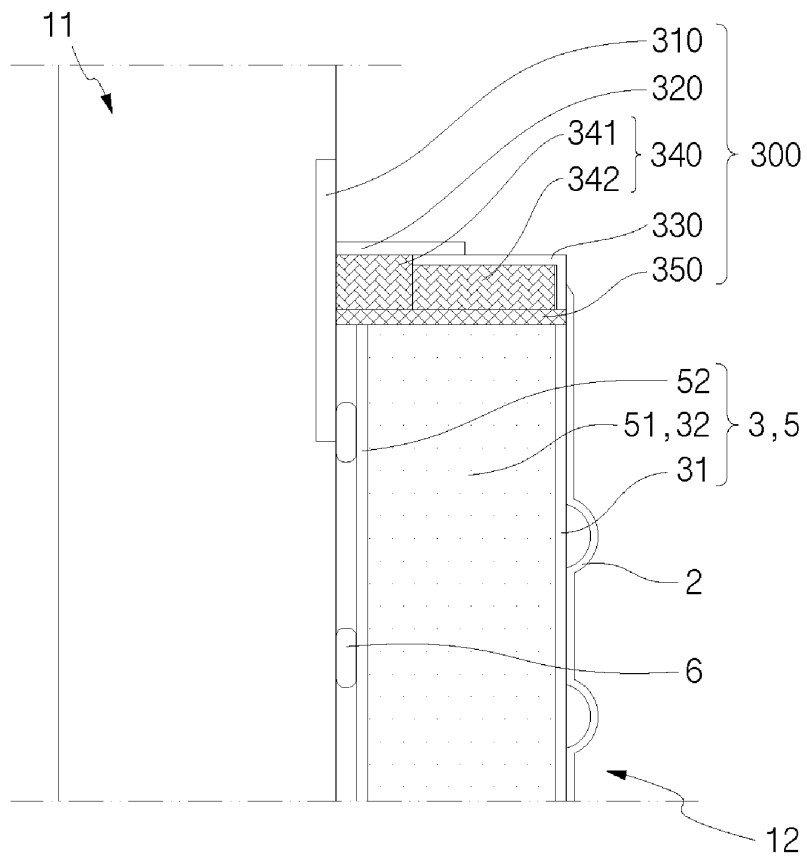


[도34]

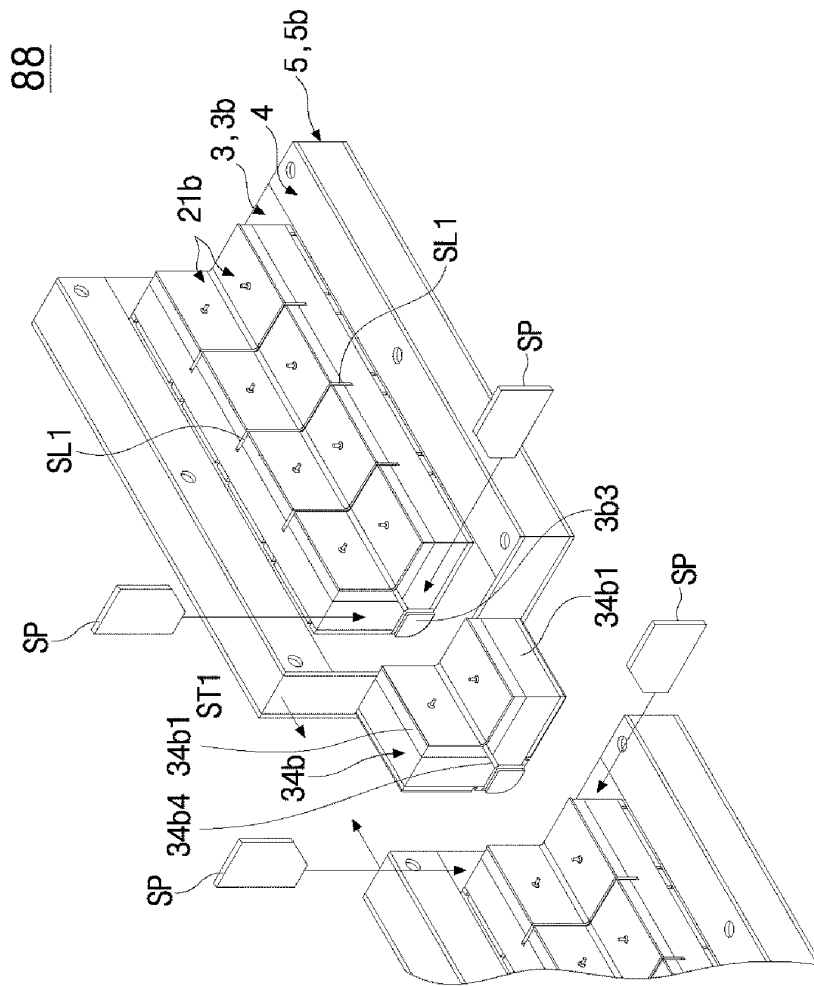




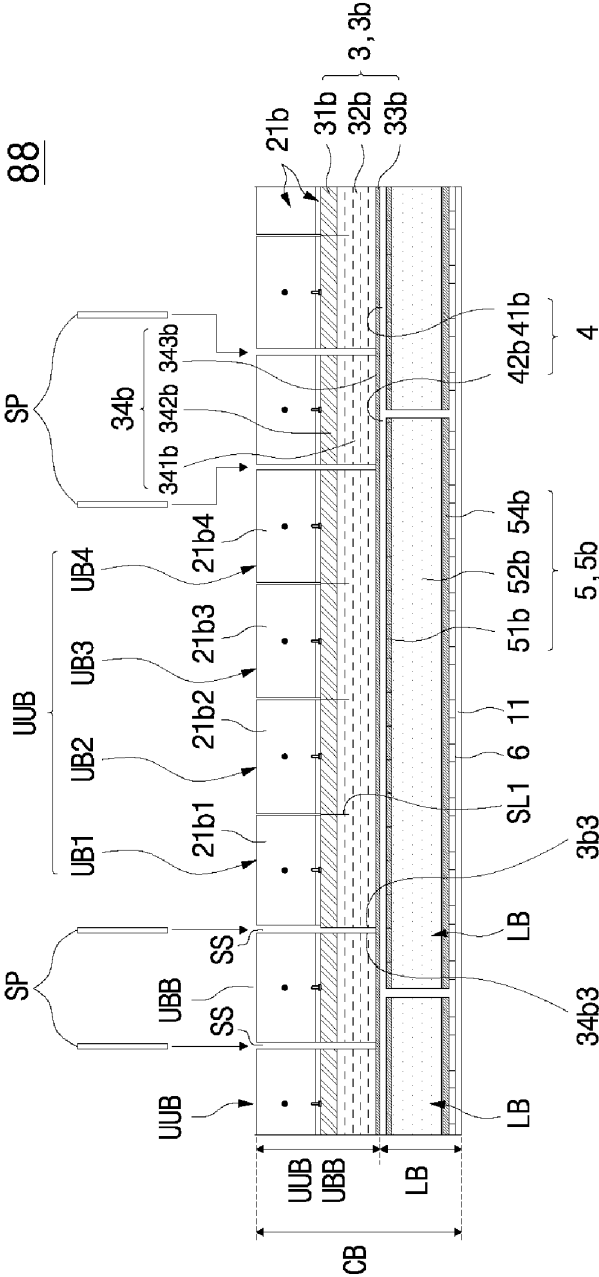
[도36]



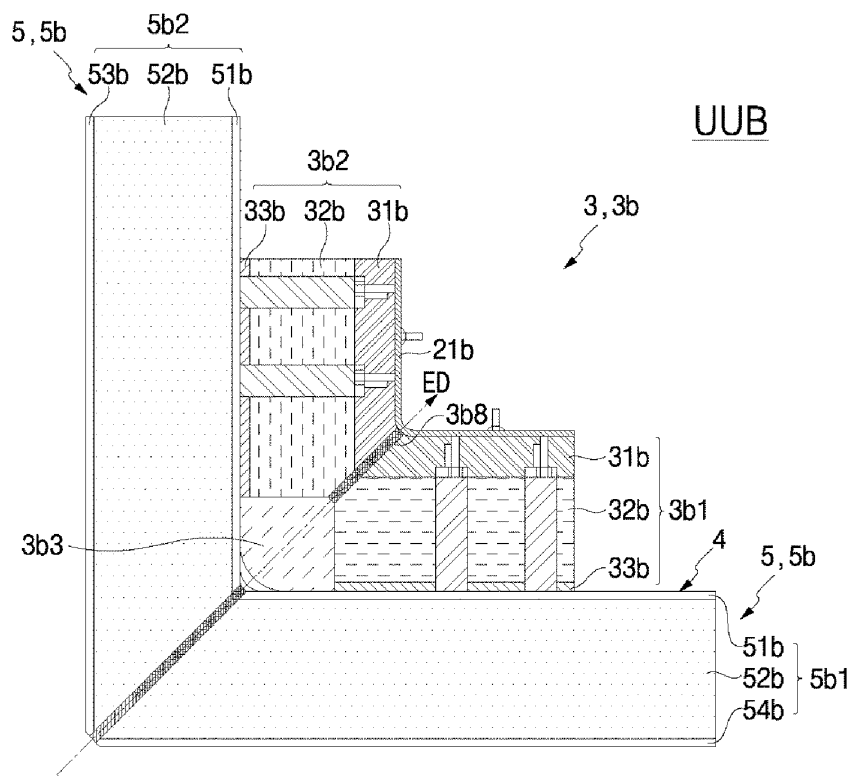
[도37]



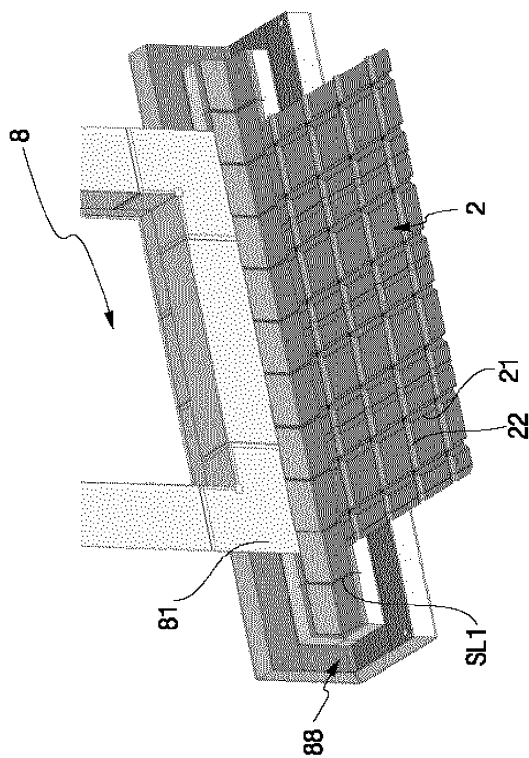
[도38]



[도39]

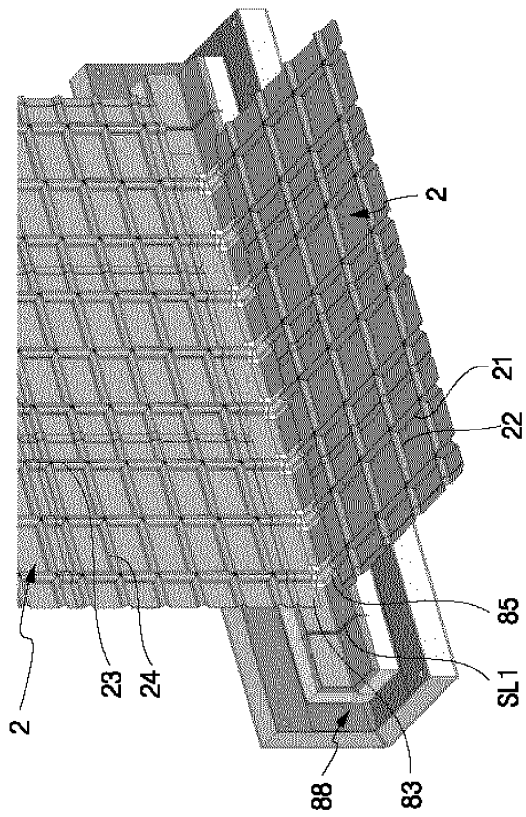


[도40]

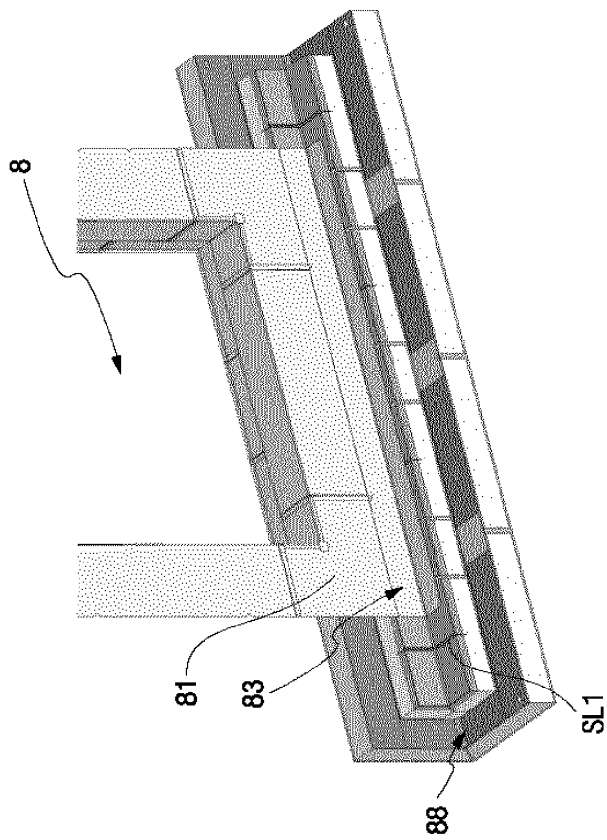




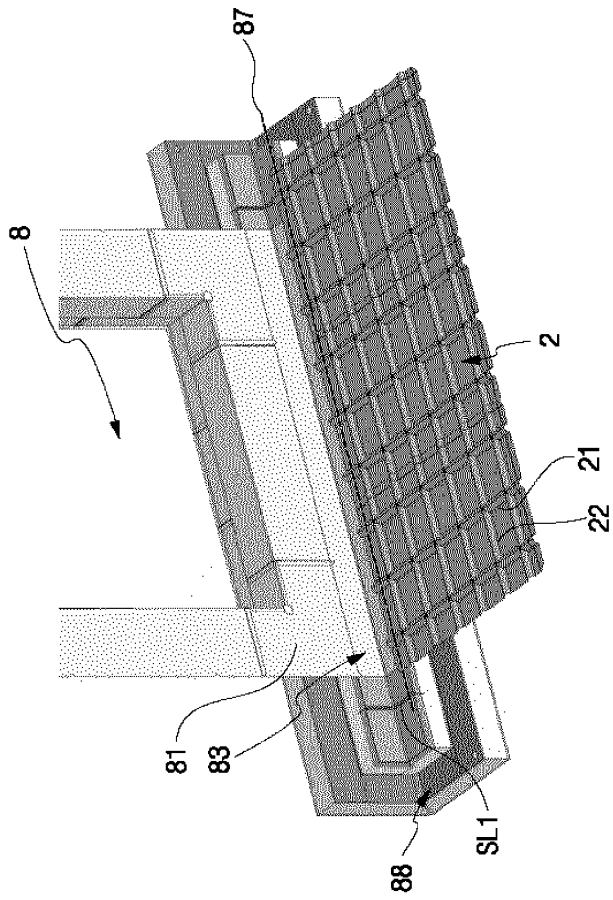
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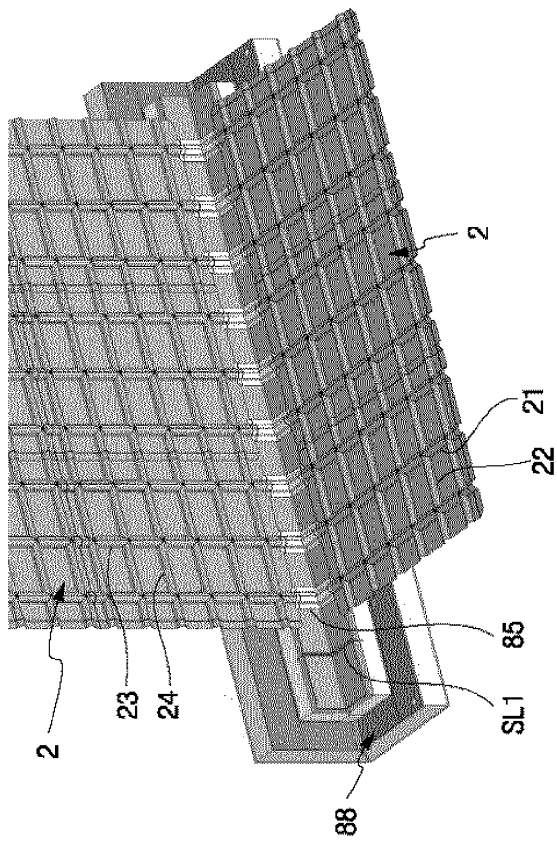
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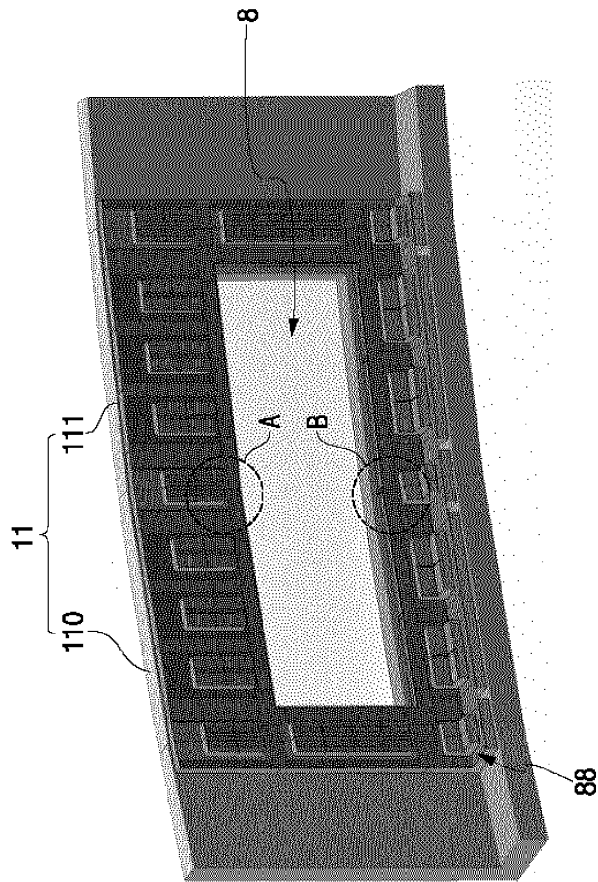
[도44]



[도45]



[도46]



[도47]

A, B

