TREATMENT OF SEMICONDUCTOR WAFERS

Field of the invention and prior art

The present invention relates to treating or cleaning the surface of a wafer in the form of a thin sheet having on its surface a layer of semiconductor material (e.g. silicon (Si) or silicon-germanium (SiGe)) termed the "useful layer", and constituting a medium from which large quantities of components (e.g. integrated circuit cells or discrete devices) can be produced.

One known technique for fabricating such wafers is the Smart Cut® technique, which can be used to obtain an SOI (silicon on insulator) wafer, for example. An example of carrying out the Smart Cut® technique applied to the production of SOI wafers is described in United States patent US-A-5 374 564 or in the article by A.J. Auberton-Hervé et al entitled "Why Can Smart-Cut Change the Future of Microelectronics?", Int Journal of High Speed Electronics and Systems, Vol 10, No 1, 2000, p 131-146. In general, the Smart Cut® technique consists in implanting atomic species into an implantation zone beneath the face of a semiconductor wafer (e.g. Si or SiGe), in bringing the face of the wafer that has undergone implantation into intimate contact with a support substrate, and in cleaving the wafer at the implantation zone to transfer the portion of the wafer that is located between the implantation zone and the surface through which implantation has taken place onto the support substrate.

Thus, a structure (e.g. SOI structure) is obtained having a layer that has been transferred onto one face of a support substrate. After cleavage and transfer, the surface of the transferred layer is treated to remove part of the thickness of the implanted layer and to reduce the roughness of said cleavage surface. Examples of such treatments are described in United States patent application US 2004/115905 and International patent

application WO-A-0115215. Typically, the treatment comprises a polishing step followed by a cleaning step carried out prior to an optional final step of sacrificial oxidation and/or a smoothing heat treatment. The polishing step can reduce the root mean square (rms) roughness to less than 2.5 Angstroms (Å) (e.g. 2 Å rms) for a scan area (carried out using an atomic force microscope, for example) of 2 micrometers (µm) by 2 µm.

More precisely, in a first step, polishing comprises a chemical-mechanical polishing step employing a polishing plate associated with a polishing solution containing both an agent for chemically attacking the surface of the layer and abrasive particles for mechanically attacking said surface, and a washing step, generally using deionized water (DIW). Thereafter, a cleaning step is carried out, consisting in treating the wafers with cleaning solutions.

To clean the surfaces of wafers having a surface layer of semiconductor material, it is known to use a standard treatment known as "RCA" (because it was developed by Radio Corporation of America) and which comprises:

· a first cleaning step using an SC1 solution (Standard Clean 1) (or APM, Ammonium-Hydrogen Peroxide Mixture); containing ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and deionized water (H_2O);

· a second cleaning step using an SC2 solution (Standard Clean 2) (or (HPM, Hydrochloric Peroxide Mixture); containing hydrochloric acid (HCl), hydrogen peroxide (H_2O_2), and deionized water.

The first solution, SC1, generally used in the range 50°C to 80°C, is principally intended to remove particles isolated on the surface of the wafer and particles buried close to the surface, as well as to render the surface hydrophilic.

The second solution, SC2, generally used in the range 70°C to 90°C, is principally intended to remove

metallic contamination that has become deposited on the wafer surface, in particular by forming chlorides.

For thin structures, i.e. structures such as SOI structures having a semiconductor useful layer of thickness of less than about 1000 Å, "HF" defect densities have been observed in the final products (i.e. after final sacrificial oxidation) which exceed the acceptable limits. "HF" defects are defects in the active semiconductor layer of the SOI structure that extend from the surface of said layer right into the buried oxide layer; their presence can be revealed by a ring pattern after treating the SOI structure with hydrofluoric acid (HF). The HF defect density observed for certain wafers may be as high as 15 defects per square centimeter (cm^2), while the recommended limit value is typically of the order of 0.5 defects per cm^2, or even less than 0.1 defects per cm^2.

HF defects are considered to be "destructive" defects for wafers, since they render them non viable (unacceptable quality) for subsequent treatments, in particular for component formation.

Summary of the invention

The invention proposes a technical solution for layers of semiconductor material that have undergone a chemical-mechanical polishing step and an RCA cleaning step which can reduce the influence of said treatments on the emergence of HF defects, in particular during subsequent treatments, and as a result can reduce the HF defect density in said layers.

This aim is achieved by a method of treating a wafer having at least a surface layer of semiconductor material, the surface of said surface layer having undergone a chemical-mechanical polishing step followed by an RCA cleaning step, in which method, after the polishing step and prior to the RCA cleaning step, an intermediate step of cleaning the surface of the surface

layer of semiconductor material is carried out using an SC1 solution under concentration and temperature conditions that allow the subsequent emergence of defects (HF defects) to be reduced compared with a similar surface layer which has not undergone said intermediate cleaning step.

As is described in detail below, the Applicant has determined that the HF defect density emerging during subsequent treatments (e.g. sacrificial oxidation) is much lower in a surface layer that has undergone an intermediate cleaning step in accordance with the invention than in a similar layer that has not undergone said step (i.e. having only undergone the polishing step and the RCA cleaning step). Without said intermediate cleaning step, defects form in the surface layer by preferential etching in the region of polishing contaminants or residues. Said defects may be defects emerging on the surface of the layer; these are thus already HF defects. When said defects do not emerge, they may become emergent defects and, as a result, HF defects, during subsequent treatments such as during thinning by sacrificial oxidation, for example, which may transform a non emergent defect into an emergent defect as thinning is "conformal", i.e. material removal is constant over the surface regardless of the initial thickness.

In one aspect of the invention, the SC1 solution comprises 1 volume of ammonium hydroxide (NH_4OH), 4 volumes of hydrogen peroxide (H_2O_2), and 10 to 40 volumes of deionized water (H_2O), said SC1 solution being used at a temperature of less than 50°C.

As an example, the SC1 solution may comprise 1 volume of ammonium hydroxide (NH_4OH), 4 volumes of hydrogen peroxide (H_2O_2), and 20 volumes of deionized water (H_2O) and be used at a temperature of 20°C ± 5°C.

The intermediate cleaning step may be carried out by immersing the wafer having the semiconductor useful layer in an SC1 solution.

In a variation, the cleaning step is carried out using a polishing unit comprising a polishing head holding the wafer, the surface of the surface layer of semiconductor material of the wafer also being held in contact with a plate, said polishing unit including an injection line via which the SC1 solution is dispensed.

The surface layer of semiconductor material is preferably less than 1000 Å thick.

The surface layer of semiconductor material may be formed from silicon (Si) or silicon-germanium (SiGe) and optionally constitute the surface layer of an SOI or SGOI (SiGe on insulator) structure respectively fabricated using the Smart Cut® technique, for example.

The present invention also provides a wafer having at least a surface layer of semiconductor material, said surface layer having a thickness of less than 1000 Å, roughness of less than 2.5 Å rms for a scan area of 2 µm × 2 µm, and an HF defect density of less than $0.5/cm^2$, or even less than $0.1/cm^2$. The wafer may be a silicon on insulator (SOI) structure.

Brief description of the figures

· Figure 1 is a diagram of a polishing unit employed to carry out the intermediate cleaning step of the invention;

· Figure 2 is a graph showing the effect of the intermediate cleaning step on silicon layers of different thicknesses.

Detailed description on implementations of the invention

The aim of the present invention is to reduce the HF defect density in finished structures having at least a surface useful layer of semiconductor material, such as a layer of silicon or silicon-germanium (SiGe) which is

less than 1000 Å thick. The term "finished" structure means a structure for which the surface of the semiconductor useful layer has undergone at least a chemical-mechanical polishing step and a step of cleaning the surface of the useful layer using an RCA treatment as described above. Said polishing step may also be preceded or followed by a surface heat treatment such as sacrificial oxidation or rapid or slow thermal anneal.

As descried in detail below, the Applicant has observed that by adding a cleaning step using an SC1 solution that is milder under its conditions of use (concentration, temperature), and that is intermediate, i.e. between the chemical-mechanical polishing step and the RCA cleaning step proper, the HF defect density in the finished structure can be significantly reduced.

Said intermediate step contributes to removing contaminants and minor defects, possibly polishing residues produced during the chemical-mechanical polishing step, and due especially to the use of a suspension of a chemical agent with abrasive particles (metallic contamination). Said contaminants and small defects act as "catalysts" in the emergence of HF defects during subsequent treatments. Said contaminants and small defects appear to constitute preferential locations for etching during the step of cleaning the surface of the semiconductor useful layer by RCA treatment and result in the emergence of defects. Said defects may pass through the thin semiconductor layer and emerge on the buried layer (e.g. oxide layer) during RCA treatment (these defects are termed HF defects since they can be revealed with HF) or are capable of emerging during a subsequent treatment, such as sacrificial oxidation.

Thus, by controlling (i.e. by reducing) the degree of etching of the SC1 solution (milder SC1 solution) used during the intermediate cleaning step, it is possible, prior to the standard RCA cleaning step, to eliminate contaminants and to passivate minor defects from which HF

defects would otherwise develop, without etching the semiconductor useful layer.

The degree of etching of the milder SC1 solution used in the intermediate cleaning step of the invention is mainly controlled by adjusting the concentrations of the components of the SC1 solution and its temperature. The intermediate cleaning step of the invention must allow elimination of contaminants and passivate minor defects to avoid the emergence of HF defects without, however, attacking the semiconductor useful layer. If the conditions of use of the SC1 solution (i.e. concentrations of constituents and temperature) endow it with too great a degree of etching, there is a risk of etching the useful layer too deeply and causing additional defects in the layer. In other words, the concentration of additive in the SC1 solution and its operating temperature must be reduced relative to the usual conditions for using SC1 solutions in RCA cleaning, but only down to a certain limit, below which the intermediate cleaning step does not have any sufficient effect (i.e. can no longer eliminate significant numbers of minor defects and contaminants or residues derived from chemical-mechanical polishing). In the light of the examples given below, the skilled person will be able to adjust the concentration and temperature conditions for the SC1 solution during the intermediate cleaning step to treat the surface of the useful layer of semiconductor material.

In known manner, an SC1 solution contains ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and deionized water (H_2O). In accordance with the invention, the formulation for the milder SC1 solution is as follows:

- 1 volume of ammonium hydroxide (NH_4OH);
- 4 volumes of hydrogen peroxide (H_2O_2); and
- 10 to 40 volumes of deionized water (H_2O).

The operating temperature of the SC1 solution in the intermediate cleaning step of the invention must not

exceed about 50°C. The solution is preferably used at ambient temperature, which avoids having to use to heating means and simplifies control of the intermediate cleaning step. In known manner, an increase in the temperature of the solution causes an increase in its degree of etching (activation).

As an example, at ambient temperature, taken to be a reference value of 20°C ± 5°C, a milder SC1 solution containing 1 volume of NH_4OH, 4 volumes of H_2O_2, and 20 volumes of H_2O provides good HF defect reduction capacity while minimizing etching of the semiconductor layer. However, an SC1 solution containing 15 volumes of H_2O also provides good results, as does an SC1 solution containing 30 volumes of H_2O at ambient temperature.

Further, the time necessary for application of said milder SC1 solution is about 1 minute.

In a first implementation of the invention, the intermediate cleaning step is carried out by immersing the wafer having the semiconductor useful layer in SC1 solution having the formulation described above. The SC1 solution is preferably at ambient temperature and the immersion time is about 1 minute.

In a further implementation of the invention, a polishing unit is employed to carry out the intermediate cleaning step with the milder SC1 solution. Figure 1 shows a polishing unit 10 which comprises a polishing head 11 into which a substrate is inserted, such as an SOI substrate 12 comprising an insulating support 120 and a layer of silicon 121 as the semiconductor useful layer. The unit 10 further comprises a plate 13 and a polishing pad 14. In accordance with the invention, a line 15, normally used to dispense abrasive suspension into the head, is used to dispense the milder SC1 solution. A pressure Fe and motion symbolized by arrow 16 are applied to the head to ensure contact of the whole surface of the layer of silicon 121 with the milder SC1 solution.

Figure 2 shows the results obtained as regards the reduction of HF defects in layers of silicon when carrying out the intermediate cleaning step using the milder SC1 solution of the invention, such as a milder SC1 solution containing 1 volume of NH_4OH, 4 volumes of H_2O_2 and 20 volumes of H_2O at ambient temperature.

In Figure 2, curves A and B represent the number of HF defects on a 200 millimeter (mm) wafer, i.e. over a surface area of 314 cm^2, observed on layers of silicon that have undergone chemical-mechanical polishing and RCA cleaning respectively, both with no intermediate cleaning step using the milder SC1 solution (curve A), and with the intermediate cleaning step using the milder SC1 solution (curve B). It will be observed that the HF defect density is linked to the thickness of the layer of silicon, curves A and B showing results where the HF defects have been revealed after thinning to the thicknesses of the layers of silicon the value of which is shown along the abscissa. This observation establishes that the HF defects observed in wafers treated using the prior art method (i.e. chemical-mechanical polishing directly followed by standard RCA treatment with no intermediate cleaning step) result in the presence of non emergent defects in the thicker layer. Said defects are transformed into HF defects during thinning of the layer.

As can be seen in Figure 2, the HF defect density in the layers of silicon is considerably reduced when an additional cleaning step in accordance with the invention (see curve B) is carried out compared with the same layers which have not undergone intermediate cleaning (see curve A). The impact of the intermediate cleaning step on the reduction of the HF defect density becomes significant for layers which are less than 1000 Å thick; and the smaller the thickness, the greater the effect.

The intermediate cleaning step of the invention as described above can minimize defects in a layer of

semiconductor material that has undergone a chemical-mechanical polishing step followed by an RCA cleaning step. As a result, the present invention is applicable to wafers of semiconductor materials alone (e.g. silicon or silicon-germanium) or to multilayer wafers having a surface layer constituted by a layer of semiconductor material.

The intermediate cleaning step of the invention as described above can in particular significantly reduce the HF defect density in SOI (or SGOI) structures typically comprising a surface layer of semiconductor material, such as silicon (or a silicon-germanium alloy) having a thickness of less than 1000 Å, which structures are fabricated using the Smart Cut® technique, i.e. by transfer (after implantation and cleavage) of a fine layer of semiconductor material onto an insulating support, necessitating steps of chemical-mechanical polishing and RCA cleaning of the surface of the transferred layer of semiconductor.

CLAIMS

1. A method of treating a wafer having at least a surface layer of semiconductor material, the surface of said surface layer having undergone a chemical-mechanical polishing step followed by an RCA cleaning step, the method being characterized in that, after the polishing step and prior to the RCA cleaning step, it comprises an intermediate step of cleaning the surface of the surface layer of semiconductor material using an SC1 solution under concentration and temperature conditions that allow the emergence of defects in the surface layer to be reduced compared with a similar surface layer which has not undergone said intermediate cleaning step.

2. A method according to claim 1, characterized in that the SC1 solution comprises 1 volume of ammonium hydroxide (NH_4OH), 4 volumes of hydrogen peroxide (H_2O_2), and 10 volumes of deionized water (H_2O), said SC1 solution being at ambient temperature.

3. A method according to claim 1, characterized in that the SC1 solution comprises 1 volume of ammonium hydroxide (NH_4OH), 4 volumes of hydrogen peroxide (H_2O_2), and 40 volumes of deionized water (H_2O), said SC1 solution being at ambient temperature.

4. A method according to claim 1, characterized in that the SC1 solution comprises 1 volume of ammonium hydroxide (NH_4OH), 4 volumes of hydrogen peroxide (H_2O_2), and 20 volumes of deionized water (H_2O), said SC1 solution being at a temperature of 20°C ± 5°C.

5. A method according to any one of claims 1 to 4, characterized in that the intermediate cleaning step is carried out for about 1 minute.

6. A method according to any one of claims 1 to 5, characterized in that the intermediate cleaning step is carried out by immersing the wafer having the semiconductor useful layer in an SC1 solution.

7. A method according to any one of claims 1 to 5, characterized in that the cleaning step is carried out using a polishing unit comprising a polishing head holding the wafer, the surface of the surface layer of semiconductor material of the wafer also being held in contact with a plate, said polishing unit including an injection line via which the SC1 solution is dispensed.

8. A method according to any one of claims 1 to 7, characterized in that the surface layer of semiconductor material is less than 1000 Å thick.

9. A method according to any one of claims 1 to 8, characterized in that the surface layer of semiconductor material is made of silicon (Si).

10. A method according to claim 9, characterized in that the wafer is a silicon on insulator (SOI) structure fabricated using the Smart-Cut® technique.

11. A method according to any one of claims 1 to 8, characterized in that the surface layer of semiconductor material is made of silicon-germanium (SiGe).

12. A method according to claim 11, characterized in that the wafer is a silicon-germanium on insulator (GGOI) structure fabricated using the Smart Cut® technique.

13. A wafer having at least a surface layer of semiconductor material, said surface layer having a thickness of less than 1000 Å, roughness of less than

2.5 Å rms for a scan area of 2 µm × 2 µm, and an HF defect density of less than 0.5/cm^2.

14. A wafer according to claim 13, characterized in that it comprises a silicon on insulator (SOI) structure.

15. A wafer according to claim 13 or claim 14, characterized in that it has an HF defect density of less than 0.1/cm^2.