CLAIMS

What is claimed is:

1. A structure comprising:

a three contact analog memory structure comprising:

a volatile memory element in series with a non-volatile memory element, wherein the three contact analog memory structure comprises a drain contact, a read contact, and a write contact, wherein current flow along a write path of the three contact analog memory structure is different from current flow along a read path of the three contact analog memory structure.

2. The structure of claim 1, wherein the non-volatile memory element comprises a memristive device.

3. The structure of claim 1, wherein the volatile memory element comprises a material that temporarily changes its resistance when subjected to an electrical field across the material.

4. The structure of claim 1, wherein the volatile memory element comprises a material which becomes more conductive upon application of an electric potential across the material and returns to a relaxed state once the electrical field induced by electric potential is removed.

5. The structure of claim 1, wherein the volatile memory element comprises a volatile memory layer located between a first conductive layer and a second conductive layer.

6. The structure of claim 1, wherein the volatile memory element comprises a volatile memory layer, and wherein a material for the volatile memory layer comprises an MITMIEC material.

7. The structure of claim 1, wherein the volatile memory element comprises a volatile memory layer, and wherein a material for the volatile memory layer is selected from the group consisting of: $XCoO_2$, $XNbO_2$, XVO_2, $XNbO_3$, $X_{4x}Ti_5O_{12}$, and/or $XSmNiO_3$, wherein X is an alkali metal.

8. The structure of claim 2, wherein the non-volatile memory element comprises a bi-directional non-volatile memory.

9. The structure of claim 2, wherein the non-volatile memory element comprises a uni-directional non-volatile memory.

10. The structure of claim 2, wherein the non-volatile memory element comprises a resistive random-access memory (RRAM).

11. The structure of claim 2, wherein the non-volatile memory element comprises a conductive bridging random-access memory (CBRAM).

12. The structure of claim 2, wherein the non-volatile memory element comprises a electrochemical random-access memory (ECRAM).

13. The structure of claim 2, wherein the non-volatile memory element comprises a phase change memory (PCM).

14. A memory structure comprising:

a three terminal memory structure comprising a volatile memory element in series with a non-volatile memory element, wherein the three terminal memory structure comprises different terminals for a read path and a write path, and wherein the volatile memory element is located in the write path of the three terminal memory structure.

15. The structure of claim 14, wherein the volatile memory layer comprises a material that temporarily changes its resistance when subjected to electrical potential across the material.

16. The structure of claim 14, wherein the volatile memory element comprises a material which becomes more conductive upon application of an electric potential across the material and returns to a relaxed state once the electric potential is removed.

17. The structure of claim 14, wherein the volatile memory element comprises a volatile memory layer located between a first conductive layer and a second conductive layer.

18. The structure of claim 14, wherein a material for the volatile memory layer is selected from the group consisting of: $XCoO_2$, $XNbO_2$, XVO_2, $XNbO_3$, $X_{4x}Ti_5O_{12}$, and/or $XSmNiO_3$, wherein X is an alkali metal.

19. A method of writing to a memory structure comprising:

applying a first pulse to an analog memory structure, wherein the analog memory structure comprises a volatile memory element and a non-volatile memristive element in series; and

applying a second pulse to the analog memory structure, wherein a time between the first pulse and the second pulse is less than a relaxation rate of the volatile memory element.

20. The method of claim 19 further comprising applying a third pulse to the analog memory structure, wherein the time between the second pulse and the third pulse is substantially similar to the time between the first pulse and the second pulse.

21. A method of writing to a memory structure comprising:

applying a first pulse to an analog memory structure, wherein the analog memory structure comprises a volatile memory element and a non-volatile memristive element in series;

applying a second pulse to the analog memory structure, and wherein a first time between the first pulse and the second pulse is less than a relaxation rate of the volatile memory element; and

applying a third negative pulse to the analog memory structure, wherein a second time between the second pulse and the third negative pulse is less than the relaxation rate of the volatile memory element and more than the first time.

22. The method of claim 21 further comprising:

prior to the first pulse, applying a plurality of pulses to the analog memory structure, wherein each pulse is substantially similar, and wherein a duration between pulses is substantially similar.

23. A method of writing to an analog memory structure comprising:

applying a first pulse to an analog memory structure, wherein the analog memory structure comprises a volatile memory element and a non-volatile memristive element in series;

applying a second pulse to the analog memory structure, and wherein a first time between the first pulse and the second pulse is less than a relaxation rate of the volatile memory element; and

applying a third pulse to the analog memory structure, wherein a second time between the second pulse and the third pulse is less than the relaxation rate of the volatile memory element and more than the first time.

24. The method of claim 23 further comprising:

prior to the first pulse, applying a plurality of pulses to the analog memory structure, wherein each pulse is substantially similar, and wherein a duration between pulses is substantially similar.

25. The structure of claim 1, wherein the read path involves current flow from the read contact to the drain contact, and wherein the write path involves current flow from the write contact to the drain contact.