

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
12 December 2002 (12.12.2002)

PCT

(10) International Publication Number
WO 2002/099963 A3

(51) International Patent Classification⁷: **G11C 5/14**,
G05F 1/56, 3/26

(21) International Application Number:
PCT/US2002/017039

(22) International Filing Date: 31 May 2002 (31.05.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/872,844 1 June 2001 (01.06.2001) US

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(71) Applicant: QUALCOMM INCORPORATED [US/US];
5775 Morehouse Drive, San Diego, CA 92121-1714 (US).

Published:
— with international search report

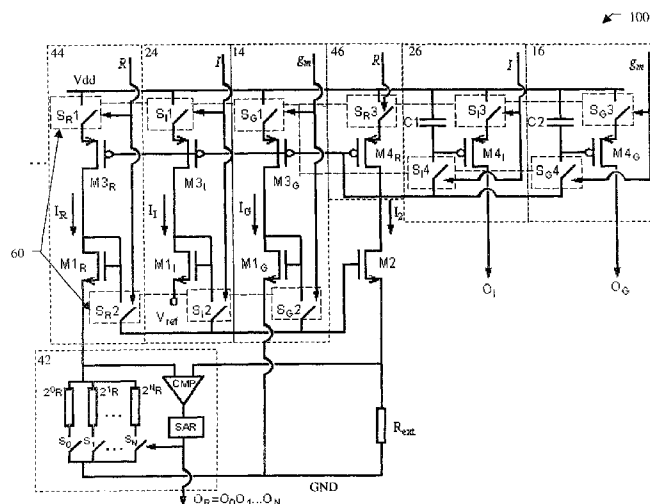
(72) Inventor: PAPATHANNASIOU, Kostas; 8324 Via
Sonoma #70, La Jolla, CA 92037 (US).

(88) Date of publication of the international search report:
12 February 2004

(74) Agents: WADSWORTH, Philip, R. et al.; Qualcomm Incorporated, 5775 Morehouse Drive, San Diego, CA 92121-1714 (US).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SYSTEM AND METHOD FOR TUNING A VLSI CIRCUIT



(57) Abstract: A circuit (100) for accurately tuning the absolute values of multiple parameters in a VLSI circuit by reusing a single external resistor. In the illustrative embodiment, the invention includes a first circuit (10) for generating an accurate transconductance using a single external resistor; a second circuit (20) for generating an accurate current reference using the same external resistor; and a switching circuit (60) for alternately switching on and off the first and second circuits in order to share the external resistor. The switching circuit (60) includes several switches controlled by a digital counter for turning off portions of the circuit which are not in use. In the illustrative embodiment, the invention further includes a third circuit (40) for generating one or more additional accurate reference signals. The third circuit can generate an accurate internal resistance R_{int} , an accurate drain to source resistance of a transistor r_{DS} , and/or an accurate internal capacitance C_{int} .

WO 2002/099963 A3