CLAIMS:

1. A method used in forming a memory array comprising strings of memory cells, comprising:

forming a stack over a control circuitry region, the stack comprising vertically-alternating insulative tiers and wordline tiers;

forming first charge-blocking material to extend elevationally along the vertically-alternating tiers, the first charge-blocking material having k of at least 7.0 and comprising a metal oxide;

forming a second charge-blocking material laterally inward of the first charge-blocking material, the second charge-blocking material having k less than 7.0;

forming storage material laterally inward of the second charge-blocking material;

forming insulative charge-passage material laterally inward of the storage material; and

forming channel material to extend elevationally along the insulative tiers and the wordline tiers laterally inward of the insulative charge-passage material and the storage material extending into the control circuitry regions with the storage material extending along an entirety of an elevation of the channel material.

2. The method of claim 1 wherein the first charge-blocking material has k of at least 8.0 and the second charge-blocking material has k of no more than 5.0.

3. The method of claim 2 wherein the first charge-blocking material has k of at least 9.0 and the second charge-blocking material has k of no more than 4.0.

4. The method of claim 1 wherein the first charge-blocking material comprises an insulative metal oxide comprising at least one of Al, Hf, Zr, Ti, La, Sc, Ta, and Dy.

5. The method of claim 4 wherein the first charge-blocking material comprises at least one of an aluminate and a silicate.

6. The method of claim 4 wherein the insulative metal oxide comprises multiple elemental metals.

7. The method of claim 4 wherein the insulative metal oxide comprises Al_2O_3.

8. The method of claim 1 wherein the second charge-blocking material comprises SiO_2.

9. The method of claim 1 comprising forming conductive material of individual wordlines in the wordline tiers after forming the channel material.

10. The method of claim 9 comprising:

forming insulator material to extend elevationally along the vertically-alternating tiers prior to forming the first charge-blocking material; and

removing the insulator material within the wordline tiers to expose a laterally outer sidewall of the first charge-blocking material prior to forming the conductive material, the conductive material being formed in the wordline tiers directly against the exposed laterally outer sidewalls of the first charge-blocking material.

11. The method of claim 10 comprising forming the insulator material by atomic layer deposition and to be directly against insulating material of the insulative tiers.

12. The method of claim 11 wherein the insulating material and the insulator material are of the same composition relative one another.

13. The method of claim 1 comprising forming conductive material of individual wordlines in the wordline tiers before forming the first charge-blocking material.

14. The method of claim 1 comprising forming each of the second charge-blocking material, the storage material, and the insulative charge-passage material to extend elevationally along the vertically-alternating tiers.

15. The method of claim 1 comprising forming CMOS under array circuitry.

16. A memory array comprising strings of memory cells, comprising:

a vertical stack over a control circuitry region, the vertical stack comprising vertically-alternating insulative tiers and wordline tiers, the wordline tiers comprising gate regions of individual memory cells, individual of the gate regions comprising part of a wordline in individual of the wordline tiers;

channel material extending elevationally along the insulative tiers and the wordline tiers and into the control circuitry region;

the individual memory cells comprising a memory structure laterally between the individual gate regions and the channel material, the memory structure comprising:

a first charge-blocking material extending elevationally along the vertically-alternating tiers; the first charge-blocking material being directly against the individual gate regions, comprising a metal oxide, and having k of at least 7.0;

a second charge-blocking material laterally inward of the first charge-blocking material, the second charge-blocking material having k less than 7.0;

storage material laterally inward of the second charge-blocking material, the storage material extending an entire elevation of the channel material and into the control circuitry region; and

insulative charge-passage material laterally inward of the storage material.

17. The memory array of claim 16 comprising NAND.

18. The memory array of claim 16 comprising CMOS under array circuitry.

19. The memory array of claim 16 wherein the first charge-blocking material has k of at least 8.0 and the second charge-blocking material has k of no more than 5.0.

20. The memory array of claim 18 wherein the first charge-blocking material has k of at least 9.0 and the second charge-blocking material has k of no more than 4.0.

21. The memory array of claim 16 wherein the first charge-blocking material comprises an insulative metal oxide comprising at least one of Al, Hf, Zr, Ti, La, Sc, Ta, and Dy.

22. The memory array of claim 20 wherein the first charge-blocking material comprises at least one of an aluminate and a silicate.

23. The memory array of claim 20 wherein the insulative metal oxide comprises multiple elemental metals.

24. The memory array of claim 20 wherein the insulative metal oxide comprises Al_2O_3.

25. The memory array of claim 16 wherein the second charge-blocking material comprises SiO_2.

26. The memory array of claim 16 wherein the second charge-blocking material is directly against the first charge-blocking material, the storage material id directly against the second charge-blocking material, and the insulative charge-passage material is directly against the storage material.