FIG. 1

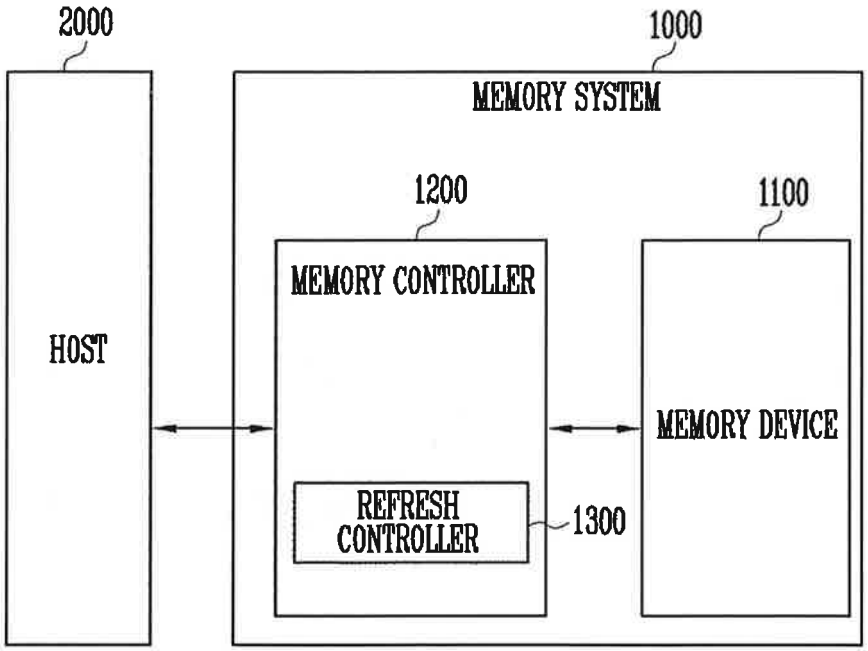

2000
1000
MEMORY SYSTEM
1200
1100
MEMORY CONTROLLER
HOST
MEMORY DEVICE
REFRESH CONTROLLER
1300

FIG. 2

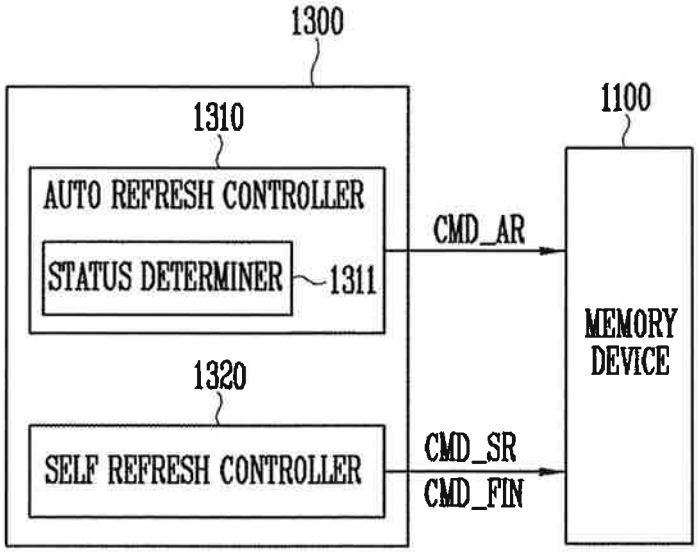

1300
1310
1100
AUTO REFRESH CONTROLLER
CMD_AR
STATUS DETERMINER
1311
MEMORY DEVICE
1320
SELF REFRESH CONTROLLER
CMD_SR
CMD_FIN

FIG. 3

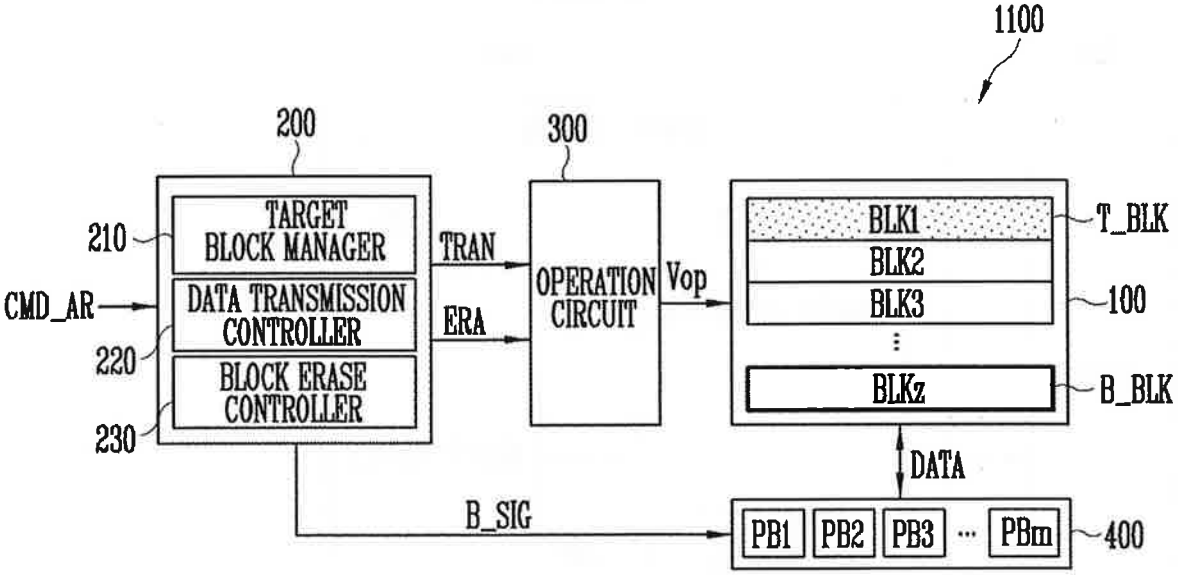

1100
200
300
210
TARGET BLOCK MANAGER
CMD_AR
DATA TRANSMISSION CONTROLLER
220
BLOCK ERASE CONTROLLER
230
TRAN
ERA
OPERATION CIRCUIT
Vop
BLK1
BLK2
BLK3
BLKz
T_BLK
100
B_BLK
DATA
B_SIG
PB1
PB2
PB3
PBm
400

FIG. 4

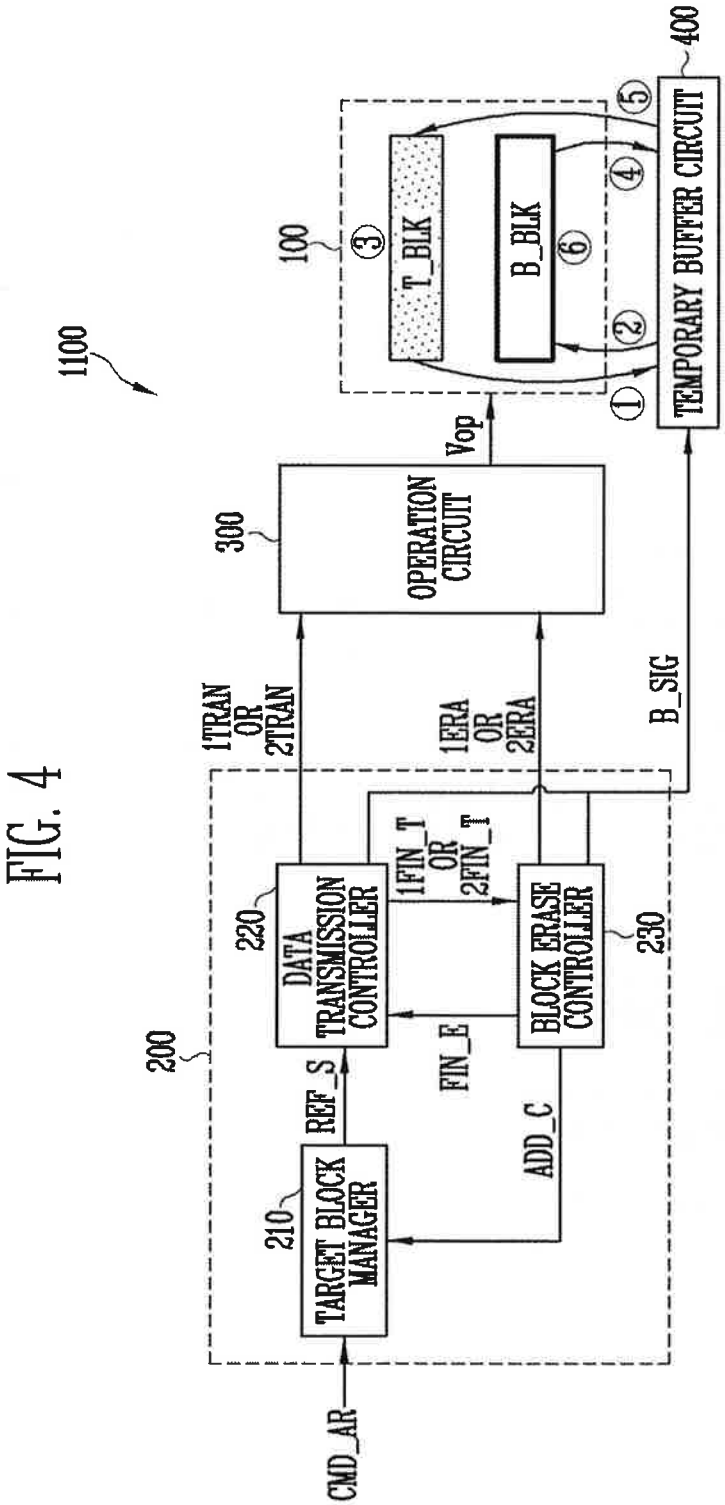

1100
100
T_BLK
B_BLK
400
TEMPORARY BUFFER CIRCUIT
Vop
300
OPERATION CIRCUIT
1TRAN OR 2TRAN
1ERA OR 2ERA
B_SIG
200
220
DATA TRANSMISSION CONTROLLER
1FIN_T OR 2FIN_T
230
BLOCK ERASE CONTROLLER
FIN_E
REF_S
ADD_C
210
TARGET BLOCK MANAGER
CMD_AR

FIG. 5A

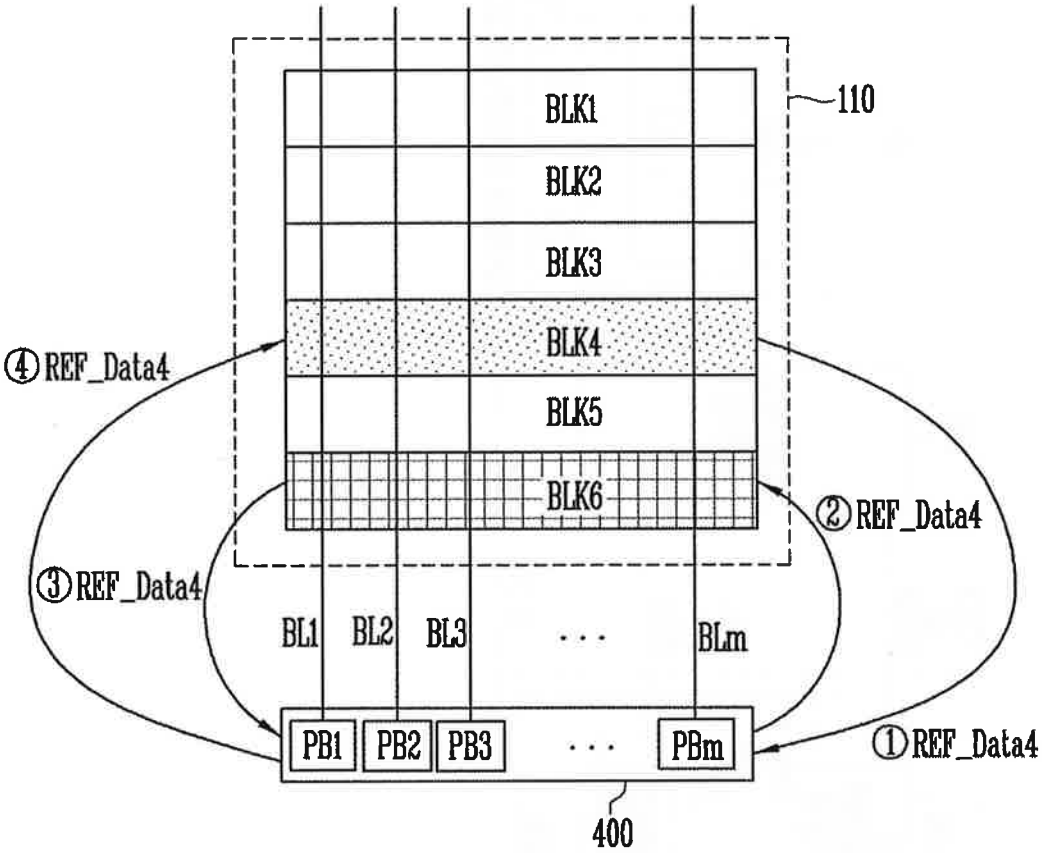


FIG. 5B

BEFORE REFRESH	BLK4
AFTER REFRESH	BLK4

FIG. 6

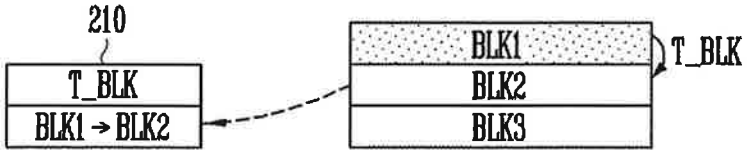

210
T_BLK
BLK1 → BLK2
BLK1
BLK2
BLK3
T_BLK

FIG. 7

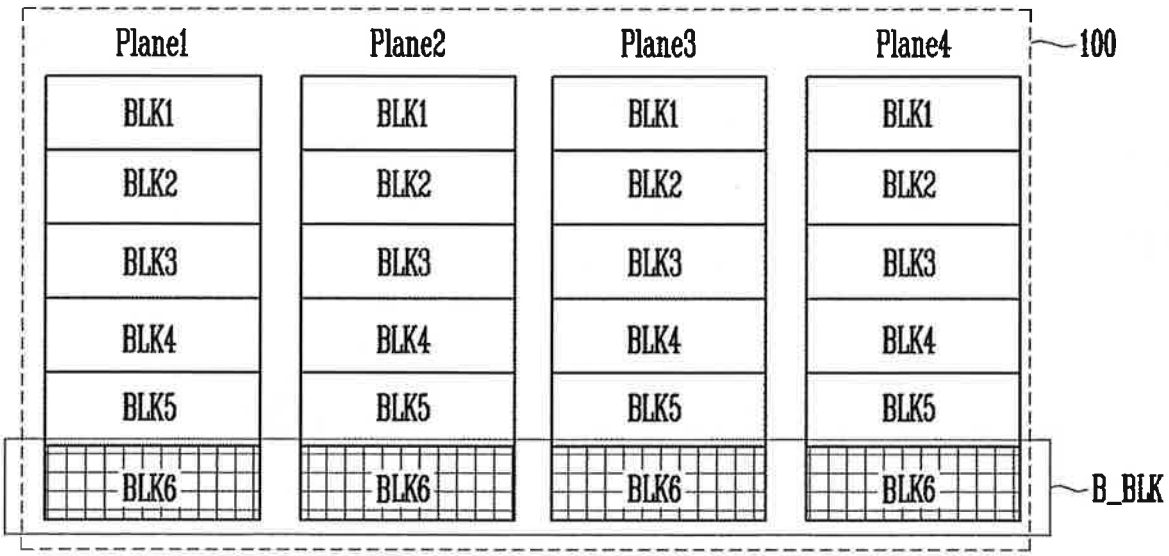

Plane1
Plane2
Plane3
Plane4
100
BLK1
BLK2
BLK3
BLK4
BLK5
BLK6
B_BLK

FIG. 8

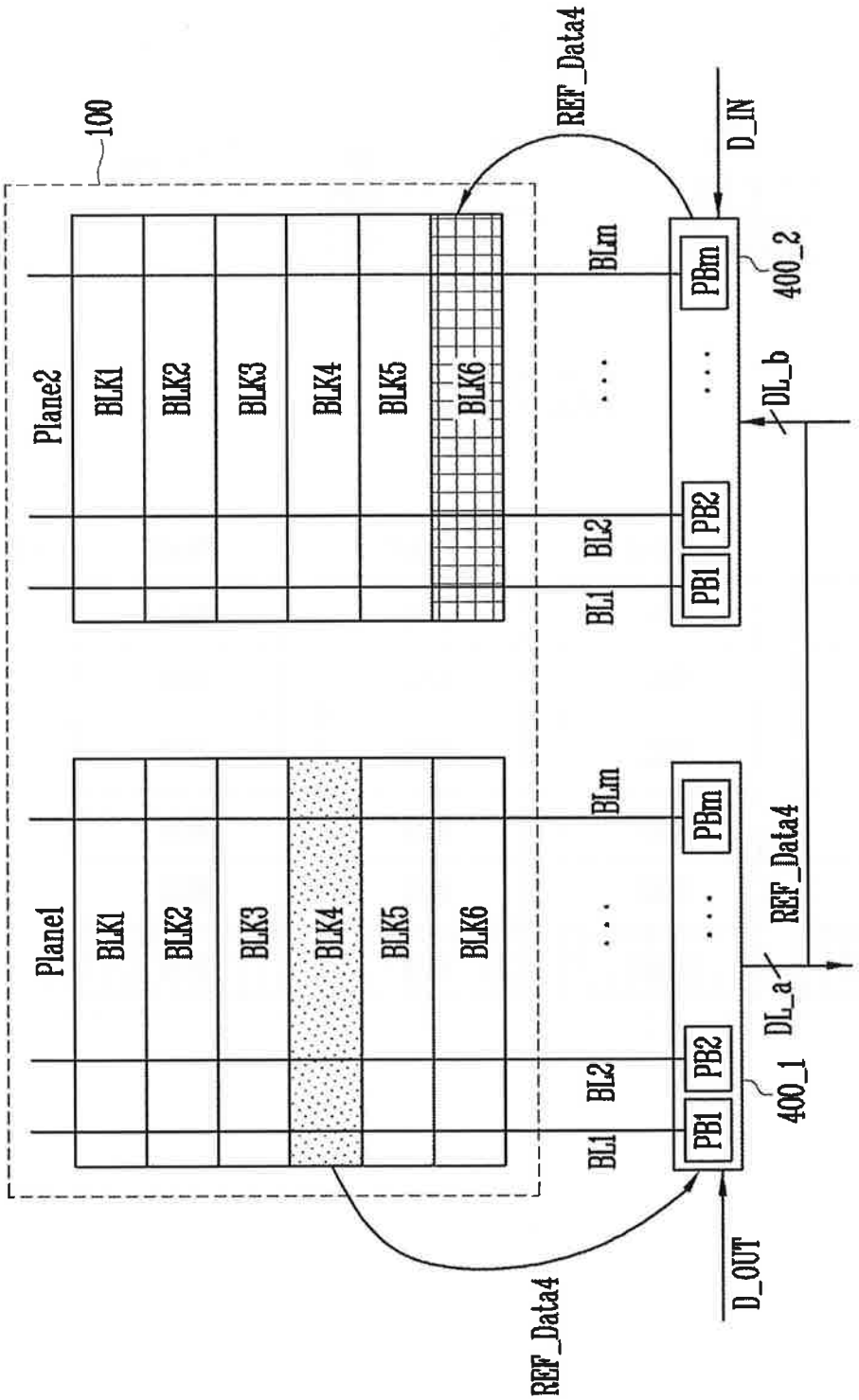

100
Plane2
BLK1
BLK2
BLK3
BLK4
BLK5
BLK6
Plane1
BLK1
BLK2
BLK3
BLK4
BLK5
BLK6
BL1
BL2
BLm
PB1
PB2
PBm
400_1
400_2
DL_a
DL_b
REF_Data4
REF_Data4
REF_Data4
D_IN
D_OUT

FIG. 9

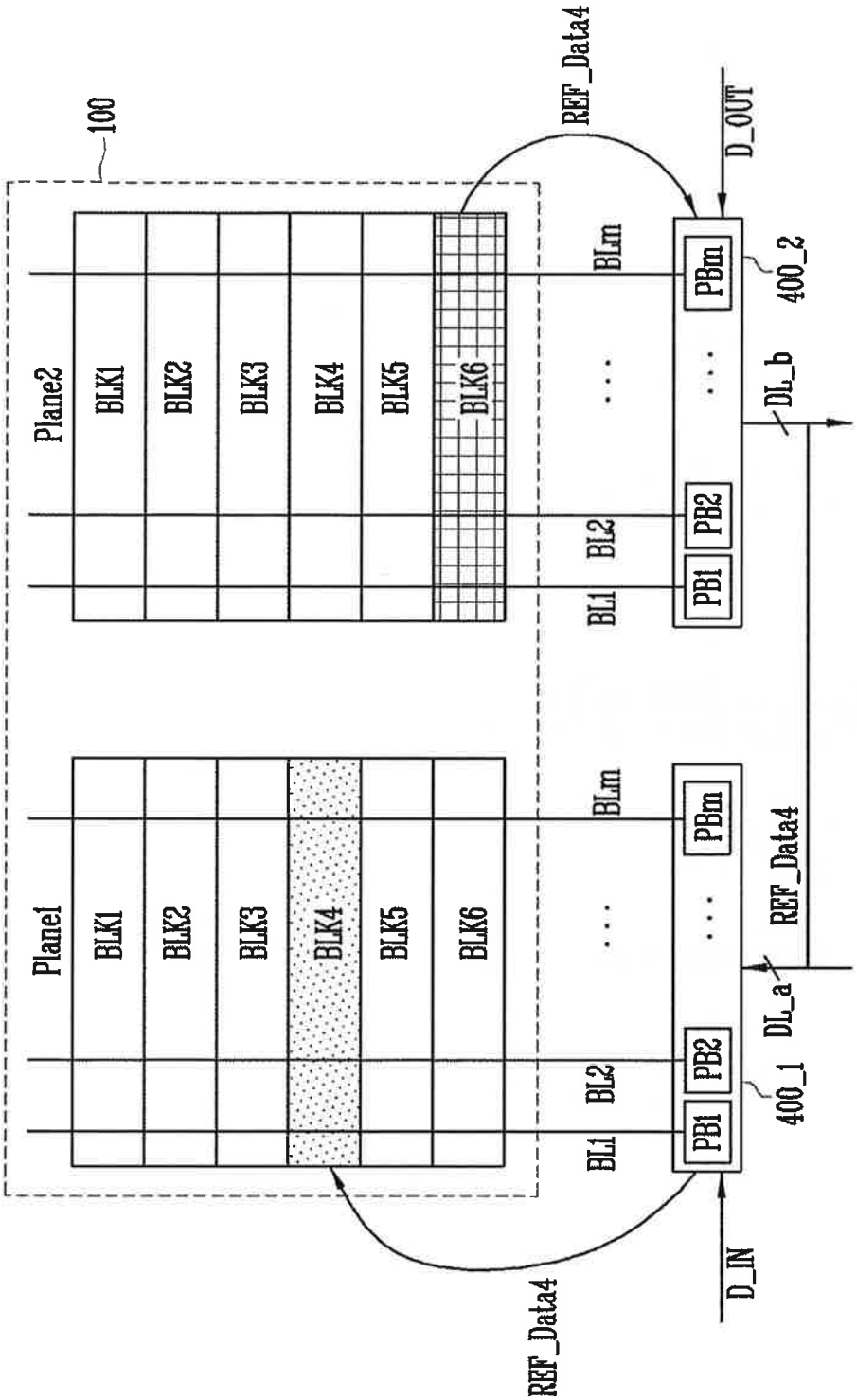

100
Plane2
BLK1
BLK2
BLK3
BLK4
BLK5
BLK6
Plane1
BLK1
BLK2
BLK3
BLK4
BLK5
BLK6
BLm
BL2
BL1
PBm
PB2
PB1
400_2
400_1
DL_b
DL_a
REF_Data4
D_OUT
D_IN
REF_Data4
REF_Data4

FIG. 10

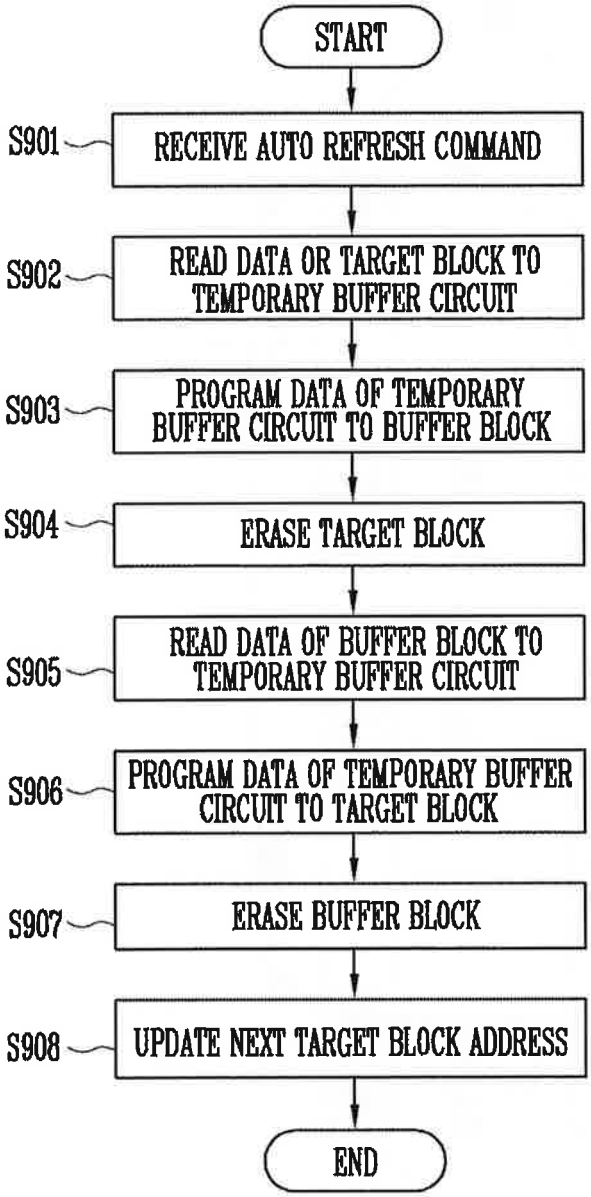

START
S901
RECEIVE AUTO REFRESH COMMAND
S902
READ DATA OR TARGET BLOCK TO TEMPORARY BUFFER CIRCUIT
S903
PROGRAM DATA OF TEMPORARY BUFFER CIRCUIT TO BUFFER BLOCK
S904
ERASE TARGET BLOCK
S905
READ DATA OF BUFFER BLOCK TO TEMPORARY BUFFER CIRCUIT
S906
PROGRAM DATA OF TEMPORARY BUFFER CIRCUIT TO TARGET BLOCK
S907
ERASE BUFFER BLOCK
S908
UPDATE NEXT TARGET BLOCK ADDRESS
END

FIG. 11

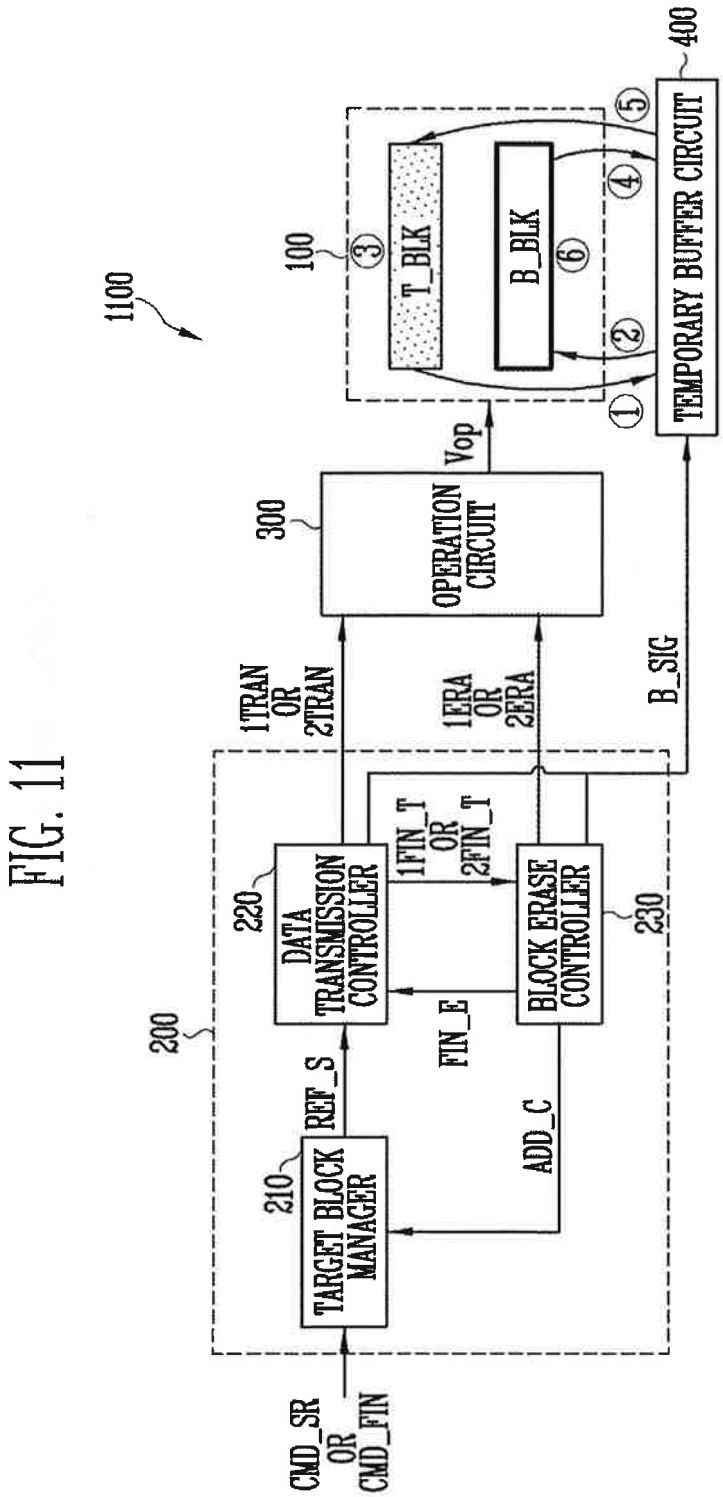

1100
100
T_BLK
B_BLK
TEMPORARY BUFFER CIRCUIT
400
Vop
300
OPERATION CIRCUIT
1TRAN OR 2TRAN
1ERA OR 2ERA
B_SIG
200
220
DATA TRANSMISSION CONTROLLER
1FIN_T OR 2FIN_T
BLOCK ERASE CONTROLLER
230
FIN_E
REF_S
ADD_C
210
TARGET BLOCK MANAGER
CMD_SR OR CMD_FIN

FIG. 12

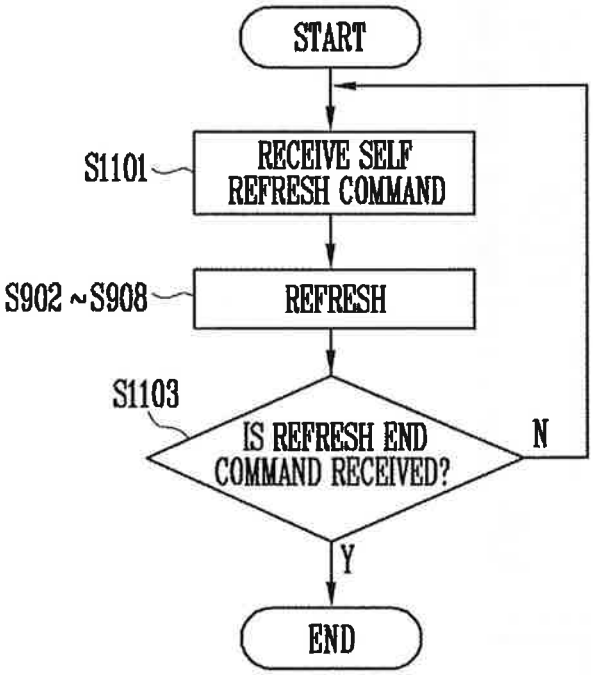

START
S1101
RECEIVE SELF REFRESH COMMAND
S902 ~S908
REFRESH
S1103
IS REFRESH END COMMAND RECEIVED?
N
Y
END

FIG. 13

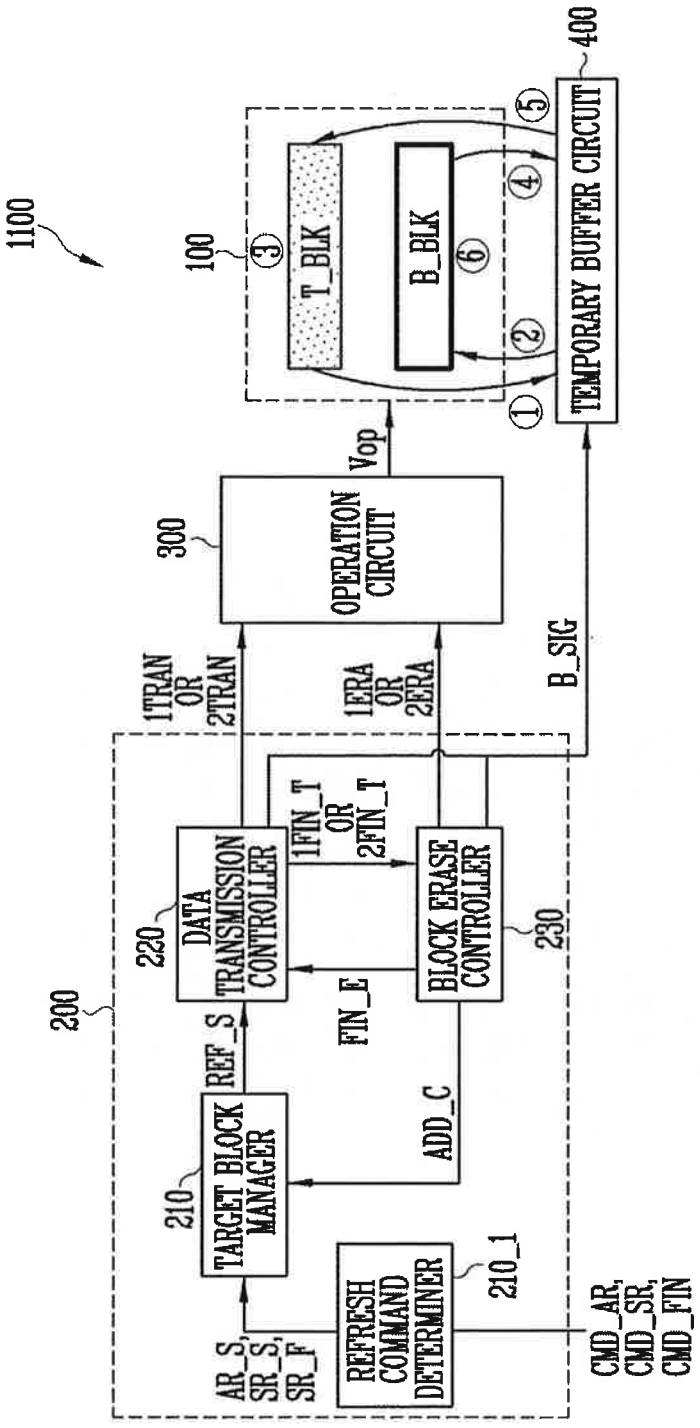

1100
100
T_BLK
B_BLK
400
TEMPORARY BUFFER CIRCUIT
300
OPERATION CIRCUIT
Vop
1TRAN OR 2TRAN
1ERA OR 2ERA
B_SIG
200
220
DATA TRANSMISSION CONTROLLER
1FIN_T OR 2FIN_T
BLOCK ERASE CONTROLLER
230
REF_S
FIN_E
ADD_C
210
TARGET BLOCK MANAGER
210_1
REFRESH COMMAND DETERMINER
AR_S, SR_S, SR_F
CMD_AR, CMD_SR, CMD_FIN

FIG. 14

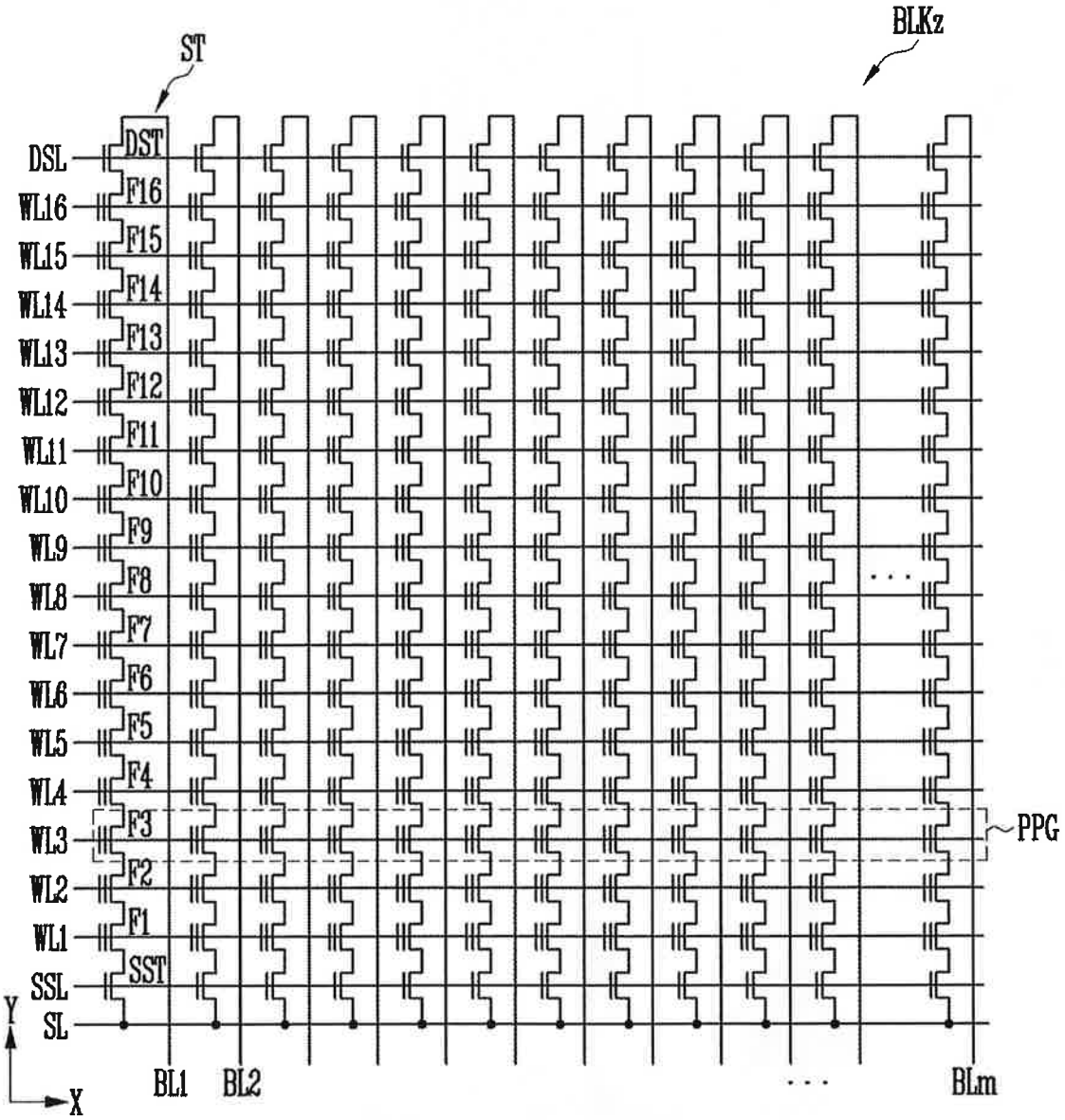

ST
BLKz
DSL
DST
WL16
F16
WL15
F15
WL14
F14
WL13
F13
WL12
F12
WL11
F11
WL10
F10
WL9
F9
WL8
F8
WL7
F7
WL6
F6
WL5
F5
WL4
F4
WL3
F3
WL2
F2
WL1
F1
SSL
SST
SL
PPG
BL1
BL2
BLm
Y
X

FIG. 15

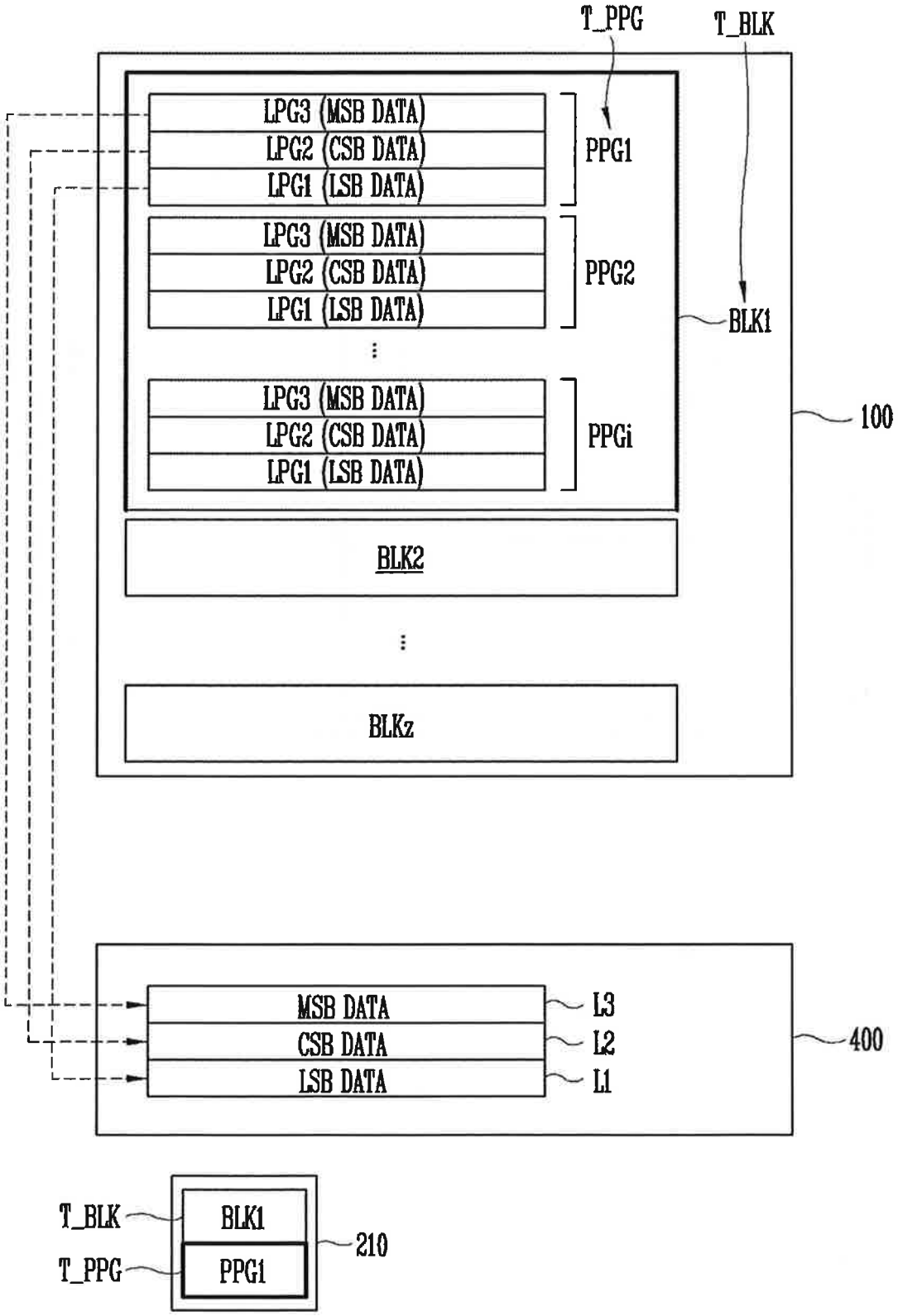

T_PPG
T_BLK
LPG3 (MSB DATA)
LPG2 (CSB DATA)
LPG1 (LSB DATA)
PPG1
LPG3 (MSB DATA)
LPG2 (CSB DATA)
LPG1 (LSB DATA)
PPG2
BLK1
LPG3 (MSB DATA)
LPG2 (CSB DATA)
LPG1 (LSB DATA)
PPGi
100
BLK2
BLKz
MSB DATA
CSB DATA
LSB DATA
L3
L2
L1
400
T_BLK
T_PPG
BLK1
PPG1
210

FIG. 16

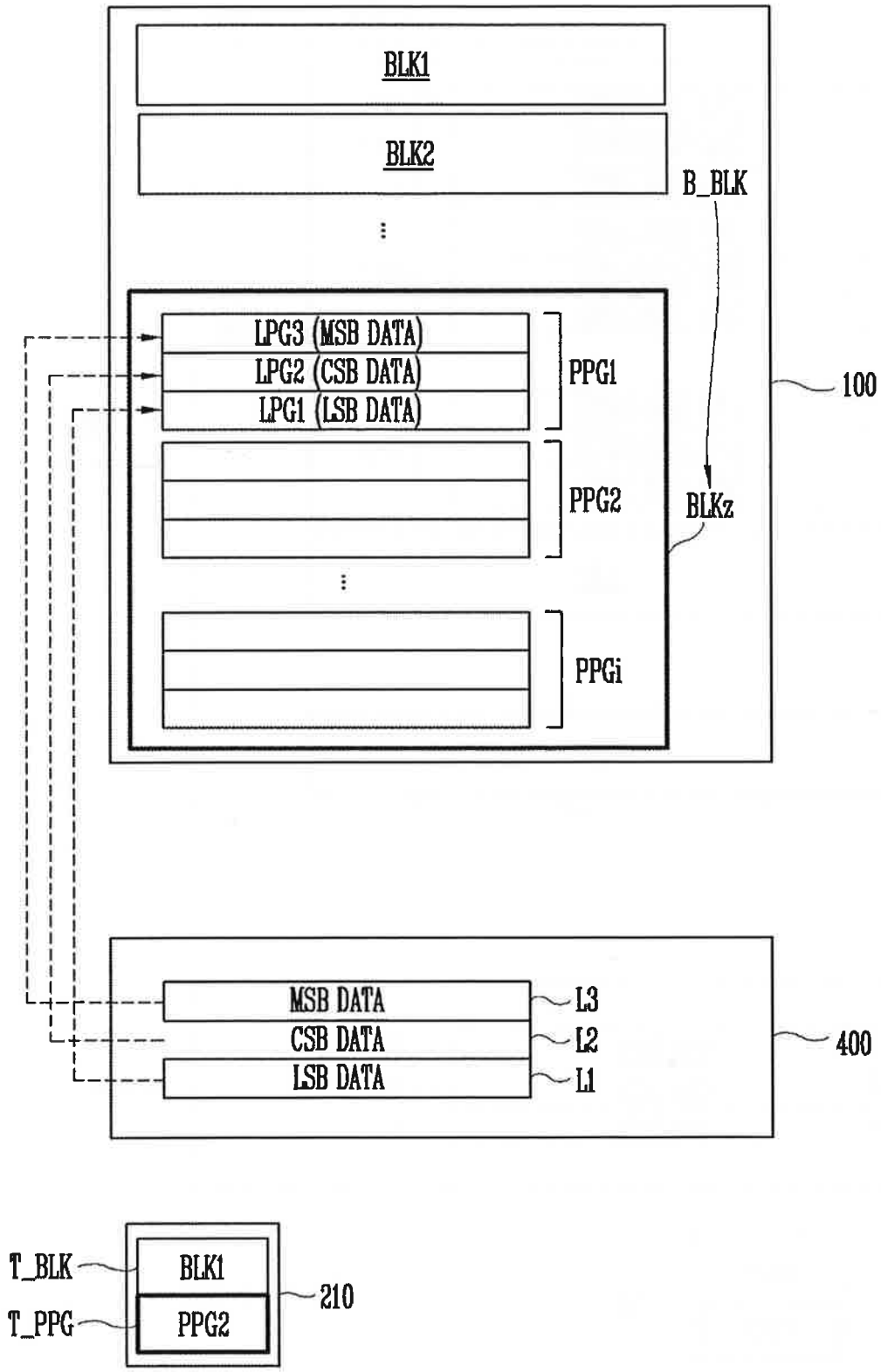

BLK1
BLK2
B_BLK
LPG3 (MSB DATA)
LPG2 (CSB DATA)
LPG1 (LSB DATA)
PPG1
PPG2
PPGi
BLKz
100
MSB DATA
CSB DATA
LSB DATA
L3
L2
L1
400
T_BLK
T_PPG
BLK1
PPG2
210

FIG. 17

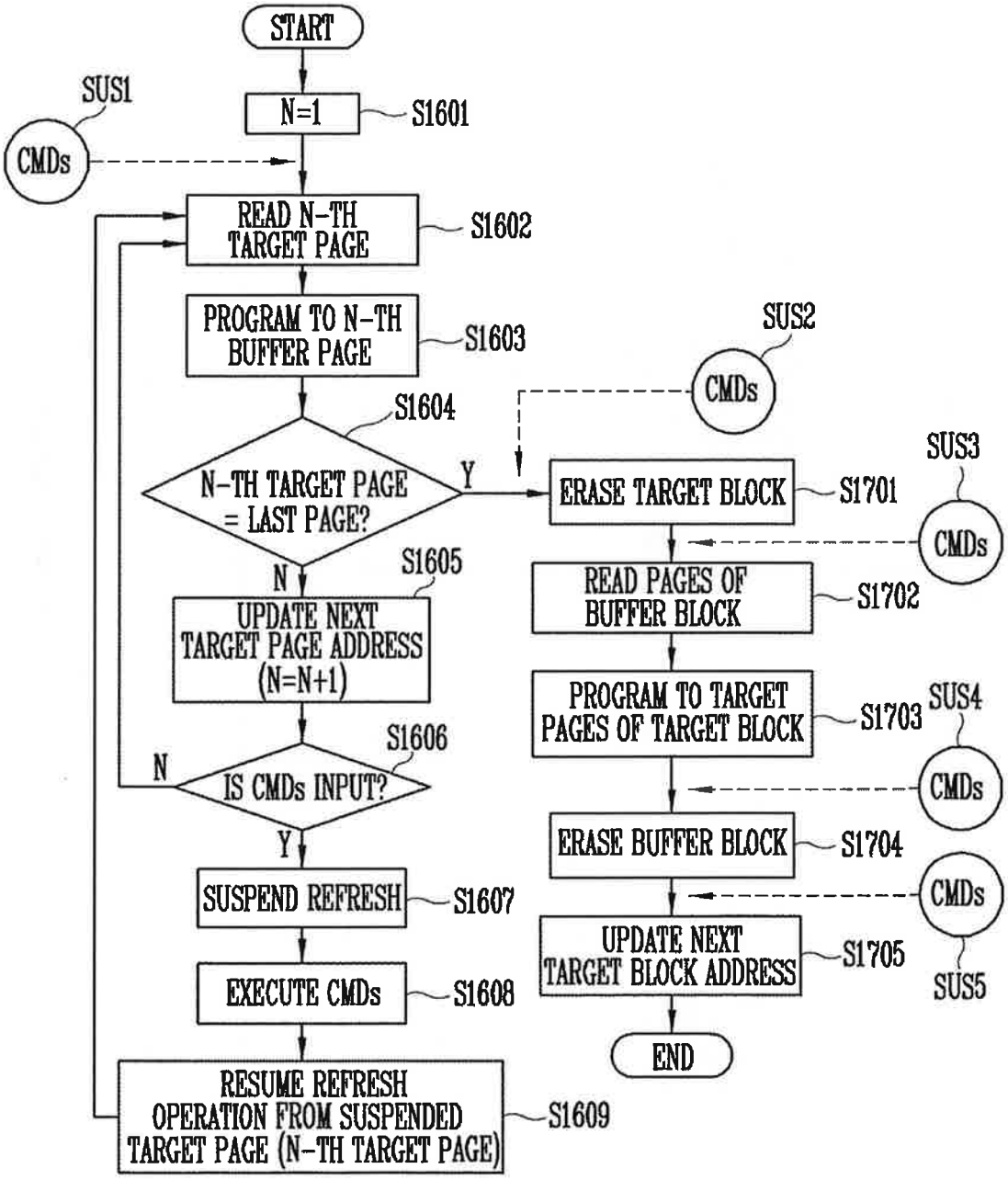

START
N=1
S1601
SUS1
CMDs
READ N-TH TARGET PAGE
S1602
PROGRAM TO N-TH BUFFER PAGE
S1603
S1604
N-TH TARGET PAGE = LAST PAGE?
Y
N
S1605
UPDATE NEXT TARGET PAGE ADDRESS (N=N+1)
S1606
IS CMDs INPUT?
N
Y
SUSPEND REFRESH
S1607
EXECUTE CMDs
S1608
RESUME REFRESH OPERATION FROM SUSPENDED TARGET PAGE (N-TH TARGET PAGE)
S1609
SUS2
CMDs
ERASE TARGET BLOCK
S1701
SUS3
CMDs
READ PAGES OF BUFFER BLOCK
S1702
PROGRAM TO TARGET PAGES OF TARGET BLOCK
S1703
SUS4
CMDs
ERASE BUFFER BLOCK
S1704
CMDs
UPDATE NEXT TARGET BLOCK ADDRESS
S1705
SUS5
END

FIG. 18

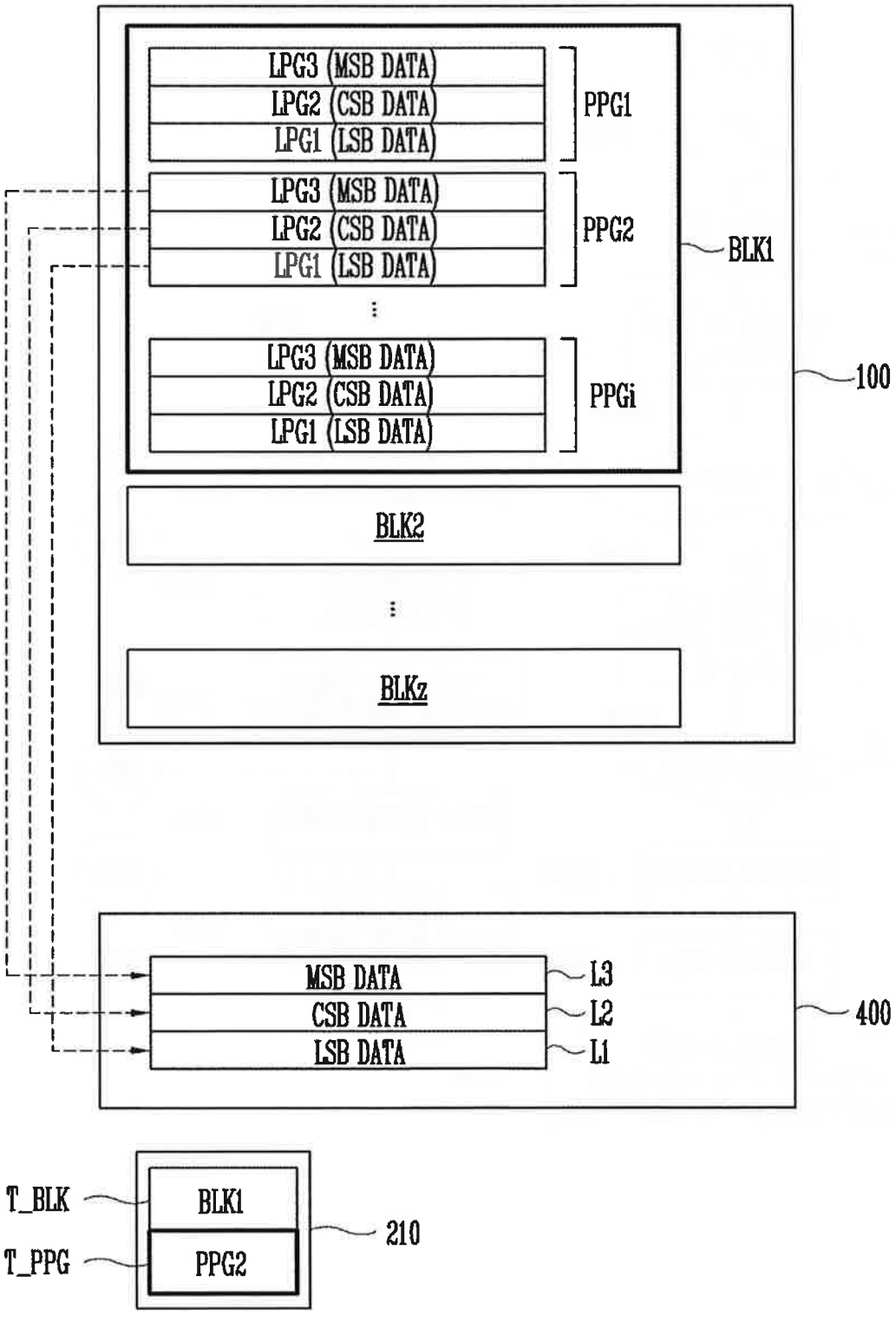

LPG3 (MSB DATA)
LPG2 (CSB DATA)
LPG1 (LSB DATA)
PPG1
LPG3 (MSB DATA)
LPG2 (CSB DATA)
LPG1 (LSB DATA)
PPG2
BLK1
LPG3 (MSB DATA)
LPG2 (CSB DATA)
LPG1 (LSB DATA)
PPGi
100
BLK2
BLKz
MSB DATA
CSB DATA
LSB DATA
L3
L2
L1
400
T_BLK
T_PPG
BLK1
PPG2
210

FIG. 19

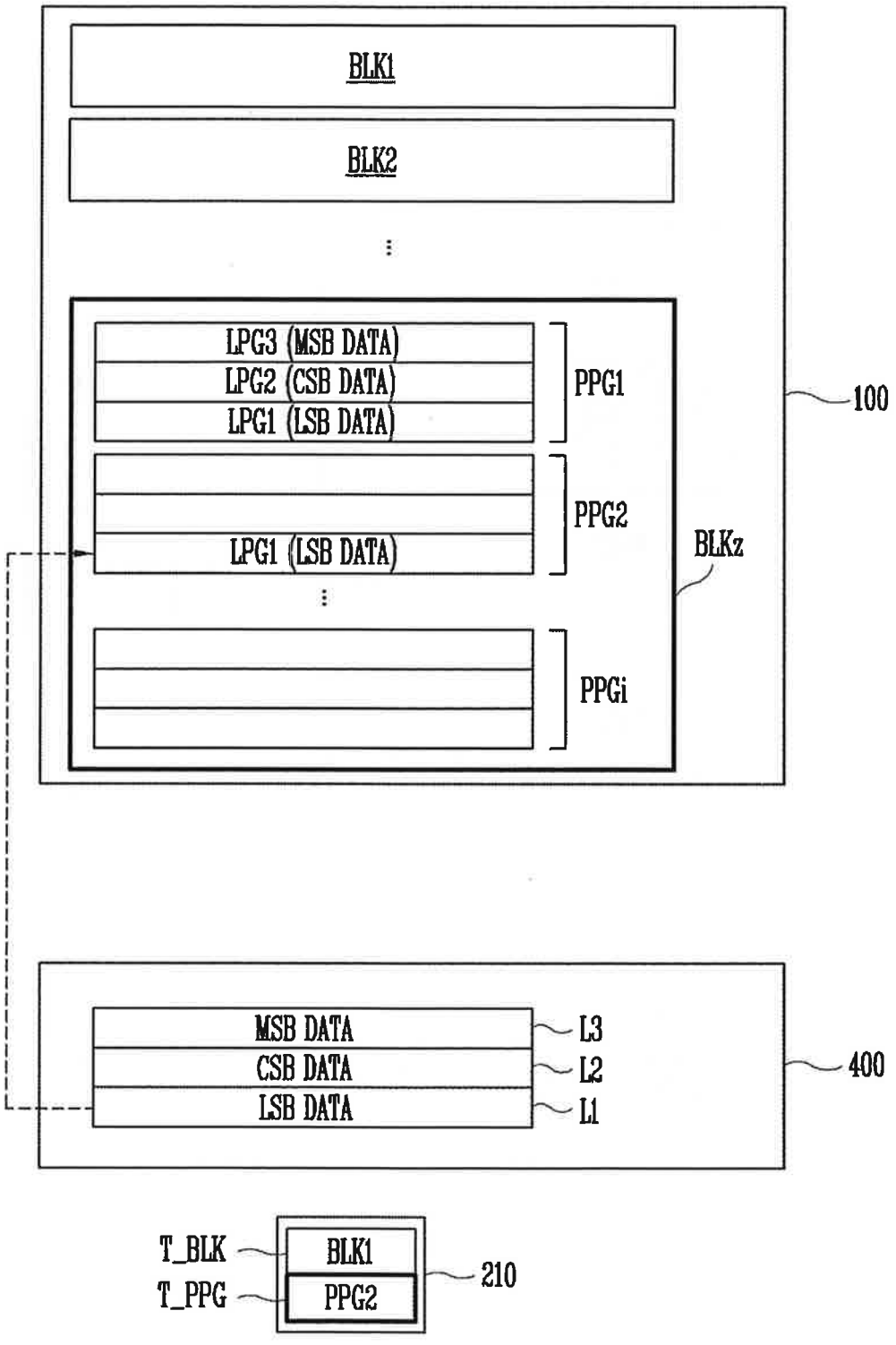

BLK1
BLK2
LPG3 (MSB DATA)
LPG2 (CSB DATA)
LPG1 (LSB DATA)
PPG1
PPG2
LPG1 (LSB DATA)
PPGi
BLKz
100
MSB DATA
CSB DATA
LSB DATA
L3
L2
L1
400
T_BLK
T_PPG
BLK1
PPG2
210

FIG. 20

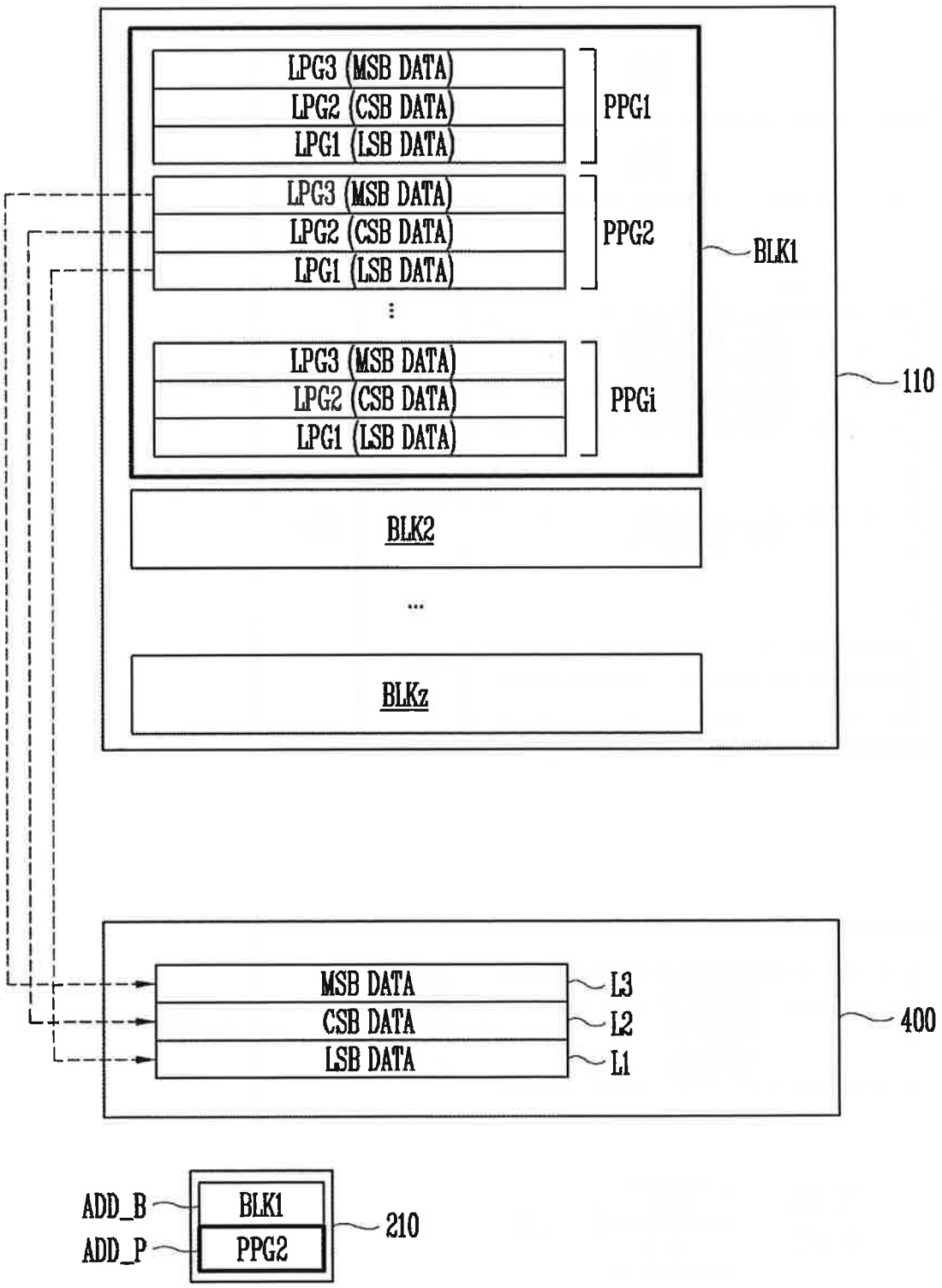

LPG3 (MSB DATA)
LPG2 (CSB DATA)
LPG1 (LSB DATA)
PPG1
LPG3 (MSB DATA)
LPG2 (CSB DATA)
LPG1 (LSB DATA)
PPG2
BLK1
LPG3 (MSB DATA)
LPG2 (CSB DATA)
LPG1 (LSB DATA)
PPGi
110
BLK2
...
BLKz
MSB DATA
CSB DATA
LSB DATA
L3
L2
L1
400
ADD_B
ADD_P
BLK1
PPG2
210

FIG. 21

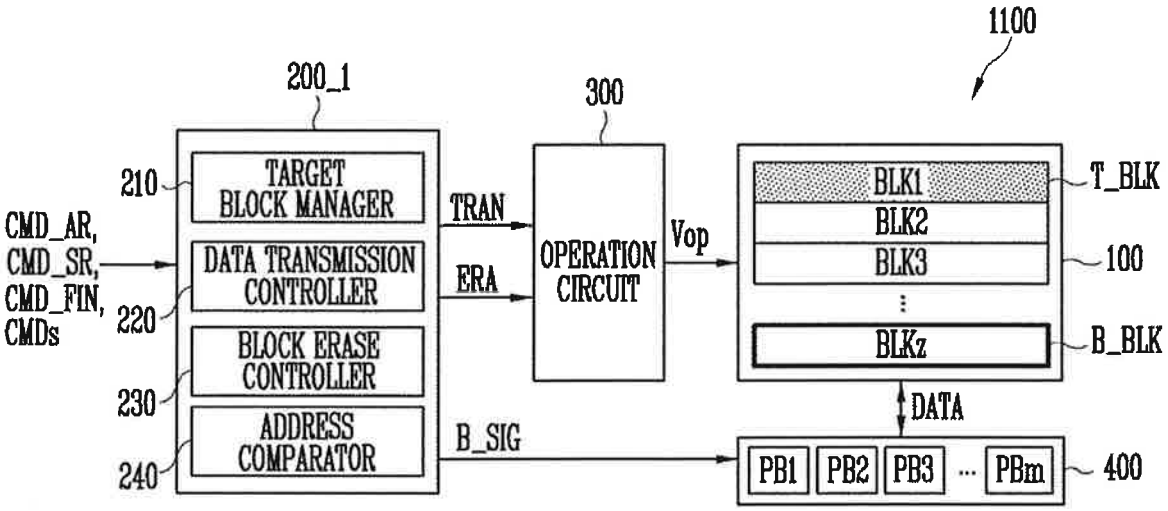
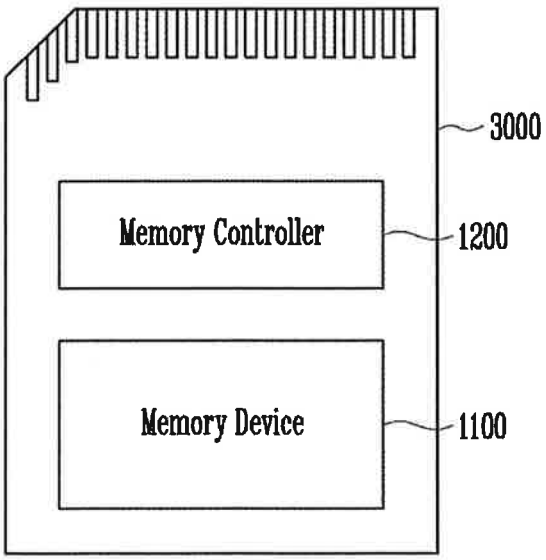

1100
200_1
300
210
TARGET BLOCK MANAGER
CMD_AR, CMD_SR, CMD_FIN, CMDs
220
DATA TRANSMISSION CONTROLLER
230
BLOCK ERASE CONTROLLER
240
ADDRESS COMPARATOR
TRAN
ERA
B_SIG
OPERATION CIRCUIT
Vop
BLK1
BLK2
BLK3
BLKz
T_BLK
100
B_BLK
DATA
PB1
PB2
PB3
PBm
400

FIG. 22


3000
Memory Controller
1200
Memory Device
1100