LIQUID CRYSTAL DISPLAY APPARATUS, STRUCTURE FOR MOUNTING SEMICONDUCTOR DEVICE, METHOD OF MOUNTING SEMICONDUCTOR DEVICE, ELECTRONIC OPTICAL APPARATUS AND ELECTRONIC PRINTING APPARATUS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a liquid crystal display apparatus having a plurality of semiconductor chips for driving liquid crystal.

Description of Related Art

Mounting of a driver IC for driving liquid crystal for use in a conventional liquid crystal display apparatus will now be described with reference to Figs. 90, 91, 92 and 93. A driver IC 50041 is mounted on a tape-carrier package (hereinafter called a "TCP") 50042 and connected to a panel 16 while interposing a connection member 19. Input lines 50044 and output lines 50045 of the TCP 50042 to and from the driver IC 50041 are disposed on the same surface of the TCP 50042, the connection with the panel 16 being established by using the connection member 19 so that a leading portion 50046 of the output line pattern 50045 on the surface of the TCP substrate 50042 and a panel terminal 18 are connected to each other.

Another method of mounting the driver IC for driving liquid crystal for use in the conventional liquid crystal display apparatus will now be described with reference to Figs. 90, 91, 92, 93, 94 and 95. The driver IC 50041 is mounted on the tape-carrier package (hereinafter called the "TCP") 50042 and connected to the panel 16 while interposing an anisotropic conductive film 50049. In the TCP 50042, the input lines 50044 to the driver IC 50041 and the output lines 50045 from the driver IC 50041 are disposed on the surface of the substrate TCP 50042 and are connected to the panel 16 in such a manner that the leading portion 50046 of the output line pattern 50045 on the surface of the substrate TCP 50042 and the panel terminal 18 are connected by using the anisotropic conductive film 50049. The anisotropic conductive film 50049 is mainly made of conductive

particles 50050 and an adhesive agent 50051. The thickness (H) of the adhesive agent 50051 is made to be lager than the particle size (D) of the conductive particles 50050. If the thickness (K) of the leading portion 50046 of the TCP 50042 is larger than the particle size (D) of the conductive particle 50050, a connection state shown in Fig. 95 is therefore realized in which the conductive particles 50050 are so crushed that conduction is established. If the thickness (k) of a connection terminal 13 is smaller than the particle size (D) of the conductive particle 50050, the adhesive agent 50051 cannot be removed sufficiently. In this case, there arises a problem in that the electrical connection by the conductive particles 50050 cannot be established satisfactorily.

The input line 50044 to the driver IC 50041 is, by soldering, connected to another substrate (hereinafter called a "bus substrate) 50043 for supplying input signals and electric power. The bus substrate 50043 is formed into two-layer shape so that the bus line can be wired in a cross manner. However, the detailed illustrations about the wired portions and connection portions are omitted here. The major portion of the TCP 50042 and the bus substrate 50043 are positioned outside the outline of the panel 16 so that the area required to mount the semiconductor chip is very wide. Further, the bus substrate must be used as an individual element and, accordingly, the cost cannot be reduced.

Then, a COG (Chip On Glass) method will now be described with reference to Fig. 93. Fig. 93 is a cross sectional view which illustrates an essential portion in which the semiconductor chip is mounted by the COG method. If a bus line 50048 is intended to be wired on the panel substrate, it must be wired on the panel substrate in a manner crossing an input line 50047 to the driver IC 50041 for driving liquid crystal. Since the lines must be formed by thin metal films made of Au or Ni or the like, each line must have a large width in order to reduce the resistance value. Therefore, a large area is required to mount the semiconductor chip, and what is worse, the cost cannot be reduced because wiring using the thin metal film must be performed in the cross manner.

A conventional liquid crystal display apparatus includes

display pixels composed of matrix electrodes each consisting of line electrodes and column electrodes. Display signals for driving a semiconductor device disposed in the peripheral portion of the liquid crystal display device in a TAB (Tape-Automated-Bonding) manner are supplied to an electrode terminal of the display device connected with an anisotropic conductive adhesive agent or a conductive rubber connector.

Figs. 97 and 98 illustrate an example of the mounting structure employed in a liquid crystal display apparatus in which a semiconductor device mounted in the TAB manner is connected to a liquid crystal display device.

Referring to Figs. 97 and 98, a TCP (Tape-Carrier-Package) 50151 for driving liquid crystal comprises a semiconductor device 111 for driving liquid crystal which is mounted on a flexible wiring member 50152 in the so-called TAB method. Further, a TCP output terminal 50153 disposed on one side of the TCP 50151 is connected to the terminal portion of a liquid crystal member 110 with an anisotropic conductive agent 115, while a TCP input terminal 50154 and a drive control circuit substrate 50155 disposed on the other side are connected by soldering.

Since the foregoing conventional technology must comprise an individual wiring substrate (the bus substrate) for supplying input signals and electric power to the driver IC and thin metal film lines wired in the cross manner, the area required to mounting the semiconductor chip cannot be reduced. Therefore, there arises a problem in that a liquid crystal display apparatus, the cost and the size of which can be reduced, cannot be provided.

SUMMARY OF THE INVENTION

The present invention is directed to overcome the foregoing problem.

Accordingly, an object of the present invention is to provide a liquid crystal display apparatus which requires a small area for mounting the semiconductor chip for driving liquid crystal thereof, the thickness and the size of which can be reduced and the cost of which can therefore be reduced satisfactorily.

The foregoing conventional technology has an arrangement that semiconductor devices 111 for driving liquid crystal are, by a TAB mounting method, connected to the electrodes of the liquid crystal display devices 110 in the sequential order of the column (connected in parallel to the pixels and sequentially) while being formed into a TCP shape for each semiconductor device. Further, the semiconductor devices 111 are connected to a drive control circuit substrate 50155 for supplying electric power for driving liquid crystal and control signals (hereinafter called a "bus lines").

Since a liquid crystal display apparatus of the type having the foregoing mounting structure and adapted to the color display requires a pixel density three times that of white and black display apparatus when the same resolution as that realized by the white and black display apparatus is intended to be realized. It leads to a fact that the number of lines for mutually connecting the TCPs increases excessively to maintain the reliability in the connection. Further, the drive control circuit substrate 50155 must have a precise wiring rule due to the increase in the number of the terminals, and, accordingly, the substrate must be formed into a multi-layer shape. As a result, the size of the liquid crystal display apparatus cannot be reduced and the number of required elements increases undesirably. Therefore, the overall cost of the apparatus cannot be reduced.

Fig. 99 is a view which illustrates the structure of a conventional color liquid crystal display apparatus disclosed in Japanese Patent Laid-Open No. 2-214826. In order to be adaptable to the increased number of the color display pixels, TCPs 50151-1 to 50151-3 are formed into three layers. The portions in which the foregoing TCPs 50151-1 to 50151-3 are connected to the drive control circuit substrate 50155 are arranged in the same as those of the structure shown in Fig. 98. Therefore, the number of required connections increases due to the rise in the pixel density. Hence, the defect occurring in the connection cannot be prevented. What is worse, the structure, in which the TCPs are stacked, causes the semiconductor device to project in the direction of the thickness, resulting in a problem to rise in

that the size of the apparatus cannot be reduced.

Accordingly, the present invention is directed to overcome the foregoing problems and therefore an object of the present invention is to provide a liquid crystal display apparatus capable of displaying precise and high density color images by a liquid crystal thereof while necessitating reduced cost and the size thereof.

A liquid crystal display apparatus according to the present invention is characterized in that; a semiconductor chip for driving liquid crystal is mounted on the surface of a multi-layer substrate; the multi-layer substrate is electrically connected to a panel terminal, the multi-layer substrate having an upper surface in which an input line pattern to the chip and an output line pattern from the chip are formed, a reverse side having a terminal to be connected to a terminal of a liquid crystal panel and at least one intermediate layer formed between the upper surface and the reverse surface and having a portion of the input lines and/or the output lines as a circuit pattern, wherein each of the lines are connected via through holes; and a plurality of multi-layer substrates are electrically connected to one another by conduction and connection means.

The structure of the liquid crystal display apparatus according to the present invention has an arrangement that bus lines and connection terminals are formed on the laminated substrate, and a plurality of the semiconductor devices are mounted to be connected to electrodes of the display device. As a result, the drive control circuit substrate can be omitted from the structure and the number of mutual connections between semiconductor devices can be decreased. Therefore, reliability can be improved and the size of the apparatus can be reduced.

Other and further objects, features and advantages of the invention will be appear more fully from the following description.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an exploded view which illustrates a multi-layer substrate according to an embodiment of the present invention;

Fig. 2 illustrates a liquid crystal display apparatus

according to an embodiment of the present invention;

Fig. 3 illustrates an essential portion of the liquid crystal display apparatus according to the embodiment of Fig. 2;

Fig. 4 is a cross sectional view which illustrates an essential portion of the liquid crystal display apparatus according to the embodiment of Fig. 2;

Fig. 5 is an exploded view which illustrates a multi-layer substrates according to another embodiment of the present invention;

Fig. 6 illustrates an essential portion of the liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 7 is an exploded view which illustrates a multi-layer substrate according to another embodiment of the present invention;

Fig. 8 illustrates an essential portion of the liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 9 illustrates an essential portion of the liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 10 is a cross sectional view which illustrates an essential portion of the liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 11 is an exploded view which illustrates a multi-layer substrates according to another embodiment of the present invention;

Fig. 12 illustrates an essential portion of the liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 13 illustrates an essential portion of the liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 14 illustrates an essential portion of the liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 15 is an exploded view which illustrates a multi-layer substrate according to an embodiment of the present invention;

Fig. 16 illustrates a liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 17 illustrates an essential portion of the liquid crystal display apparatus according to the present invention;

Fig. 18 is a cross sectional view which illustrates the liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 19 is an exploded view which illustrates the liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 20 illustrates an essential portion of the liquid crystal display apparatus according to the other embodiment of the present invention;

Fig. 21 is a cross sectional view which illustrates an anisotropic conductive film according to an embodiment of the present invention;

Fig. 22 is a cross sectional view which illustrates an anisotropic conductive film according to another embodiment of the present invention;

Fig. 23 is a cross sectional view which illustrates an anisotropic conductive film according to another embodiment of the present invention;

Fig. 24 is a cross sectional view which illustrates an essential portion of the connection portion of the anisotropic conductive film or an anisotropic conductive adhesive agent;

Fig. 25 is a cross sectional view which illustrates the structure for mounting a semiconductor device and a state where it is connected to a display device according to an embodiment of the present invention;

Fig. 26 is a plan view of the structure shown in Fig. 25;

Fig. 27 is a circuit diagram of a connection portion according to an embodiment of the present invention;

Fig. 28 is a circuit block diagram for a liquid crystal display apparatus according to an embodiment of the present invention;

Fig. 29 illustrates a structure for mounting a semiconductor device according to an embodiment of the present invention;

Fig. 30 is a plan view of a substrate adapted to be used

with the structure of Fig. 29;

Fig. 31 is a plan view of the reverse side of the substrate of Fig. 30;

Fig. 32 illustrates an embodiment of an LCD module on which the semiconductor device according to the present invention is mounted;

Fig. 33 illustrates a structure for mounting a semiconductor device according to an embodiment of the present invention;

Fig. 34 illustrates a structure for mounting a semiconductor device according to an embodiment of the present invention;

Fig. 35 illustrates a structure for mounting a semiconductor device according to an embodiment of the present invention;

Fig. 36 illustrates an embodiment of an electronic printing apparatus on which the semiconductor device according to the present invention is mounted;

Fig. 37 illustrates an embodiment of an electronic printing apparatus on which the semiconductor device according to the present invention is mounted;

Fig. 38 illustrates a structure for mounting a semiconductor device according to an embodiment of the present invention;

Fig. 39 illustrates a structure for mounting a semiconductor device according to an embodiment of the present invention;

Fig. 40 is a plan view which illustrates a liquid display apparatus according to an embodiment of the present invention;

Fig. 41 illustrates an embodiment of a liquid crystal display apparatus on which the semiconductor device according to the present invention is mounted;

Fig. 42 illustrates a structure for mounting a semiconductor device according to an embodiment of the present invention;

Fig. 43 is an exploded view which illustrates a multi-layer substrate according to an embodiment of the present invention;

Fig. 44 illustrates a state where a semiconductor device is mounted on a multi-layer circuit substrate according to an embodiment of the present invention;

Fig. 45 is a cross-sectional view of the structure shown in Fig. 44;

Fig. 46 illustrates a state where a semiconductor device is mounted on a multi-layer circuit substrate according to an

embodiment of the present invention;

Fig. 47 is a cross-sectional view of the structure shown in Fig. 46;

Fig. 48 illustrates a state where a plurality of semiconductor devices are mounted on a multi-layer circuit substrate according to an embodiment of the present invention;

Fig. 49 is a front elevational view of the structure shown in Fig. 48;

Fig. 50 illustrates a state where a plurality of semiconductor devices are mounted on a multi-layer circuit substrate according to an embodiment of the present invention;

Fig. 51 is a front elevational view of the structure shown in Fig. 50;

Fig. 52 illustrates a state where a plurality of semiconductor devices are mounted on a multi-layer circuit substrate according to an embodiment of the present invention;

Fig. 53 illustrates a state where a plurality of semiconductor devices are mounted on a multi-layer circuit substrate according to an embodiment of the present invention;

Fig. 54 is a front elevational view of the structure shown in Fig. 53;

Fig. 55 illustrates a state where a plurality of semiconductor devices are mounted on a multi-layer circuit substrate according to an embodiment of the present invention;

Fig. 56 is a front elevational view of the structure shown in Fig. 55;

Fig. 57 illustrates a state where a plurality of semiconductor devices are mounted on a multi-layer circuit substrate according to an embodiment of the present invention;

Fig. 58 illustrates a state where multi-layer circuit substrates are mounted on an electronic optical apparatus;

Fig. 59 illustrates a state where multi-layer circuit substrates are mounted on an electronic printing apparatus;

Fig. 60 illustrates a state where multi-layer circuit substrates are mounted on an electronic optical apparatus;

Fig. 61 illustrates a state where multi-layer circuit substrates are mounted on an electronic printing apparatus;

Fig. 62 illustrates a state where multi-layer circuit

substrates are mounted on an electronic optical apparatus;

Fig. 63 illustrates a state where multi-layer circuit substrates are mounted on an electronic printing apparatus;

Fig. 64 illustrates a state where multi-layer circuit substrates are mounted on an electronic optical apparatus;

Fig. 65 illustrates a state where multi-layer circuit substrates are mounted on an electronic printing apparatus;

Fig. 66 illustrates a state where multi-layer circuit substrates are mounted on an electronic optical apparatus;

Fig. 67 illustrates a state where multi-layer circuit substrates are mounted on an electronic printing apparatus;

Fig. 68 illustrates a state where multi-layer circuit substrates are mounted on an electronic optical apparatus;

Fig. 69 illustrates a state where multi-layer circuit substrates are mounted on an electronic printing apparatus;

Fig. 70 illustrates an essential portion of a liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 71 illustrates an essential portion of a liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 72 illustrates an essential portion of a liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 73 is an exploded view which illustrates a multi-layer substrate according to an embodiment of the present invention;

Fig. 74 is a cross sectional view which illustrates an essential portion of a liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 75 illustrates an essential portion of a liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 76 illustrates a liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 77 illustrates a fastening hole of a multi-layer substrate according to another embodiment of the present invention;

Fig. 78 illustrates a fastening hole of a multi-layer

substrate according to another embodiment of the present invention;

Fig. 79 is a perspective view which illustrates another-shape fastening hole of a multi-layer substrate according to another embodiment of the present invention;

Fig. 80 illustrates a liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 81 is a cross sectional view which illustrates a liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 82 illustrates a multi-layer substrate according to another embodiment of the present invention;

Fig. 83 is an perspective view which illustrates a multi-layer substrate according to another embodiment of the present invention;

Fig. 84 illustrates a first layer of the multi-layer substrate according to the embodiment of Fig. 83;

Fig. 85 illustrates a second layer of the multi-layer substrate according to the embodiment of Fig. 83;

Fig. 86 illustrates a third layer of the multi-layer substrate according to the embodiment of Fig. 83;

Fig. 87 illustrates a fourth layer of the multi-layer substrate according to the embodiment of Fig. 83;

Fig. 88 illustrates a fifth layer of the multi-layer substrate according to the embodiment of Fig. 83;

Fig. 89 illustrates a liquid crystal display apparatus according to another embodiment of the present invention;

Fig. 90 illustrates a conventional liquid crystal display apparatus;

Fig. 91 illustrates an essential portion of the conventional liquid crystal display apparatus;

Fig. 92 is a cross sectional view which illustrates an essential portion of the conventional liquid crystal display apparatus;

Fig. 93 is a cross sectional view which illustrates an essential portion of another conventional liquid crystal display apparatus;

Fig. 94 is a cross sectional view which illustrates a

conventional anisotropic conductive film;

Fig. 95 is a cross sectional view which illustrates an essential portion a connection portion of the conventional anisotropic conductive film;

Fig. 96 is a cross sectional view which illustrates an essential portion a connection portion of the conventional anisotropic conductive film;

Fig. 97 is a cross sectional view which illustrates a conventional structure for mounting a semiconductor device and a state where it is mounted on a display device;

Fig. 98 is a cross sectional view which illustrates a conventional structure for mounting a semiconductor device and a state where it is mounted on a display device; and

Fig. 99 is a cross sectional view which illustrates another conventional structure for mounting a semiconductor device and a state where it is mounted on a display device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

A first embodiment of the present invention will now be described with reference to Figs. 1, 2, 3 and 4.

Fig. 1 is an exploded perspective view which illustrates a multi-layer substrate according to the first embodiment of the present invention in which a semiconductor chip for driving liquid crystal is mounted on the surface of a multi-layer substrate by a face-down bonding method.

Reference numerals 1, 2 and 3 represent layers of the multi-layer (comprising three layers) substrate composed of a first layer 1, a second layer 2 and a third layer 3. A semiconductor chip 4 for driving liquid crystal is mounted on the surface of the first layer 1 in the face-down bonding manner by a known method (for example, a method in which an Au bump of the semiconductor is connected to the substrate by using Ag paste or a method in which an anisotropic conductive film is used or a flip chip method in which soldering bump is used). After the semiconductor chip 4 has been bonded as described above, molding members 20 are respectively disposed around the semiconductor chip 4 and between the semiconductor chip 4 and the first layer

1 in order to prevent corrosion and reinforce bonding. The molding members 20 are made of sole epoxy, acryl, urethane or polyester material or a mixture or compound of two or more of these materials in the form of a solvent or thermo-hardening or light hardening type or a mixture thereof. Input lines 5 corresponding to input pads of the semiconductor chip 4 are formed on the surface of the first layer 1 by patterning. The input lines 5 are connected to bus lines 10 of the second layer 2 via through holes 6. Further, lands 7 are formed at the leading portions of the input lines 5 for establishing a wire bonding connection with another multi-layer substrate formed similarly and positioned adjacently.

Output lines 8 corresponding to output pads of the semiconductor chip 4 are formed on the surface of the first layer 1 by patterning. Since the pitch of the terminals of the panel is longer than the pitch of the output pads of the semiconductor chip 4 , the line pattern is widened on the first layer 1 so that the output pads and the terminals of the panel are aligned to one another. Further, through holes 9 are formed at the leading portions of the output lines 8 so that the output lines 8 pass through holes 11 of the second layer 2 and are connected to connection terminals 13 of the panel via through holes 12 of the third layer 3.

Each of the first, second and the third layers 1, 2 and 3 is made of ceramic substrates manufactured by simultaneously sintering alumina bases at low temperature to have a thickness of 0.25 mm. The input lines 5, the output lines 8 and the bus lines 10 are formed by sintering Au, Ag, AgPd or Cu metal paste. Similarly, the through holes 6, 9, 11 and 12 are formed by sintering Au, Ag, AgPd or Cu metal paste. Also the lands 7 and the connection terminals 13 are respectively formed by sintering Au, Ag, AgPd or Cu metal paste. The foregoing elements for each layer are formed by a known print patterning method, and the layers are stacked, sintered and integrated so that forming of the multi-layer substrate is completed. Each of the metal layers formed by patterning and sintering as described above usually has a thickness of about 0.001 mm to about 0.05 mm. The foregoing thickness may be about 0.05 mm to about 0.2 mm in order to reduce

the resistance value.

Depending upon the pitch of the lines and upon the dimension accuracy, the input lines 5, the lands 7, the output lines 8 on the first layer 1 and the connection terminals 13 on the reverse side of the third layer 3 may be formed by photolithographic patterning after the Au, Ag, AgPd or Cu metal paste or a mixture of two or more of these has been printed on the entire surface. In this case, the thickness of the formed pattern is about 0.001 mm to about 0.2 mm. As an alternative to employing the printing method, the pattern may be formed by a photolithographic method or a plating method after Au, Ag or Cu has been evaporated or after the thin film has been formed by sputtering. In this case, the thickness of the formed pattern is about 0.0005 mm to about 0.1 mm.

Since the ceramic substrates subjected to the sintering process exhibit excellent dimension stability against moisture, excellent connection stability can be realized in the portion in which the semiconductor chip 4 and the multi-layer circuit substrate 14 are connected to each other and in the portion in which the connection terminals 13 of the multi-layer circuit substrate 14 and the panel terminals 18 are connected to one another.

Each of the first, second and the third layers 1, 2 and 3 may be made of different materials, for example, a glass epoxy plate made of a composite material of glass fiber and epoxy resin. The thickness of the glass epoxy plate may be about 0.05 mm to about 0.8 mm in place of the employed thickness of 0.1 mm. The input lines 5, the output lines 8, the through holes 10, the lands 7 and the connection terminals 13 for each layer are formed by known sub-tractive method or an additive method in which metal, such as copper, is patterned. The through holes 6, 9, 11 and 12 are, by a known plating method using metal such as copper, formed for each layer or collectively while stacking the layers. Although the thickness of the patterned metal is about 0.001 mm to about 0.035 mm, it may be about 0.035 mm to about 0.2 mm in order to reduce the resistance and to permit large electric currents to flow. The surface of each of the input lines 5, the output lines 8, the bus lines 10, the lands 7, the connection

terminals 13, the through holes 6, 9, 11 and 12 may be applied with plating using sole metal, such as Ni, Au, Cr, Co, Pd, Sn, Pb or In or a mixture of two or more of these materials, plating being performed to have a thickness of about 0.00005 mm to about 0.05 mm. If a glass epoxy plate is used, the thickness can be decreased as compared with the foregoing ceramic substrate. Further, the cost can be reduced because ordinary material and manufacturing process can be employed.

Each of the first, second and the third layers 1, 2 and 3 may be formed by an organic resin film solely made of polyimide (PI), polyethylene terephthalate (PET), polyether sulfon (PES), polycarbonate (PC), polyester (PS), cellulose triacetate (TAC), polysulfon (PS), acryl, epoxy, polyether ether ketone (PEEK) or polyarylate or made of a mixture of two or more of these. Although the polyimide film having a thickness of 0.025 mm is employed as the organic resin film, the thickness of the organic resin film may be about 0.001 mm to about 0.5 mm. The input lines 5, the output lines 8, the bus lines 10, the lands 7 and the connection terminals 13 for each layer are formed by a known sub-tractive method or an additive method in which metal, such as copper, is patterned. The through holes 6, 9, 11 and 12 are formed collectively for each layer or formed after the layers 1, 2 and 3 have been stacked by a known plating method using metal, such as copper. As an alternative to this, a member formed by applying a PI coat (by a known casting method or the like) to metal foil made of, for example, copper, may be patterned and stacked. Although the thickness of the patterned metal is about 0.001 mm to about 0.035 mm, the thickness may be made to be about 0.035 mm to about 0.2 mm in order to reduce the resistance or to permit large electric currents to flow. The surface of each of the lines 5, 8, 10, the lands 7, the connection terminals 13, the through holes 6, 9, 11 and 12 may be applied with plating solely using Ni, Au, Cr, Co, Pd, Sn, Pb or In or using a mixture of two or more of these materials. The thickness of the layers made by plating is about 0.0001 mm to about 0.05 mm. If the organic resin film is used, the thickness can be reduced as compared with the thickness realized by using the ceramic substrate or the epoxy glass plate and the connection between the panel terminal

18 and the connection member 19 can easily be established. Therefore, the connection reliability can be improved and the connection process can be simplified.

Fig. 2 illustrates an example in which the multi-layer substrate according to the first embodiment shown in Fig. 1 is connected to a liquid crystal display panel.

Fig. 3 is an enlarged view which illustrates an essential portion of the connection portion shown in Fig. 2.

Fig. 4 illustrates the cross sectional view of the essential portion of the connection portion shown in Fig. 2.

A light crystal display panel (for example, 640 dots x 480 dots) 16 has 16 multi-layer substrates 14 according to the first embodiment shown in Fig. 1 mounted in direction X and 5 multi-layer substrates 14 in direction Y, the multi-layer substrates 14 thus disposed being connected to the panel terminals 18. However, 12 multi-layer substrates 14 in the direction X and 5 multi-layer substrates 14 in the direction Y are omitted in Fig. 2. The terminals 13 of the multi-layer substrate 14 and the panel terminals 18 are connected to one another by the connection member 19. The connection member 19 establishes electrical connections and somewhat fixes the multi-layer substrate 14 to the panel.

The connection member 19 is made of an anisotropic conductive film mainly composed of conductive particles and an adhesive agent. The conductive particles are sole soldering particles, sole Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these, complex metal particles made by plating, particles formed by plating sole Ni, Co, Pd, Au, Ag, Cu, Fe, Sn or Pb or a mixture of two or more of these materials on plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The foregoing adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials. The anisotropic conductive film is disposed between the panel terminals 18 and the connection terminals 13 of the multi-layer substrate 14. If the anisotropic conductive film is a thermo-hardening film or a blend type of a thermoplastic film and a thermo-hardening film, a heating and pressurizing head

is abutted against the multi-layer substrate 14 so that the anisotropic film is hardened and connected. If the anisotropic conductive film is an ultraviolet hardening type film, a pressuring head is abutted against the multi-layer substrate 14 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminal 18 (adjacent to the glass) to harden the ultraviolet hardening type film.

Alternatively, as the connection member 19, an anisotropic conductive adhesive agent mainly composed of conductive particles and an adhesive agent is used. The conductive particles are sole soldering particles, sole Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these materials, complex metal particles made by plating, particles formed by plating sole Ni, Co, Pd, Au, Ag, Cu, Fe, Sn or Pb or a mixture of two or more of these materials on plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The foregoing adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials. The anisotropic conductive adhesive agent is a fluid or paste agent and applied to the portion in which the panel terminal 16 is connected by a known method, for example, printing or a dispensing method using a dispenser. If the anisotropic conductive adhesive agent is a thermo-hardening agent or a blended agent of a thermoplastic agent and a thermo-hardening agent, a heating and pressuring head is abutted against the multi-layer substrate 14 so that the agent is hardened and connected. If the anisotropic conductive film is an ultraviolet hardening type film, a pressuring head is abutted against the multi-layer substrate 14 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminal 18 (adjacent to the glass) to harden the ultraviolet hardening type film.

In order to protect the exposed portion of the panel terminal 18, a molding 21 is placed. The molding 21 also serves to fix the multi-layer substrate 14 to the panel. The molding 21 is made of sole epoxy, acryl, urethane or polyester material or a mixture or compound of two or more of these materials of any

one of solvent type, thermo-hardening type, or light hardening type or a mixture thereof.

The bus lines between adjacent multi-layer substrates 14 are connected by wire bonding with wires 15 via the lands 7. The wires 15 may be made of metal such as Au, Al or Cu or the like or their alloy (alloy containing Be, Si or Mg or the like included). The width of the wire-bonded portion is so determined as to be narrower than the width of the multi-layer substrate, resulting in that the wire-bonded portion can be mounted in a satisfactorily compact manner in which it is included within the outline of the panel 16.

The connection member 19 may be an anisotropic conductive film arranged as shown in Fig. 21 and mainly composed of conductive particles 32 and an adhesive agent 33. The thickness (h) of the adhesive agent 33 is made thinner than the particle size (d) of the conductive particles 32. The anisotropic conductive film 31 may be formed on a separator 34 (a teflon or a PET sheet (film) or a paper sheet). The conductive particles 32 are, as shown in Fig. 22, sole soldering particles, Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these, complex metal particles made by plating, particles formed by plating sole Ni, Au, Cu or Fe or a mixture of two or more of these materials on plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The particle size (d) is about 0.001 mm to about 0.020 mm. The adhesive agent 27 is sole styrene butadiene styrene (SBS), epoxy, acrylic, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials having a thickness (h) ranging from about 0.0005 mm to about 0.018 mm.

The anisotropic conductive film 31 is disposed between the panel terminal 18 and the connection terminal 13 of the multi-layer substrate 14. If the anisotropic conductive film 31 is a thermo-hardening agent or a blend type of a thermoplastic agent and a thermo-hardening agent, a heating and pressurizing head is abutted against the multi-layer substrate 14 so that the anisotropic adhesive agent is hardened and connected. If the anisotropic conductive film 31 is an ultraviolet hardening type adhesive agent, a pressuring head is abutted against the multi-

layer substrate 14 and ultraviolet rays are applied to the anisotropic conductive adhesive agent from a position adjacent to the panel terminal 18 (adjacent to the glass) to harden and connect the ultraviolet hardening type film. Even if the thickness (k) of the connection terminal 13 of the multi-layer substrate 14 is thinner than the particle size (d) of the conductive particle 32 (in particular, if the pitch of the connection terminals is 0.1 mm or shorter), the adhesive agent 33 can be removed satisfactorily at the time of applying pressure so that the panel terminal 18 and the connection terminal 13 of the multi-layer substrate 14 can be assuredly electrically connected to each other by the conductive particles 32 (see Fig. 10). The thus established connection state is maintained by the adhesive agent 33 so that satisfactory connection reliability is maintained.

Another conductive member may be employed as shown in Fig. 23 which has an arrangement that an anisotropic adhesive agent 35 in the form of fluid or paste including the conductive particles 32 and the adhesive agent 33 is applied to the portion, in which the panel terminal 16 is connected, by a known method, such as a printing method or a dispensing method using a dispenser. At this time, the viscosity and the thixotropic characteristics of the anisotropic conductive agent 35 are so controlled as to make the thickness (h) of the adhesive agent 33 to be smaller than the particle size (d) of the conductive particles 32. As a result, the connection can reliably be established as shown in Fig. 24 by a method similar to that for connecting the foregoing anisotropic conductive film with pressure.

In order to protect the exposed portion of the panel terminal 18 from corrosion, a molding 21 is placed. The molding 21 also serves to fix the multi-layer substrate 14 to the panel. The molding 21 is made of sole epoxy, acryl, urethane or polyester material or a mixture or compound of two or more of these materials of any one of solvent type, thermo-hardening type, or light hardening type or a mixture thereof.

The bus lines between adjacent multi-layer substrates 14 are connected by wire bonding with wires 15 via the lands 7. The wires 15 may be made of metal such as Au, Al or Cu or the like or

their alloy (alloy containing Be, Si or Mg or the like included). The width of the wire-bonded portion is so determined as to be narrower than the width of the multi-layer substrate, resulting in that the wire-bonded portion can be mounted in a satisfactorily compact manner in which it is included within the outline of the panel 16 as shown in Fig. 4.

As described above, use of the multi-layer substrate according to this embodiment enables the lines to be wired in the cross manner in the same multi-layer substrate as contrasted with the conventional TAB method using individual bus substrates to wire the bus lines in the cross manner. Therefore, the overall size can be reduced as compared with the TAB method by raising the density of the lines wired on the substrate. Further, the cost can be reduced because individual bus lines are not used.

Since the conventional COG method has the arrangement that the cross wiring of the bus lines is performed on the panel substrate, a wide area is required to wire the bus lines. Further, metal lines must be used to reduce the resistance value of the wired lines, resulting in an enlargement of the cost. However, use of the multi-layer substrate according to this embodiment enables the space required to wire the bus lines and the cost to be reduced as compared with the COG method.

Second Embodiment

A second embodiment of the present invention will now be described with reference to Fig. 5.

Fig. 5 is an exploded perspective view which illustrates a multi-layer substrate of a liquid crystal display apparatus according to a second embodiment of the present invention in which a semiconductor chip for driving liquid crystal is mounted on the surface of a multi-layer substrate by wire bonding.

Wire bonding lands 22 are, on the surface of the first layer 1 of the multi-layer substrate, formed for the input lines 5 and the output lines 8 to correspond to the input/output pads of the semiconductor chip 4 . The residual factors, such as the pattern, through holes, the method of forming the multi-layer substrate, the arrangement and the structure are the same as those according to the first embodiment.

The reverse side of the semiconductor chip 4 is secured to

the surface of the multi-layer substrate. Further, the input/output pads of the semiconductor chip 4 and the lands 22 on the surface of the first layer 1 of the multi-layer substrate are wire-bonded to one another. Wire 23 for use to connect the multi-layer substrates according to the first embodiment may be used here. Further, the bonded portions and the wired portions are, although omitted from illustration, applied with molding material to be protected and reinforced similarly to the first embodiment.

The bus lines between the adjacent multi-layer substrates are connected by wire bonding similarly to the first embodiment. Further, the bonded portions and the wired portions are, although omitted from illustration, applied with molding material to be protected and reinforced similarly to the first embodiment.

As described above, use of the multi-layer substrate according to this embodiment enables the size and the cost to be reduced similarly to the first embodiment as compared with the conventional TAB method and the COG method.

Third Embodiment

A third embodiment will now be described with reference to Fig. 6.

Fig. 6 illustrates a liquid crystal display apparatus according to the present invention in which the multi-layer substrates 14 having the face-down-bonded semiconductor chips 4 thereon is connected to the panel terminal 18 of the liquid crystal display panel by using the anisotropic conductive film 19 similarly to the first embodiment. The essential portion of the connection portion is arranged to be similar to that according to the first embodiment shown in Fig. 4. However, the leading portions of the input lines of the first layer 1 of the multi-layer substrate are formed into shapes adaptable to be connected to heat seal or flexible substrates in place of the wire bonding lands.

The bus lines of the adjacent multi-layer substrates 14 are connected to one another by using a connection substrate 24. The connection substrate 24 may be a heat seal or a flexible substrate.

The width of the portion, in which the connection substrate

24 is connected, is so determined as to be narrower than the width of the multi-layer substrate 14, resulting in that the wire-bonded portion can be mounted in a satisfactorily compact manner in which it is included within the outline of the panel 16 as shown in Fig. 4.

As described above, use of the multi-layer substrate according to this embodiment enables the size and the cost to be reduced similarly to the first embodiment as compared with the conventional TAB method and the COG method.

Further, the connection of the semiconductor chip for driving liquid crystal to the surface of the multi-layer substrate and the electrical connection between the adjacent multi-layer substrates may be established by combining the methods according to first, second and the third embodiments. In any case, the size and the cost can be reduced similarly.

Further, the multi-layer substrate having the semiconductor chip for use in the foregoing embodiments mounted thereon can be mounted on another display apparatus or an electronic printing apparatus such that it can be mounted on a plasma display or an EL display apparatus by changing the foregoing semiconductor chip to a semiconductor chip for driving the plasma display or a semiconductor chip for driving the EL. By similarly mounting a semiconductor chip for driving a thermal head on the multi-layer substrate and by similarly connecting the multi-layer substrate to the thermal head, application to an electronic printing apparatus can be realized.

Fourth Embodiment

A fourth embodiment will now be described with reference to Figs. 4, 7, 8, 9 and 10.

Fig. 7 is an exploded perspective view which illustrates a liquid crystal display apparatus according to the present invention in which a multi-layer substrate according to this embodiment includes a semiconductor chip for driving liquid crystal face-down bonded thereon.

Reference numerals 1, 2 and 3 represent layers of the multi-layer (comprising three layers) substrate composed of a first layer 1, a second layer 2 and a third layer 3. A semiconductor chip 4 for driving liquid crystal is mounted on the surface of

the first layer 1 in the face-down bonding manner by a known method (for example, a method in which an Au bump of the semiconductor is connected to the substrate by using Ag paste or a method in which an anisotropic conductive film is used or a flip chip method in which soldering is performed). After the semiconductor chip 4 has been bonded as described above, molding members 20 are respectively disposed around the semiconductor chip 4 and between the semiconductor chip 4 and the first layer 1 in order to prevent corrosion and reinforce bonding. The molding members 20 are made of sole epoxy, acryl, urethane or polyester material or a mixture or compound of two or more of these materials in the form of a solvent or thermo-hardening or light hardening type or a mixture thereof. Input lines 5 corresponding to input pads of the semiconductor chip 4 are formed on the surface of the first layer 1 by patterning. The input lines 5 are connected to bus lines 10 of the second layer 2 via through holes 6 and through holes 25. Further, the input lines 5 are connected to the connection terminals 27 formed on the reverse side of the third layer 3 via the through holes 26 formed in the third layer 3. The connection terminals 27 are respectively formed into a proper shape to have a proper size and a thickness to be connected to the connection terminals 29 of the bus lines 28 on the panel. The connection terminals 27 are disposed on the side of the multi-layer substrate 14 perpendicular to the side on which the connection terminals 13 for establishing the connection with the panel are disposed. Although the illustrated structure comprises the connection terminals 27 disposed in a line, a two-line configuration may be employed.

Output lines 8 corresponding to output pads of the semiconductor chip 4 are formed on the surface of the first layer 1 by patterning. Since the pitch of the terminals of the panel is longer than the pitch of the output pads of the semiconductor chip 4 , the line pattern is widened on the first layer 1 so that the output pads and the terminals of the panel are aligned to one another. Further, through holes 9 are formed at the leading portions of the output lines 8 so that the output lines 8 pass through the through holes 11 of the second layer 2

and are connected to connection terminals 13 of the panel via through holes 12 of the third layer 3. Although a method of making coinciding the pitch of the pads of the semiconductor chip with the pitch of the terminals of the panel of the multi-layer substrate composed of the three layers is described here, the coincidence may be made over a plurality of layers (two or more layers) in place of making only one layer coincide.

Each of the first, second and the third layers 1, 2 and 3 is made of ceramic substrates manufactured by simultaneously sintering alumina bases at low temperature to have a thickness of 0.25 mm. The input lines 5, the output lines 8 and the bus lines 10 are formed by sintering solely or mixture of Au, Ag, AgPd or Cu metal paste. Similarly, the through holes 6, 9, 11, 12, 25 and 26 are formed by sintering Au, Ag, AgPd or Cu metal paste. Also the connection terminals 13 and 27 are respectively formed by sintering solely Au, Ag, AgPd or Cu metal paste or a mixture of two or more of these. The foregoing elements for each layer are formed by a known print patterning method, and the layers are stacked sintered and integrated so that forming of the multi-layer substrate is completed. Each of the metal layers formed by patterning and sintering as described above usually has a thickness of about 0.001 mm to about 0.05 mm. The foregoing thickness may be about 0.05 mm to about 0.2 mm in order to reduce the resistance value.

Depending upon the pitch of the lines and upon the dimension accuracy, the input lines 5 and the output lines 8 on the surface of the first layer 1 and the connection terminals 13 and 27 on the third layer 3 may be formed by photolithographic patterning after the Au, Ag, AgPd or Cu metal paste or a mixture paste of two or more of these materials has been printed on the entire surface. In this case, the thickness of the formed pattern is about 0.001 mm to about 0.2 mm. As an alternative to employing the printing method, the pattern may be formed by a photolithographic method or a plating method after Au, Ag or Cu has been evaporated or after the thin film has been formed by sputtering. In this case, the thickness of the formed pattern is about 0.0005 mm to about 0.1 mm.

Fig. 8 is an exploded view which illustrates an essential

portion in which the multi-layer substrate according to this embodiment shown in Fig. 7 is connected to the liquid crystal display panel. The cross section (section x-x of Fig. 8) of the essential portion of the connection portion is as shown in Fig. 4 similarly to the first embodiment. Connection terminals 18, bus lines 28 and connection terminals 29 to be disposed at the end portions of the bus lines 28 are, by patterning, formed on the panel 16 to correspond to the portion in which the multi-layer substrate 14 will be mounted. Although a straight-line pattern is formed in the structure shown in Fig. 8, the pattern may be formed fully in an allowable area in terms of wiring if the resistance of the circuit and that of the connections are intended to be reduced. The bus lines 28 on the panel serve as bus lines for establishing the connections between the foregoing multi-layer substrates.

Fig. 9 illustrates a structure arranged substantially similarly to that according to the embodiment shown in Fig. 8 except for an arrangement in which the connection terminals 13 of the multi-layer substrate 14 are disposed inside the panel 16. The cross section (section y-y of Fig. 9) of the essential portion of the connection portion is as shown in Fig. 10 whereby the length of each of lines arranged from the panel terminals 18 to the inside portion of the panel can be shorter than that according to the embodiment shown in Fig. 4. As a result, an effect can be obtained in that the circuit resistance can be reduced.

The connection terminals 13, the panel terminals 18, the connection terminals 27 and the panel terminals 28 are connected to one another by connection members 19. The connection members 19 maintain the electrical connections and also act to fix somewhat the multi-layer substrates 14 to the panel.

The connection member 19 is made of an anisotropic conductive film mainly composed of conductive particles and an adhesive agent. The conductive particles are sole soldering particles, sole Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these, complex metal particles made by plating, particles formed by plating sole Ni, Co, Pd, Au, Ag, Cu, Fe, Sn or Pb or a mixture of two or more of these materials on

plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The foregoing adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials. The anisotropic conductive film is disposed between the panel terminals 18 and the connection terminals 13 and 27 of the multi-layer substrate 14. If the anisotropic conductive film is a thermo-hardening film or a blend type of a thermoplastic film and a thermo-hardening film, a heating and pressurizing head is abutted against the multi-layer substrate 14 so that the anisotropic film is hardened and connected. If the anisotropic conductive film is an ultraviolet hardening type film, a pressuring head is abutted against the multi-layer substrate 14 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminals 18 and 29 (adjacent to the glass) to harden the ultraviolet hardening type film. If the pressuring head is formed into a U-shape facing sidewards or if a multiplicity of the pressuring heads are used to correspond to the configuration of the connection terminals 13 and 27, the input/output terminals of the multi-layer substrate 14 can be collectively connected to the corresponding panel terminals 18 and 29 while necessitating only one pressurizing process.

Alternatively, as the connection member 19, an anisotropic conductive adhesive agent is used which is mainly composed of conductive particles and an adhesive agent. The conductive particles are sole soldering particles, sole Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these materials, complex metal particles made by plating, particles formed by plating sole Ni, Co, Pd, Au, Ag, Cu, Fe, Sn or Pb or a mixture of two or more of these materials on plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The foregoing adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials. The anisotropic conductive adhesive agent is a fluid or paste agent and applied to the portion in which the panel terminal 16 is connected by a known method, for example, printing

or a dispensing method using a dispenser. If the anisotropic conductive adhesive agent is a thermo-hardening agent or a blended agent of a thermoplastic agent and a thermo-hardening agent, a heating and pressuring head is abutted against the multi-layer substrate 14 so that the agent is hardened and connected. If the anisotropic conductive adhesive agent is an ultraviolet hardening type adhesive agent, a pressuring head is abutted against the multi-layer substrate 14 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminals 18 and 19 (adjacent to the glass) to harden the ultraviolet hardening type film. If the pressuring head is formed into a U-shape facing sidewards or if a multiplicity of the pressuring heads are used to correspond to the configuration of the connection terminals 13 and 27, the input/output terminals of the multi-layer substrate 14 can be collectively connected to the corresponding panel terminals 18 and 29 while necessitating only one pressurizing process.

In order to protect the exposed portion of the panel terminal 18 from corrosion, a molding 21 is placed. The molding 21 also serves to fix the multi-layer substrate 14 to the panel. The molding 21 is made of sole epoxy, acryl, urethane or polyester material or a mixture or compound of two or more of these materials of any one of solvent type, thermo-hardening type, or light hardening type or a mixture thereof.

As shown in Fig. 4, the multi-layer substrate can be mounted in a compact manner within the outline of the panel 16.

As described above, the bus lines formed on the panel to serves as the means for establishing the electrical connections between the multi-layer substrates enables the bus lines to be formed simultaneously with the other lines on the panel. Therefore, an individual forming process does not need to be performed. Further, individual elements such as the heat seal can be omitted. In addition, the fact that the connections of the input and output terminals can be collectively established causes the manufacturing process to be simplified.

Fifth Embodiment

A fifth embodiment will now be described with reference to Figs. 4, 10, 11, 12, 13 and 14.

Fig. 11 is an exploded perspective view which illustrates a liquid crystal display apparatus according to the present invention in which a multi-layer substrate according to this embodiment includes a semiconductor chip for driving liquid crystal face-down bonded thereon.

Reference numerals 1, 2 and 3 represent layers of the multi-layer (comprising three layers) substrate composed of a first layer 1, a second layer 2 and a third layer 3. A semiconductor chip 4 for driving liquid crystal is mounted on the surface of the first layer 1 in the face-down bonding manner by a known method (for example, a method in which an Au bump of the semiconductor is connected to the substrate by using Ag paste or a method in which an anisotropic conductive film is used or a flip chip method in which soldering is performed). After the semiconductor chip 4 has been bonded as described above, molding members 20 are respectively disposed around the semiconductor chip 4 and between the semiconductor chip 4 and the first layer 1 in order to prevent corrosion and reinforce bonding. The molding members 20 are made of sole epoxy, acryl, urethane or polyester material or a mixture or compound of two or more of these materials in the form of a solvent or thermo-hardening or light hardening type or a mixture thereof. Input lines 5 corresponding to input pads of the semiconductor chip 4 are formed on the surface of the first layer 1 by patterning. The input lines 5 are connected to bus lines 10 of the second layer 2 via through holes 6 and through holes 25. The bus lines 10 are connected to through holes 30 of the second layer 2 and connected to the connection terminals 27 formed on the reverse side of the third layer 3 via the through holes 30 and the through holes 26 of the second layer 2. The connection terminals 27 are disposed to substantially run parallel to the connection terminals 13. The connection terminals 27 and the connection terminals 13 are formed into the same shape, have the same size and thickness. Although Fig. 11 illustrates the structure in which the connection terminals 13 and 27 respectively have the same shape and are disposed at the same pitch, the connection terminals 13 and 27 may be respectively different from one another. Although the through holes 13 and 26 are disposed in one line, they may be

disposed to form plural lines.

Output lines 8 corresponding to output pads of the semiconductor chip 4 are formed on the surface of the first layer 1 by patterning. Since the pitch of the terminals of the panel is longer than the pitch of the output pads of the semiconductor chip 4 , the line pattern is widened on the first layer 1 so that the output pads and the terminals of the panel are aligned to one another. Further, through holes 9 are formed at the leading portions of the output lines 8 so that the output lines 8 pass through the through holes 11 of the second layer 2 and and connected to connection terminals 13 of the panel via through holes 12 of the third layer 3. Although a method of making coinciding the pitch of the pads of the semiconductor chip with the pitch of the terminals of the panel of the multi-layer substrate composed of the three layers is described here, the coincidence may be made over a plurality of layers (two or more layers) in place of making only one layer coincide.

Each of the first, second and the third layers 1, 2 and 3 is made of ceramic substrates manufactured by simultaneously sintering alumina bases at low temperature to have a thickness of 0.25 mm. The input lines 5, the output lines 8 and the bus lines 10 are formed by sintering solely or mixture of Au, Ag, AgPd or Cu metal paste. Similarly, the through holes 6, 9, 11, 12, 25, 26 and 30 are formed by sintering Au, Ag, AgPd or Cu metal paste. Also the connection terminals 13 and 27 are respectively formed by sintering solely Au, Ag, AgPd or Cu metal paste or a mixture of two or more of these. The foregoing elements for each layer are formed by a known print patterning method, and the layers are stacked sintered and integrated so that forming of the multi-layer substrate is completed. Each of the metal layers formed by patterning and sintering as described above usually has a thickness of about 0.001 mm to about 0.05 mm. The foregoing thickness may be about 0.05 mm to about 0.2 mm in order to reduce the resistance value.

Depending upon the pitch of the lines and upon the dimension accuracy, the input lines 5 and the output lines 8 on the surface of the first layer 1 and the connection terminals 13 and 27 on the third layer 3 may be formed by photolithographic patterning

after the Au, Ag, AgPd or Cu metal paste or a mixture paste of two or more of these materials has been printed on the entire surface. In this case, the thickness of the formed pattern is about 0.001 mm to about 0.2 mm. As an alternative to employing the printing method, the pattern may be formed by a photolithographic method or a plating method after Au, Ag or Cu has been evaporated or after the thin film has been formed by sputtering. In this case, the thickness of the formed pattern is about 0.0005 mm to about 0.1 mm.

Fig. 12 is an exploded view which illustrates an essential portion in which the multi-layer substrate according to this embodiment shown in Fig. 7 is connected to the liquid crystal display panel. The cross section (section x-x of Fig. 12) of the essential portion of the connection portion is as shown in Fig. 4 similarly to the first embodiment. Connection terminals 18, bus lines 28 and connection terminals 29 to be disposed at the end portions of the bus lines 28 are, by patterning, formed on the panel 16 to correspond to the portion in which the multi-layer substrate 14 will be mounted. The connection terminals 18 and 29 are disposed on one straight line. Although the bus lines 28 are simply illustrated by a continuous line in Fig. 12, they may be arranged to have different pattern widths upon consideration of the circuit resistance and the connection resistance so that the resistance values of the lines are made to be the same. The bus lines 28 on the panel serve as bus lines for establishing the connections between the foregoing multi-layer substrates.

The connection terminals 13, the panel terminals 18, the connection terminals 27 and the panel terminals 28 of the multi-layer substrate 14 are connected to one another by connection members 19. The connection members 19 maintain the electrical connections and also act to fix somewhat the multi-layer substrates 14 to the panel.

The connection member 19 is made of an anisotropic conductive film mainly composed of conductive particles and an adhesive agent. The conductive particles are sole soldering particles, sole Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these, complex metal particles made by

plating, particles formed by plating sole Ni, Co, Pd, Au, Ag, Cu, Fe, Sn or Pb or a mixture of two or more of these materials on plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The foregoing adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials. The anisotropic conductive film is disposed between the panel terminals 18 and the connection terminals 13 and 27 of the multi-layer substrate 14. If the anisotropic conductive film is a thermo-hardening film or a blend type of a thermoplastic film and a thermo-hardening film, a heating and pressurizing head is abutted against the multi-layer substrate 14 so that the anisotropic film is hardened and connected. If the anisotropic conductive film is an ultraviolet hardening type film, a pressuring head is abutted against the multi-layer substrate 14 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminals 18 and 29 (adjacent to the glass) to harden the ultraviolet hardening type film. Since the connection terminals 13 and 27 are disposed on one straight line, the pressurizing head may be formed into a simple straight shape so that the connections can be established by using a simple pressurizing and connecting device. Further, the input/output terminals of the multi-layer substrate 14 can be collectively connected to the corresponding panel terminals 18 and 29 while necessitating only one pressurizing process.

Alternatively, as the connection member 19, an anisotropic conductive adhesive agent is used which is mainly composed of conductive particles and an adhesive agent. The conductive particles are sole soldering particles, sole Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these, complex metal particles made by plating, particles formed by plating sole Ni, Co, Pd, Au, Ag, Cu, Fe, Sn or Pb or a mixture of two or more of these materilas on plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The foregoing adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials. The

anisotropic conductive adhesive agent is a fluid or paste agent and applied to the portion in which the panel terminal 16 is connected by a known method, for example, printing or a dispensing method using a dispenser. If the anisotropic conductive adhesive agent is a thermo-hardening agent or a blended agent of a thermoplastic agent and a thermo-hardening agent, a heating and pressuring head is abutted against the multi-layer substrate 14 so that the agent is hardened and connected. If the anisotropic conductive adhesive agent is an ultraviolet hardening type adhesive agent, a pressuring head is abutted against the multi-layer substrate 14 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminals 18 and 19 (adjacent to the glass) to harden the ultraviolet hardening type film. Since the connection terminals 13 and 27 are disposed on one straight line, the pressurizing head may be formed into a simple straight shape so that the connections can be established by using a simple pressurizing and connecting device. Further, the input/output terminals of the multi-layer substrate 14 can be collectively connected to the corresponding panel terminals 18 and 29 while necessitating only one pressurizing process.

In order to protect the exposed portion of the panel terminals 18, 28 and 29 from corrosion, a molding 21 is placed. The molding 21 also serves to fix the multi-layer substrate 14 to the panel. The molding 21 is made of sole epoxy, acryl, urethane or polyester material or a mixture or compound of two or more of these materials of any one of solvent type, thermo-hardening type, or light hardening type or a mixture thereof.

As shown in Fig. 4, the multi-layer substrate can be mounted in a compact manner within the outline of the panel 16.

As described above, the bus lines formed on the panel to serves as the means for establishing the electrical connections between the multi-layer substrates enables the bus lines to be formed simultaneously with the other lines on the panel. Therefore, an individual forming process does not need to be performed. Further, individual elements such as the heat seal can be omitted. In addition, the fact that the connections of the input and output terminals can be collectively established

causes the manufacturing process to be simplified.

Fig. 13 illustrates a structure arranged substantially similarly to that according to the embodiment shown in Fig. 12 except for an arrangement in which the connection terminals 13 of the multi-layer substrate 14 are disposed inside the panel 16. The cross section (section Y-Y of Fig. 13) of the essential portion of the connection portion is as shown in Fig. 10 whereby the length of each of lines arranged from the panel terminals 18 to the inside portion of the panel can be shorter than that according to the embodiment shown in Fig. 4. As a result, an effect can be obtained in that the circuit resistance can be reduced.

The connection terminals 13, the panel terminals 18, the connection terminals 27 and the panel terminals 28 of the multi-layer substrate 14 are connected to one another by connection members 19. The connection members 19 maintain the electrical connections and also act to fix somewhat the multi-layer substrates 14 to the panel.

The connection member 19 is made of an anisotropic conductive film mainly composed of conductive particles and an adhesive agent. The conductive particles are sole soldering particles, sole Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these, complex metal particles made by plating, particles formed by plating sole Ni, Co, Pd, Au, Ag, Cu, Fe, Sn or Pb or a mixture of two or more of these materials on plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The foregoing adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials. The anisotropic conductive film is disposed between the panel terminals 18 and the connection terminals 13 and 27 of the multi-layer substrate 14. If the anisotropic conductive film is a thermo-hardening film or a blend type of a thermoplastic film and a thermo-hardening film, a heating and pressurizing head is abutted against the multi-layer substrate 14 so that the anisotropic film is hardened and connected. If the anisotropic conductive film is an ultraviolet hardening type film, a pressuring head is abutted against the multi-layer

substrate 14 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminals 18 and 29 (adjacent to the glass) to harden the ultraviolet hardening type film. Since the connection terminals 13 and 27 are disposed on one straight line, the pressurizing head may be formed into a simple straight shape so that the connections can be established by using a simple pressurizing and connecting device. Further, the input/output terminals of the multi-layer substrate 14 can be collectively connected to the corresponding panel terminals 18 and 29 while necessitating only one pressurizing process.

Alternatively, as the connection member 19, an anisotropic conductive adhesive agent is used which is mainly composed of conductive particles and an adhesive agent. The conductive particles are sole soldering particles, sole Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these, complex metal particles made by plating, particles formed by plating sole Ni, Co, Pd, Au, Ag, Cu, Fe, Sn or Pb or a mixture of two or more of these materials on plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The foregoing adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials. The anisotropic conductive adhesive agent is a fluid or paste agent and applied to the portion in which the panel terminal 16 is connected by a known method, for example, printing or a dispensing method using a dispenser. If the anisotropic conductive adhesive agent is a thermo-hardening agent or a blended agent of a thermoplastic agent and a thermo-hardening agent, a heating and pressuring head is abutted against the multi-layer substrate 14 so that the agent is hardened and connected. If the anisotropic conductive adhesive agent is an ultraviolet hardening type adhesive agent, a pressuring head is abutted against the multi-layer substrate 14 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminals 18 and 19 (adjacent to the glass) to harden the ultraviolet hardening type film. Since the connection terminals 13 and 27 are disposed on one straight line,

the pressurizing head may be formed into a simple straight shape so that the connections can be established by using a simple pressurizing and connecting device. Further, the input/output terminals of the multi-layer substrate 14 can be collectively connected to the corresponding panel terminals 18 and 29 while necessitating only one pressurizing process.

In order to protect the exposed portion of the panel terminals 18, 28 and 29 from corrosion, a molding 21 is placed. The molding 21 also serves to fix the multi-layer substrate 14 to the panel. The molding 21 is made of sole epoxy, acryl, urethane or polyester material or a mixture or compound of two or more of these materilas of any one of solvent type, thermo-hardening type, or light hardening type or a mixture thereof.

As shown in Fig. 10, the multi-layer substrate can be mounted in a compact manner within the outline of the panel 16.

As described above, the bus lines formed on the panel to serves as the means for establishing the electrical connections between the multi-layer substrates enables the bus lines to be formed simultaneously with the other lines on the panel. Therefore, an individual forming process does not need to be performed. Further, individual elements such as the heat seal can be omitted. In addition, the fact that the connections of the input and output terminals can be collectively established causes the manufacturing process to be simplified.

Fig. 14 illustrates a structure arranged similarly to that according to the embodiment shown in Fig. 12 except for an arrangement that the bus lines 28 on the panel are also disposed in an area in the panel that does not affect the display n addition to the area on which the multi-layer substrate 13 will be mounted. Therefore, the area that can be used to form the bus lines 28 can be widened, the width of the bus lines can be enlarged to reduce the circuit resistance while eliminating a necessity of enlarging the area required to mount the multi-layer substrates 14. The reduction in the resistance value of the bus lines enables an effect to be obtained in that the quality of display made by the liquid crystal display apparatus can be improved. The cross section (section Z-Z of Fig. 14) of the essential portion of the connection portion is as shown in Fig.

10. As shown in the drawing, a liquid crystal display apparatus can be provided in which the area required to mount the multi-layer substrate 14 can further be reduced and which exhibits excellent quality of display.

The connection terminals 13, the panel terminals 18, the connection terminals 27 and the panel terminals 28 of the multi-layer substrate 14 are connected to one another by connection members 19. The connection members 19 maintain the electrical connections and also act to fix somewhat the multi-layer substrates 14 to the panel.

The connection member 19 is made of an anisotropic conductive film mainly composed of conductive particles and an adhesive agent. The conductive particles are sole soldering particles, sole Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these, complex metal particles made by plating, particles formed by plating sole Ni, Co, Pd, Au, Ag, Cu, Fe, Sn or Pb or a mixture of two or more of these materials on plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The foregoing adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials. The anisotropic conductive film is disposed between the panel terminals 18 and the connection terminals 13 and 27 of the multi-layer substrate 14. If the anisotropic conductive film is a thermo-hardening film or a blend type of a thermoplastic film and a thermo-hardening film, a heating and pressurizing head is abutted against the multi-layer substrate 14 so that the anisotropic film is hardened and connected. If the anisotropic conductive film is an ultraviolet hardening type film, a pressuring head is abutted against the multi-layer substrate 14 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminals 18 and 29 (adjacent to the glass) to harden the ultraviolet hardening type film. Since the connection terminals 13 and 27 are disposed on one straight line, the pressurizing head may be formed into a simple straight shape so that the connections can be established by using a simple pressurizing and connecting device. Further, the input/output terminals of the multi-layer

substrate 14 can be collectively connected to the corresponding panel terminals 18 and 29 while necessitating only one pressurizing process.

Alternatively, as the connection member 19, an anisotropic conductive adhesive agent is used which is mainly composed of conductive particles and an adhesive agent. The conductive particles are sole soldering particles, sole Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these, complex metal particles made by plating, particles formed by plating sole Ni, Co, Pd, Au, Ag, Cu, Fe, Sn or Pb or a mixture of two or more of these materials on plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The foregoing adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials. The anisotropic conductive adhesive agent is a fluid or paste agent and applied to the portion in which the panel terminal 16 is connected by a known method, for example, printing or a dispensing method using a dispenser. If the anisotropic conductive adhesive agent is a thermo-hardening agent or a blended agent of a thermoplastic agent and a thermo-hardening agent, a heating and pressuring head is abutted against the multi-layer substrate 14 so that the agent is hardened and connected. If the anisotropic conductive adhesive agent is an ultraviolet hardening type adhesive agent, a pressuring head is abutted against the multi-layer substrate 14 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminals 18 and 19 (adjacent to the glass) to harden the ultraviolet hardening type film. Since the connection terminals 13 and 27 are disposed on one straight line, the pressurizing head may be formed into a simple straight shape so that the connections can be established by using a simple pressurizing and connecting device. Further, the input/output terminals of the multi-layer substrate 14 can be collectively connected to the corresponding panel terminals 18 and 29 while necessitating only one pressurizing process.

In order to protect the exposed portion of the panel terminals 18, 28 and 29 from corrosion, a molding 21 is placed.

The molding 21 also serves to fix the multi-layer substrate 14 to the panel. The molding 21 is made of sole epoxy, acryl, urethane or polyester material or a mixture or compound of two or more of these materials of any one of solvent type, thermo-hardening type, or light hardening type or a mixture thereof.

As shown in Fig. 10, the multi-layer substrate can be mounted in a compact manner within the outline of the panel 16.

As described above, the bus lines formed on the panel to serves as the means for establishing the electrical connections between the multi-layer substrates enables the bus lines to be formed simultaneously with the other lines on the panel. Therefore, an individual forming process does not need to be performed. Further, individual elements such as the heat seal can be omitted. In addition, the fact that the connections of the input and output terminals can be collectively established causes the manufacturing process to be simplified. Therefore, a liquid crystal display apparatus, the cost of which can further be reduced, can be provided.

As described above, use of the multi-layer substrate according to this embodiment enables the lines to be wired in the cross manner in the same multi-layer substrate as contrasted with the conventional TAB method using individual bus substrate to wire the bus lines in the cross manner. Therefore, the overall size can be reduced as compared with the TAB method by raising the density of the lines wired on the substrate. Further, the cost can be reduced because individual bus lines are not used.

Since the conventional COG method has the arrangement that the cross wiring of the bus lines is performed on the panel substrate, a wide area is required to wire the bus lines. Further, metal lines must be used to reduce the resistance value of the wired lines, resulting in an enlargement of the cost. However, use of the multi-layer substrate according to this embodiment enables the space required to wire the bus lines and the cost to be reduced as compared with the COG method.

Sixth Embodiment

A sixth embodiment of the present invention will now be described with reference to Figs. 15, 16, 17 and 18.

Fig. 15 is an exploded perspective view which illustrates a

multi-layer substrate according to this embodiment which includes two semiconductor chips for driving liquid crystal face-down bonded thereon.

Reference numerals 1, 2 and 3 represent layers of the multi-layer (comprising three layers) substrate composed of a first layer 1, a second layer 2 and a third layer 3. Semiconductor chips 4 and 4' for driving liquid crystal are mounted on the surface of the first layer 1 in the face-down bonding manner by a known method (for example, a method in which an Au bump of the semiconductor is connected to the substrate by using Ag paste or a method in which an anisotropic conductive film is used or a flip chip method in which soldering is performed). After the semiconductor chips 4 and 4' have been bonded as described above, molding members 20 are respectively disposed around the semiconductor chips 4 and 4' and between the semiconductor chips 4 and 4' and the first layer 1 in order to prevent corrosion and reinforce bonding. The molding members 20 are made of sole epoxy, acryl, urethane or polyester material or a mixture or compound of two or more of these materilas in the form of a solvent or thermo-hardening or light hardening type or a mixture thereof. Input lines 5 and 5' corresponding to input pads of the semiconductor chip 4 and 4' are formed on the surface of the first layer 1 by patterning. The input lines 5 and 5' are connected to bus lines 10 of the second layer 2 via through holes 6. Further, lands 7 are formed at the leading portions of the input lines 5 and 5' for wire-bonding with another multi-layer substrate arranged similarly.

Output lines 8 and 8' corresponding to output pads of the semiconductor chips 4 and 4' are formed on the surface of the first layer 1 by patterning. Since the pitch of the terminals of the panel is longer than the pitch of the output pads of the semiconductor chips 4 and 4' , the line pattern is widened on the first layer 1 so that the output pads and the terminals of the panel are aligned to one another. Further, through holes 9 are formed at the leading portions of the output lines 8 and 8' so that the output lines 8 and 8' pass through the through holes 11 of the second layer 2 and are connected to connection terminals 13 of the panel via through holes 12 of the third layer 3.

Each of the first, second and the third layers 1, 2 and 3 is made of ceramic substrates manufactured by simultaneously sintering alumina bases at low temperature to have a thickness of 0.25 mm. The input lines 5 and 5', the output lines 8 and 8' and the bus lines 10 are formed by sintering solely or mixture of Au, Ag, AgPd or Cu metal paste. Similarly, the through holes 6, 9, 11 and 12 are formed by sintering Au, Ag, AgPd or Cu metal paste. Also lands 7 and the connection terminals 13 are respectively formed by sintering solely Au, Ag, AgPd or Cu metal paste or a mixture of two or more of these. The foregoing elements for each layer are formed by a known print patterning method, and the layers are stacked sintered and integrated so that forming of the multi-layer substrate is completed. Each of the metal layers formed by patterning and sintering as described above usually has a thickness of about 0.001 mm to about 0.05 mm. The foregoing thickness may be about 0.05 mm to about 0.2 mm in order to reduce the resistance value.

Depending upon the pitch of the lines and upon the dimension accuracy, the input lines 5 and 5', the lands 7, the output lines 8 and 8' on the first layer and connection terminals 13 on the reverse side of the third layer 3 may be formed by photolithographic patterning after the Au, Ag, AgPd or Cu metal paste or a mixture paste of two or more of these has been printed on the entire surface. In this case, the thickness of the formed pattern is about 0.001 mm to about 0.2 mm. As an alternative to employing the printing method, the pattern may be formed by a photolithographic method or a plating method after Au, Ag or Cu has been evaporated or after the thin film has been formed by sputtering. In this case, the thickness of the formed pattern is about 0.0005 mm to about 0.1 mm.

The arrangement in which the two semiconductor chips for driving liquid crystal are bonded on one multi-layer substrate enables the input/output lines to be wired efficiently as compared with an arrangement in which one semiconductor chip for driving liquid crystal on one multi-layer substrate. Further, the semiconductor chips can be disposed efficiently. Therefore, the required area for the multi-layer substrate can be reduced and, accordingly, the parts cost can be reduced. Further, the

process for exploding (dicing or breaking) the multi-layer substrate and the process for setting/resetting the multi-layer substrate for bonding and molding the semiconductor chip can also be simplified. Therefore, the cost can be reduced.

Fig. 16 illustrates an embodiment in which the multi-layer substrate according to an embodiment shown in Fig. 15 is connected to a liquid crystal display panel.

Fig. 17 is an enlarged view which illustrates an essential portion of the connection portion.

Fig. 18 illustrates the cross section of an essential portion of the connection portion.

A liquid crystal display panel (for example, 640 x 480 dot display) 16 has a panel terminal 18 to which 8 multi-layer substrates 14 according to the embodiment shown in Fig. 1 are connected on the direction X thereof and 5 multi-layer substrates 14 on the direction Y thereof. However, four multi-layer substrates 14 on the direction X and five multi-layer substrates 14 on the direction Y are not shown in Fig. 16. The conductive member 19 maintains the electrical connection and also fix somewhat the multi-layer substrate 14 to the panel.

The connection member 19 is made of an anisotropic conductive film mainly composed of conductive particles and an adhesive agent. The conductive particles are sole soldering particles, sole Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these, complex metal particles made by plating, particles formed by plating sole Ni, Co, Pd, Au, Ag, Cu, Fe, Sn or Pb or a mixture of two or more of these materials on plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The foregoing adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials. The anisotropic conductive film is disposed between the panel terminals 18 and the connection terminals 13 of the multi-layer substrate 14. If the anisotropic conductive film is a thermo-hardening film or a blend type of a thermoplastic film and a thermo-hardening film, a heating and pressurizing head is abutted against the multi-layer substrate 14 so that the anisotropic film is hardened and connected. If the anisotropic

conductive film is an ultraviolet hardening type film, a pressuring head is abutted against the multi-layer substrate 14 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminals 18 (adjacent to the glass) to harden the ultraviolet hardening type film.

Alternatively, as the connection member 19, an anisotropic conductive adhesive agent is used which is mainly composed of conductive particles and an adhesive agent. The conductive particles are sole soldering particles, sole Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these, complex metal particles made by plating, particles formed by plating sole Ni, Co, Pd, Au, Ag, Cu, Fe, Sn or Pb or a mixture of two or more of these materials on plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The foregoing adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials. The anisotropic conductive adhesive agent is a fluid or paste agent and applied to the portion in which the panel terminal 16 is connected by a known method, for example, printing or a dispensing method using a dispenser. If the anisotropic conductive adhesive agent is a thermo-hardening agent or a blended agent of a thermoplastic agent and a thermo-hardening agent, a heating and pressuring head is abutted against the multi-layer substrate 14 so that the agent is hardened and connected. If the anisotropic conductive adhesive agent is an ultraviolet hardening type adhesive agent, a pressuring head is abutted against the multi-layer substrate 14 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminals 18 (adjacent to the glass) to harden the ultraviolet hardening type film.

In order to protect the exposed portion of the panel terminals 18 from corrosion, a molding 21 is placed. The molding 21 also serves to fix the multi-layer substrate 14 to the panel. The molding 21 is made of sole epoxy, acryl, urethane or polyester material or a mixture or compound of two or more of these materials of any one of solvent type, thermo-hardening type, or light hardening type or a mixture thereof.

The bus lines between the adjacent multi-layer substrates 14 are connected by wire bonding performed by using wires 15 via the lands 7. The wires 15 are made of metal, such as Au, Al, or Cu or the like or their alloy (alloy containing Be, Si or Mg or the like included). The width of the portion to be wire-bonded is narrower than the width of the multi-layer substrate so that the multi-layer substrate is mounted within the outline of the panel 16 as shown in Fig. 18.

Since the two semiconductor chips are bonded on one multi-layer substrate, the number of connection portions to connect the multi-layer substrates can be decreased by 8 (14 connection portions can be made to be 6 connection portions). Therefore, the number of wires 15 can be reduced and the wire bonding process can be simplified.

As described above, use of the multi-layer substrates according to this embodiment enables the lines to be wired in the cross manner in the same multi-layer substrate as contrasted with the conventional TAB method using individual bus substrate to wire the bus lines in the cross manner. Therefore, the overall size can be reduced as compared with the TAB method by raising the density of the lines wired on the substrate. Further, the cost can be reduced because individual bus lines are not used.

Since the conventional COG method has the arrangement that the cross wiring of the bus lines is performed on the panel substrate, a wide area is required to wire the bus lines. Further, metal lines must be used to reduce the resistance value of the wired lines, resulting in an enlargement of the cost. However, use of the multi-layer substrate according to this embodiment enables the space required to wire the bus lines and the cost to be reduced as compared with the COG method.

Seventh Embodiment

A seventh embodiment will now be described with reference to Fig. 19.

Fig. 19 is an exploded perspective view which illustrates a multi-layer substrate of a liquid crystal display apparatus according to the present invention in which two semiconductor chips for driving liquid crystal are wire-bonded to the surface of one multi-layer substrate.

The surface of the first layer 1 of the multi-layer substrate has input lines 5 and 5' corresponding to input/output pads of the semiconductor chips 4 and 4' for driving liquid crystal. Further, the output lines 8 and 8' have wire bonding lands 22. The pattern, the through holes, the method of forming the multi-layer substrate, the arrangement and the structure are the same as those according to the sixth embodiment.

The reverse side of the semiconductor chip is secured to the surface of the multi-layer substrate. Further, the input/output pads of the semiconductor chips 4 and 4' and lands 22 on the surface of the first layer 1 of the multi-layer substrate are wire bonded. The wires may be wires of the same type as those used to connect the multi-layer substrates according to the sixth embodiment. Although omitted from the illustration, the bonding portions and the wiring portions are molded by molding members made similarly to the sixth embodiment.

The bus lines between the adjacent multi-layer substrates are wire-bonded similarly to the sixth embodiment. Although omitted from the illustration, the bonding portions and the wiring portions are molded by molding members made similarly to the first embodiment.

As described above, use of the multi-layer substrate according to this embodiment also enables the size and the cost to be reduced similarly to the sixth embodiment as compared with the conventional TAB method and the COG method.

Eighth Embodiment

An eighth embodiment will now be described with reference to Fig. 20.

Fig. 20 illustrates a liquid crystal display apparatus according to the present invention in which a multi-layer substrate 14 having two semiconductor chips 4 and 4' for driving liquid crystal face-down-bonded on the surface thereof is connected to the terminal 18 of the liquid crystal display panel by using a connection member 19. An essential portion of the connection portion is arranged to be similar to that according to the embodiment shown in Fig. 18. However, the leading portions of the input lines on the first layer 1 of the multi-layer

substrate are formed into heat seals or shapes that are suitable to connect the flexible substrate in place of the wire bonding lands.

The bus lines between the adjacent multi-layers 14 are connected by using a connection substrate 24. The connection substrate 24 may be a heat seal or a flexible substrate.

The width of a portion to which the connection substrate 24 is connected is smaller than the width of the multi-layer substrate 14 so that the multi-layer substrate 14 can be mounted within the outline of the panel 16.

As described above, use of the multi-layer substrate according to this embodiment also enables the size and the cost to be reduced as compared with the conventional TAB method and the COG method.

The connection of the semiconductor chips for driving liquid crystal to the surface of the multi-layer substrate and the electrical connection between the adjacent multi-layer substrates may be performed by methods which are the combination of the methods according to the sixth, seventh and the eighth embodiments. In any case, the size and the cost can also be reduced.

Further, the multi-layer substrate having the semiconductor chip for use in the foregoing embodiments mounted thereon can be mounted on another display apparatus or an electronic printing apparatus such that it can be mounted on a plasma display or an EL display apparatus by changing the foregoing semiconductor chip to a semiconductor chip for driving the plasma display or a semiconductor chip for driving the EL. By similarly mounting a semiconductor chip for driving a thermal head on the multi-layer substrate and by similarly connecting the multi-layer substrate to the thermal head, application to an electronic printing apparatus can be realized.

Ninth Embodiment

A ninth embodiment will now be described with reference to Figs. 25 to 28.

Fig. 25 is a cross sectional view which illustrates an embodiment of a mounting structure adapted to a liquid crystal display apparatus according to the present invention in which a

semiconductor device mounted on a laminated substrate is connected to a liquid crystal display device. Fig. 26 is a plan view which illustrates the mounting structure shown in Fig. 25. Fig. 27 is a detailed plan view which illustrates the terminal connection portion of the foregoing liquid crystal display device. Fig. 28 is a block diagram which illustrates a color liquid crystal apparatus structured by using the foregoing mounting structure.

Referring to Fig. 25, a liquid crystal display device 110 is a display substrate including a line electrode group, a column electrode group and a color filter. A liquid crystal composition is enclosed among the foregoing elements and electrode terminal group 113 is formed.

Laminated substrates 112-1 and 112-2 shown in Figs. 25 and 26 have output lines P11 to P3n and bus lines formed by patterning to establish the vertical electrical connections between the substrate layers, the laminated substrates 112-1 and 112-2 being stacked. Semiconductor devices 111-1, 111-2 and 111-3 are ICs which drive liquid crystal and which have connection terminals in which bumps are formed. Each of the semiconductor devices 111 is connected to the connection terminals formed on the laminated substrate 112 in a face-down mounting manner. Although three semiconductor devices 111-1, 111-2 and 111-3 are mounted to correspond to three-color pixels in this embodiment, the number of the semiconductor devices may be determined to be adaptable to the number of the pixels.

Each laminated substrate 112 has terminals for connecting each semiconductor device formed on the surface layer thereof, input/output line P11 of the semiconductor device 111-1 formed on the first layer thereof, input/output line P21 of the semiconductor device 111-2 on the second layer thereof, input/output line P31 of the semiconductor device 111-3 formed on the third layer thereof and bus lines formed on the surface of the third layer thereof. Although the laminated substrate 112 is formed into tree layers, the present invention is not limited to the number of layers if an efficient wiring pattern can be formed. Although this embodiment employs ceramic to make laminated substrate 112 depending upon consideration of expansion

and contraction occurring due to thermal influence, a polyimide film or the like, which is a flexible substrate, may be used.

As can be seen from Fig. 25, the structure for mounting a semiconductor device according to this embodiment has the arrangement that the lines for driving the liquid crystal display device 110 and the bus lines are formed on the substrate thereof. Therefore, the drive control circuit substrate can be omitted from the structure and, accordingly, the number of required elements can be decreased considerably. Therefore, the cost of the elements can be reduced significantly.

Referring to Fig. 27, the laminated substrate 112-1 and the liquid crystal display device 110 are connected to each other such that alignment is established between the liquid crystal display device electrode terminal group 113 respectively pulled out for color pixel R (red) 131-1, G (green) 131-2 and B (blue) 131-3 and the laminated substrate terminal group 114 connected to the semiconductor devices 111-1 (for red), 111-2 (for green) and 111-3 (for blue) corresponding to each pixel and formed at the extensions of the liquid crystal driving output line P11 (the output from the semiconductor device 111-1), P21 (the output from the semiconductor device 111-2) and P31 (the output from the semiconductor device 111-3). Further, a pressing machine is used to press and connect them under pressing conditions: 180°C, 30 Kg/cm^2 and 20 seconds so that the connection is established.

Color display suffers from a problem in that the contrast is unsatisfactory due to excessive cross talk as compared with white and black display because the drive method must bear a high duty. However, the connection method according to this embodiment is able to reduce the cross talk and, accordingly, a high-contrast display can be realized because individual output lines for semiconductor devices are connected for each color electrode and, therefore, a proper drive waveform can be supplied.

Fig. 28 is a block diagram which illustrates an embodiment of a color liquid crystal display apparatus using the foregoing mounting structure according to this embodiment. A display device 10 is a 640 x 480 dots STN color liquid crystal display, and semiconductor devices 111-1 to 111-12 are segment drivers for driving liquid crystal having 160 outputs.

Each of the laminated substrates 112-1 to 112-4 has semiconductor devices 111-1 to 111-12 for R (red), G (green) and B (blue) mounted thereon. The laminated substrates 112-1 to 112-4 are mounted in parallel on electrode terminals formed on the periphery of the liquid crystal display device 110. The laminated substrates 112-1 to 112-4, on which the semiconductor devices 111-1 to 111-12 are mounted, are mutually connected at four points for the purpose of supplying electric power and control signals.

When a color liquid crystal display apparatus was manufactured by employing the foregoing mounting structure, a compact liquid crystal display apparatus was formed because the density of the structure for mounting the semiconductors was raised. Further, the number of connections required to connect the liquid crystal display devices could be reduced to 1/3 as compared with the conventional structure. Therefore, the connection reliability was improved.

A liquid crystal display apparatus using the structure for mounting the semiconductor device according to this embodiment was manufactured and a reliability test was performed. As a result, satisfactory results were obtained in a TS test (between - 30°C and 80°C) in 1000 cycles and a TH test (at 60°C and 90%RH) for 1000 hours. Excellent connection reliability was realized.

Tenth Embodiment

Fig. 29 is a cross sectional view which illustrates an essential portion of the structure for mounting a semiconductor device according to this embodiment. In this embodiment, a liquid crystal display device (hereinafter called an "LCD") 203 is used as the electronic device.

Referring to Fig. 29, an LSI 201 is, at a predetermined position, mounted on a laminated substrate 202 having an internal conductive layer 221, an input line 204, an output line 205, a via-hole 261 and a bump 206 and the like, the LSI 201 being mounted by a face down method. The input and output terminals of the LSI 201 are connected to the input line 204 and the output line 205. The LSI 201 mounted as described above may be secured by an adhesive agent 208 if necessary to improve the reliability, such as the moisture resistance. The laminated substrate 202

includes an internal conductive layer 221 which electrically connects the two sides of each substrate to transmit each signal to the input line 204 and to make the internal conductive portion 221 to have a ground level so that noise is prevented. The bump portion 206 of the laminated substrate 202 and a terminal 231 of the LCD 203 are electrically connected to each other by using an ACF 209. Although the ACF 209 shown in Fig. 29 is used in a limited space adjacent to the bump 206, it may be disposed on the entire surface of the laminated substrate 202.

Fig. 30 is a plan view which illustrates one laminated substrate 202 adapted to the mounting structure according to this embodiment. Referring to Fig. 30, the output line 205 connected to the output terminal of an LSI 201 is electrically connected between the two sides of the laminated substrate 202 via the via-hole 261 and connected to the bump 206. Fig. 31 is a plan view which illustrates one laminated substrate 202 and which illustrates the reverse side. Referring to Fig. 31, bumps 206 for receiving signals from the output terminals of the LSI 201 are disposed in a zigzag manner. If the pitch of the output terminals is shortened to correspond to a fine pitch, it can be realized by increasing the zigzag lines to three or four lines.

The characteristics of the elements according to this embodiment are as follows:

LSI 201	formed into a square-like shape or an elongated shape arranged to have a ratio of the shorter side and the longer side of 1:5 or more. If an elongated LSI is used, an LSI of a type having output terminals and input terminals concentrated on one side as much as possible is used. Each terminal has a bump
Laminated Substrate 202	made of ceramics or glass epoxy resin and composed of three stacked layers
Electronic Device 203	an electronic device such as a liquid

crystal display device

Input Line 204	made of only Au or formed by applying Ni and Au plating to an AgPd base or a Cu base
Output Line 205	arranged similarly to the input line 204 formed by a method in which a conductive material is charged into the through hole and half-cut and a method in which it is printed on the side surface of the laminated substrate
Output Terminal 205a	arranged similarly to the output line 205
Bump 206	arranged similarly to the input line 204. It is preferable that the bump is formed into a circle or a rectangular shape having a top flat surface. Although the size of the bump is, of course, varied depending upon the pitch of the wire pattern, it is preferable to have a maximum size in a range in which the insulation can be maintained.
Mold 208	epoxy adhesive agent
ACF 209	thermo-hardening ACF such as #6000 series or #7000 series of Hitachi Chemical
Adhesive Agent 211	ultraviolet hardening adhesive agent or thermo-hardening epoxy adhesive agent

Fig. 32 is a plan view which illustrates an LCD module having the structure for mounting a semiconductor device and the mounting method according to the present invention. Referring to Fig. 32, a plurality of laminated substrates 202 are mounted on the terminals of the LCD 203. Although the laminated substrates 202 are connected to each other by using conductive wires made of Au, CU or Al or the like, a method using a heat seal or an FPC may be employed. Use of the mounting structure according to this embodiment even in a large-size LCD realizes a very compact mounting area.

Eleventh Embodiment

Fig. 33 is a cross sectional view which illustrates an essential portion of the structure for mounting a semiconductor device according to an eleventh embodiment, this embodiment having an arrangement that an LCD 203 is used as the electronic device. As contrasted with the tenth embodiment, this embodiment is characterized in that the laminated substrate 202 is so mounted that the bumps 206 are placed adjacently to the LCD 203.

Twelfth Embodiment

Fig. 34 is a cross sectional view which illustrates an essential portion of the structure for mounting a semiconductor device according to a twelfth embodiment, this embodiment having an arrangement that an LCD 203 is used as the electronic device. As contrasted with the tenth embodiment, this embodiment is characterized in that the output lines 205 of the laminated substrate 2 are electrically connected by lines 251 on the side surface in place of the via hole, the output lines 205 being connected to the bumps 206 on the reverse side.

Thirteenth Embodiment

Fig. 35 is a cross-sectional view which illustrates a thermo-sensitive electronic printing apparatus (hereinafter called an "electronic printing apparatus") according to a thirteenth embodiment and using the structure for mounting a semiconductor device according to the present invention. Referring to Fig. 35, a plurality of laminated substrates 202 are mounted on the terminal of a thermal printer head, which is the electronic printing device 213. Fig. 36 is a plan view which illustrates an electronic printing apparatus according to this

embodiment. Similarly to the structure using the LCD, a very compact mounting area can be realized.

Fourteenth Embodiment

Fig. 37 is a plan view which illustrates an embodiment of an electronic printing apparatus using the structure for mounting a semiconductor device according to the present invention. As contrasted with the thirteenth embodiment, this embodiment is characterized in that the laminated substrate 202 is formed into one integrated substrate.

Fifteenth Embodiment

Fig. 38 is a cross sectional view which illustrates an embodiment of an electronic printing apparatus using the structure for mounting a semiconductor device according to the present invention. This embodiment is characterized in that the laminated substrate 202 of the twelfth embodiment is applied to an electronic printing apparatus.

Sixteenth Embodiment

Fig. 39 is a cross sectional view which illustrates an embodiment of the structure for mounting a semiconductor device according to the present invention, wherein a liquid crystal display device is used as the electronic device. Referring to Fig. 39, an LSI 201 is, at a predetermined position, mounted on a laminated substrate 202 having an internal conductive layer 221, an input line 204 and an output line 205, the LSI 201 being mounted by a face down method. The input and output terminals of the LSI 201 are connected to the input line 204 and the output line 205. The LSI 201 mounted as described above may be secured by an adhesive agent 208 if necessary to improve the reliability, such as the moisture resistance. The laminated substrate 202 includes an internal conductive layer 221 which electrically connects the two sides of each substrate to transmit each signal to the input line 204 and to make the internal conductive portion 221 to have a ground level so that noise is prevented.

The output line 205 of the laminated substrate 202 is extended to reach the side surface of the laminated substrate 202, the output line 205 having the side surface portion which is formed into an output terminal 204a which can be connected to another electronic device. The output terminal 205a and an

electronic device 203 (which is a liquid crystal display device according to this embodiment and called an "LCD" hereinafter) are mounted and electrically connected to each other by using an ACF 209 so that the surface of the laminated substrate 202 and that of the electronic device (LCD) 203 are disposed perpendicular to each other. After the laminated substrate 202 is mounted, the laminated substrate 202 and the electronic device (LCD) 203 may be bonded and fixed by an adhesive agent 211 in order to strengthen the fixation. As a result of the employment of the foregoing mounting method, the mounting area A at the end portion of the electronic device 203 can be made 2 mm or smaller. Fig. 40 is a plan view which illustrates a liquid crystal apparatus. It is preferable that the size of the portion A shown in Fig. 40 is minimized to satisfy the characteristics required for a product. If a back-light is mounted on the reverse side of the LCD, the size of the portion A can be reduced significantly by using the mounting structure according to this embodiment. As a result, the quality of a manufactured LCD module can be improved considerably.

The characteristics of the elements according to this embodiment are as follows:

LSI 201	formed into a square-like shape or an elongated shape arranged to have a ratio of the shorter side and the longer side of 1:5 or more. If an elongated LSI is used, an LSI of a type having output terminals and input terminals concentrated on one side as much as possible is used. Each terminal has a bump
Laminated Substrate 202	made of ceramics or glass epoxy resin or the like having three stacked layers
Electronic Device 203	electronic device such as a liquid crystal display device

Input Line 204	made of only Au or formed by applying Ni and Au plating to an AgPd base or a Cu base
Output Line 205	similar to the input line 204
Output Terminal 205a	similar to the input line 204. A method in which a through hole (via hole) is formed and a terminal is formed by cutting at the central portion or a method in which a conductive pattern is printed and formed on the side surface of the substrate was employed.
Mold 208	epoxy adhesive agent
ACF 209	thermo-hardening ACF, such as AC 6000 series or 7000 series of Hitachi Chemical, the conductive particle density of which was 1000 particles/mm^2prior to the pressurization was used
Adhesive Agent 11	ultraviolet hardening type adhesive agent or thermo-hardening epoxy adhesive agent

Seventeenth Embodiment

Fig. 41 illustrates an embodiment of a liquid crystal display apparatus using the structure for mounting a semiconductor device according to the present invention. Referring to Fig. 41, a plurality of laminated substrates 202 are mounted on the terminal of the LCD 203 by using the structure for mounting a semiconductor device according to the present invention. The substrates are connected by wire bonding by using metal wires made of, for example, Au, Cu or Al or the like. The connection may be established by using a heat seal or an FPC using an ACF. Through use of the mounting structure according to this embodiment, a very compact mounting area can be realized

even in a large LCD as shown in Fig. 41.

Eighteenth Embodiment

Fig. 42 illustrates an example of a thermo-sensitive electronic printing apparatus (hereinafter called an "electronic printing apparatus") using the structure for mounting a semiconductor device according to the present invention. A laminated substrate 202 is mounted on the terminal of a thermal printer head, which is the electronic printing device 213. Similarly to the structure in which the LCD is used, a very compact mounting area can be realized.

Nineteenth Embodiment

A nineteenth embodiment will now be described with reference to Fig. 43.

Fig. 43 is an exploded perspective view which illustrates a multi-layer circuit substrate 311 according to an embodiment in which a semiconductor device 304 is, by using the method of mounting a semiconductor according to the present invention, face-down bonded on the multi-layer circuit substrate 311 having an opening portion 320 formed in the first layer 301, the semiconductor device 304 having the input terminals and output terminals disposed such that only an output terminal group is disposed on any one of peripheral sides of the semiconductor device and an input terminal group is disposed on one or two sides that are perpendicular to the foregoing side on which only the output terminal group is disposed. Reference numerals 301, 302 and 303 represent layers of the multi-layer circuit substrate (composed of three layers). Reference numeral 301 represents a first layer, 302 represents a second layer and 303 represents a third layer, the first layer 301 having the opening portion 320. The second layer 302 has, on the surface thereof, input lines 305 corresponding to the input electrodes of the semiconductor device 304, the input lines 305 being formed by patterning. The input lines 305 are connected to bus lines 309 of the third layer 303 via through holes 306. The input lines 305 have, at the leading portions thereof, lands 307 for establishing the connections between bus lines with an adjacent and similar multi-layer substrate 311.

Further, the output lines 308 on the second layer 302 have

output terminal through holes 324 at the leading portion thereof, the output lines 308 being connected to external connection terminals 310 via through holes formed in the third layer 303.

In this embodiment, the layers 301, 302 and 303 are made of a ceramic substrate obtained by simultaneously sintering alumina substrates at a low temperature. Each layer is formed into a thin layer having a thickness of about 0.25 mm. The input lines 305, the output lines 308 and the bus lines 309 are made by sintering paste of metal, such as Au, Ag, AgPd or Cu or the like. Similarly, the through holes 306 and 324 are formed by sintering paste of metal, such as Au, Ag, AgPd or Cu or the like. Also the lands 307 and the external connection terminals 310 are formed by sintering paste of metal, such as Au, Ag, AgPd or Cu or the like. The foregoing elements for the corresponding layers are formed by patterning performed by a known printing method, and the layers are stacked, sintered and integrated. As a result, forming of the layers is completed. The thickness of the metal patterned and sintered is usually about 0.001 mm to about 0.05 mm. The thickness may be about 0.05 mm to about 0.2 mm in order to reduce the resistance value.

Depending upon the pitch of the lines and upon the dimension accuracy, the input lines 305 and the lands 307 on the first layer 1, the output lines 8 on the second layer and the external connection terminals 310 on the third layer 303 may be formed by photolithographic patterning after the Au, Ag, AgPd or Cu metal paste has been printed on the entire surface. In this case, the thickness of the formed pattern is about 0.001 mm to about 0.2 mm. As an alternative to employing the printing method, the pattern may be formed by a photolithographic method or a plating method after Au, Ag or Cu has been evaporated or after the thin film has been formed by sputtering. In this case, the thickness of the formed pattern is about 0.0005 mm to about 0.1 mm.

Although the multi-layer circuit substrate is made of ceramic in this embodiment, it may be made of color-epoxy, paper phenol or polyimide.

Twentieth Embodiment

A twentieth embodiment will now be described with reference to Figs. 44 and 45.

Fig. 44 is a perspective view which illustrates an embodiment of the structure for mounting a semiconductor device according to this embodiment. Fig. 45 is a cross-sectional view of the structure. In this embodiment, a semiconductor device 304 is mounted on the multi-layer circuit substrate 311 according to the nineteenth embodiment such that the semiconductor device 304 is face-down bonded on the surface of the second layer 302 via the opening portion 320 of the first layer 301 by a known method (for example, a method in which Au bumps of the semiconductor is connected to the substrate by using Ag paste or a method using an anisotropic conductive film or the like).

After the face-down bonding process is performed, molding material 317 is supplied around the semiconductor device 304 and to the portion between the semiconductor device 304 and the surface of the second layer 302 in order to prevent corrosion and reinforce the fixation. This embodiment is characterized in that the surface of the second layer 302 has input lines 305 corresponding to the input electrodes of the semiconductor device 304 and formed by patterning.

Twenty-First Embodiment

A twenty-first embodiment will now be described with reference to Figs. 46 and 47.

Fig. 46 is a perspective view which illustrates an embodiment of the structure in which the semiconductor device 304 is fixed by an adhesive agent while passing through the opening portion 320 formed in the first layer 301 of the multi-layer circuit substrate 311 according to the nineteenth embodiment such that the upper surface of the active surface of the semiconductor device 304 faces upwards. The electrodes 325 of the semiconductor device 304 and the wire bonding lands 318 of the first layer 301 of the multi-layer circuit substrate 311 are connected by a wire bonding mounting method. This embodiment is characterized in that the pitch of the wire bonding lands 318 is made to be 60 μm to 300 μm and that the electrodes 325 and the wire bonding lands 318 are connected by Au wires 312.

Fig. 47 is a cross sectional view which illustrates an embodiment of the method of mounting the semiconductor device according to the twenty-first embodiment.

Twenty-Second Embodiment

A twenty-second embodiment will now be described with reference to Figs. 48 and 49.

Fig. 48 is an exploded perspective view which illustrates each element of an embodiment of the structure for mounting a semiconductor device according to this embodiment. Fig. 48 shows an embodiment of a method of mounting a bus line in which the semiconductor device 304 according to the twentieth embodiment passes through the opening portion 320 formed in the first layer 1 of the multi-layer circuit substrate 311, and the semiconductor device 304 is face-down mounted on the second layer 302. The bus lines 309 of the multi-layer circuit substrate 311, on which a plurality of semiconductor devices 304 are mounted, are wired by using an FPC 326 for wiring bus lines. This embodiment is characterized in that the FPC for wiring bus lines has connection lands 328 for wiring bus lines to correspond to the lands 307 of the multi-layer circuit substrate 311. Further, the lands 307 and the lands 328 for wiring bus lines are connected to one another by soldering or by using anisotropic conductive films or the like.

Fig. 49 is a front elevational view which illustrates a state where the semiconductor devices 304 and the FPC 326 shown in Fig. 48 have been mounted.

Twenty-Third Embodiment

A twenty-third embodiment will now be described with reference to Figs. 50 and 51.

Fig. 50 is an exploded perspective view which illustrates each element of an embodiment of the structure for mounting a semiconductor device according to this embodiment. Fig. 48 shows an embodiment of a method of mounting a bus line in which the semiconductor device 304 according to the twentieth embodiment passes through the opening portion 320 formed in the first layer 301 of the multi-layer circuit substrate 311, and the semiconductor device 304 is face-down mounted on the second layer 302. The bus lines 309 of the multi-layer circuit substrate 311, on which a plurality of semiconductor devices 304 are mounted, are wired by using a PCB substrate for wiring bus lines having a plurality of opening portions 329. This embodiment is

characterized in that the PCB substrate for wiring bus lines has connection lands 328 for wiring bus lines to correspond to the lands 307 of the multi-layer circuit substrate 311. Further, the lands 307 and the lands 328 for wiring bus lines are connected to one another by soldering or by using anisotropic conductive films or the like.

Fig. 51 is a front elevational view which illustrates a state where the semiconductor devices 304 and the PCB substrate 327 shown in Fig. 50 have been mounted.

Twenty-Fourth Embodiment

A twenty-fourth embodiment will now be described with reference to Fig. 52.

Fig. 52 is a perspective view which illustrates an embodiment of the structure for mounting a semiconductor device according to this embodiment. Fig. 52 shows an embodiment of a method of mounting a bus line in which the semiconductor device 304 according to the twentieth embodiment passes through the opening portion 320 formed in the first layer 301 of the multi-layer circuit substrate 311, and the semiconductor device 304 is face-down mounted on the second layer 302. The bus lines of the multi-layer circuit substrate 311, on which a plurality of semiconductor devices 304 are mounted, are connected by using the lands 307 formed on the first layer 301 of the multi-layer circuit substrate 311 with Au wires 312 by the wire bonding mounting method.

Twenty-Fifth Embodiment

A twenty-fifth embodiment will now be described with reference to Figs. 53 and 54.

Fig. 53 is an exploded perspective view which illustrates each element of an embodiment of the structure for mounting a semiconductor device according to this embodiment. Fig. 53 illustrates an example of the mounting method in which the semiconductor device 304 according to the twentieth embodiment is secured on the second layer 302 of the multi-layer circuit substrate 311 with an adhesive agent or the like in such a manner that the active side of the semiconductor device 304 faces upwards while passing through the opening portion 320 formed in the first layer 301 of the multi-layer circuit substrate 311.

Further, the electrodes 325 of the semiconductor device 304 and the wire bonding lands 318 of the first layer 301 of the multi-layer circuit substrate 311 are connected to one another by the wire bonding mounting method. The bus lines 309 of the multi-layer circuit substrate 311, on which a plurality of semiconductor devices 304 are mounted, are wired by using an FPC 326 for wiring bus lines. This embodiment is characterized in that the FPC for wiring bus lines has connection lands 328 for wiring bus lines to correspond to the lands 307 of the multi-layer circuit substrate 311. Further, the lands 307 of the multi-layer circuit substrate 311. Further, the lands 307 and the connection lands 328 for wiring lands are connected by soldering or by using anisotropic conductive films.

Fig. 54 is a front elevational view which illustrates a state where the semiconductor devices 304 and the FPC substrate 326 shown in Fig. 54 have been mounted.

Twenty-Sixth Embodiment

A twenty-sixth embodiment will now be described with reference to Figs. 55 and 56.

Fig. 55 is an exploded perspective view which illustrates each element of an embodiment of the structure for mounting a semiconductor device according to this embodiment. Fig. 55 illustrates an example of the mounting method in which the semiconductor device 304 according to the twentieth embodiment is secured on the second layer 302 of the multi-layer circuit substrate 311 with an adhesive agent or the like in such a manner that the active side of the semiconductor device 304 faces upwards while passing through the opening portion 320 formed in the first layer 301 of the multi-layer circuit substrate 311. Further, the electrodes 325 of the semiconductor device 304 and the wire bonding lands 318 of the first layer 301 of the multi-layer circuit substrate 311 are connected to one another by the wire bonding mounting method. The bus lines 309 of the multi-layer circuit substrate 311, on which a plurality of semiconductor devices 304 are mounted, are wired by using a PCB substrate for wiring bus lines having a plurality of openings. This embodiment is characterized in that the PCB substrate for wiring bus lines has connection lands 328 for wiring bus lines to

correspond to the lands 307 of the multi-layer circuit substrate 311. Further, the lands 307 of the multi-layer circuit substrate 311. Further, the lands 307 and the connection lands 328 for wiring lands are connected by soldering or by using anisotropic conductive films.

Fig. 56 is a front elevational view which illustrates a state where the semiconductor devices 304 and the PCB 327 shown in Fig. 55 have been mounted.

Twenty-Seventh Embodiment

A twenty-seventh embodiment of the present invention will now be described with reference to Fig. 57.

Fig. 57 is a perspective view which illustrates an embodiment of the structure for mounting a semiconductor device. Fig. 57 illustrates an example of the mounting method in which the semiconductor device 304 according to the twentieth embodiment is secured on the second layer 302 of the multi-layer circuit substrate 311 with an adhesive agent or the like in such a manner that the active side of the semiconductor device 304 faces upwards while passing through the opening portion 320 formed in the first layer 301 of the multi-layer circuit substrate 311. Further, the electrodes 325 of the semiconductor device 304 and the wire bonding lands 318 of the first layer 301 of the multi-layer circuit substrate 311 are connected to one another by the wire bonding mounting method. The bus lines 309 of the multi-layer circuit substrate 311, on which a plurality of semiconductor devices 304 are mounted, are connected by using the land formed on the surface of the first layer 301 of the multi-layer circuit substrate 311 by the wire bonding method using Au wires 312.

Twenty-Eighth Embodiment

A twenty-eighth embodiment will now be described with reference to Fig. 58.

Fig. 58 is a cross sectional view which illustrates an embodiment in which the structure for mounting the semiconductor device according to the present invention is adapted to a liquid crystal display apparatus, which is an electronic optical apparatus. Fig. 58 illustrates a state where the multi-layer circuit substrate 311, on which a plurality of semiconductor

devices according to the twenty-second embodiment, passing through the opening portion 320 formed in the first layer 301 of the multi-layer circuit substrate 311 and face-down mounting on the second layer 302 are mounted, is mounted on a liquid crystal display apparatus, the multi-layer circuit substrate 311 having the bus lines 309 mounted by using the FPC 326 for wiring bus lines. The external connection terminal 310 of the multi-layer circuit substrate 311 and the panel terminal 315 are connected to each other by an anisotropic conductive film 316. The anisotropic conductive film 316 establishes the electrical connection and as well as somewhat secures the multi-layer circuit board 311 to the liquid crystal panel 313. If the anisotropic conductive film 316 is made of a thermo-hardening material or a blend type of a thermoplastic material and a thermo-hardening material, a heating and pressurizing head is abutted against the multi-layer substrate 311 so that the anisotropic conductive film 316 is hardened and connected. If the anisotropic conductive film 316 is made of an ultraviolet hardening type material, a pressuring head is abutted against the multi-layer circuit substrate and ultraviolet rays are applied from a position adjacent to the panel terminal 315 (adjacent to the glass) so that the anisotropic conductive film 316 is hardened.

Further, molds 330 are charged to protect exposed portions of the panel terminal from corrosion, the molds 330 also serving to secure the multi-layer circuit substrate to the liquid crystal panel 313.

By using the multi-layer circuit substrate according to this embodiment as described above, adaption to a fine pitch of 80 μm or less, which has been previous considered difficult with the conventional TCP method can be realized.

Further, the conventional COG method in which the wiring of the bus lines in the cross manner on the liquid crystal panel requires a wide area in which the bus lines are wired. What is worse, metal lines must be used in order to reduce the circuit resistance and, accordingly, the cost cannot be reduced. However, use of the multi-layer circuit substrate 311 enables the space required to wire the bus lines and cost can be reduced as

compared with the COG method.

Twenty-Ninth Embodiment

A twenty-ninth embodiment will now be described with reference to Fig. 59.

Fig. 59 is a cross sectional view which illustrates an embodiment in which the structure for mounting the semiconductor according to the present invention is adapted to the head portion of a thermal printer which is the electronic printing apparatus. In this embodiment,
the multi-layer circuit substrate 311, on which a multiplicity of semiconductor devices 304 according to the twenty-second embodiment passing through the opening portion 320 of the first layer 301 of the multi-layer circuit substrate 311 and face-down mounted on the second layer 311 are mounted, is mounted on the thermal printer head of the electronic printing apparatus. The external connection terminal 310 of the multi-layer substrate 311 and the panel terminal 315 are connected to each other by an anisotropic conductive film 316.

Thirtieth Embodiment

A thirty embodiment will now be described with reference to Fig. 60.

Fig. 60 is a cross sectional view which illustrates an embodiment in which the mounting structure of the multi-layer circuit substrate according to the twenty-third embodiment is adapted to a liquid crystal display apparatus which is the electronic optical apparatus. As contrasted with the twenty-eighth embodiment, this embodiment is characterized in that bus lines of a plurality of multi-layer circuit board 311 are mounted by using a PCB substrate 327 for wiring bus lines having a plurality of opening portions 321.

Thirty-First Embodiment

A thirty-first embodiment of the present invention will now be described with reference to Fig. 61.

Fig. 61 is a cross sectional view which illustrates an embodiment in which the mounting structure of the multi-layer circuit board according to the twenty-third embodiment is adapted a thermal printer head of an electronic printing apparatus. As contrasted with the twenty-ninth embodiment, this embodiment is

characterized in that the bus lines of a plurality of multi-layer circuit substrates 311 are mounted by using a PCB substrate 327 having a plurality of opening portion 321.

Thirty-Second Embodiment

A thirty-second embodiment will now be described with reference to Fig. 62.

Fig. 62 is a perspective view which illustrates an embodiment in which the mounting structure of the multi-layer circuit substrate according to the twentieth embodiment is adapted to a liquid crystal display apparatus which is an electronic optical apparatus. As contrasted with the twenty-eighth embodiment, this embodiment is characterized in that the bus lines of a plurality of multi-layer circuit boards 311 are connected by using Au wires 312 by the wire bonding method.

Thirty-Third Embodiment

A thirty-third embodiment will now be described with reference to Fig. 63.

Fig. 63 is a perspective view which illustrates an embodiment in which the mounting structure of the multi-layer circuit substrate according to the twentieth embodiment is adapted to the head portion of a thermal printer which is the electronic printing apparatus. As contrasted with the twenty-ninth embodiment, this embodiment is characterized in that the bus lines of a plurality of multi-layer circuit boards 311 are connected by using Au wires 312 by the wire bonding method.

Thirty-Fourth Embodiment

A thirty-fourth embodiment will now be described with reference to Fig. 64.

Fig. 64 is a cross sectional view which illustrates an embodiment in which the mounting structure of the multi-layer circuit substrate according to the twenty-first embodiment is adapted to the liquid crystal display apparatus which is the electronic optical apparatus. As contrasted with the twenty-eighth embodiment, the input/output terminals of the semiconductor device 304 are connected by the wire bonding method.

Thirty-Fifth Embodiment

A thirty-fifth embodiment will now be described with

reference to Fig. 65.

Fig. 65 is a cross sectional view which illustrates an embodiment in which the mounting structure of the multi-layer circuit substrate according to the twenty-ninth embodiment is adapted to the head portion of a thermal printer which is the electronic printing apparatus. As contrasted with the twenty-ninth embodiment, the input/output terminals of the semiconductor device 304 are connected by the wire bonding method.

Thirty-Sixth Embodiment

A thirty-sixth embodiment will now be described with reference to Fig. 66.

Fig. 66 is a cross sectional view which illustrates an embodiment in which the mounting structure of the multi-layer circuit substrate according to the twenty-first embodiment is adapted to the liquid crystal display apparatus which is the electronic optical apparatus. As contrasted with the thirty-fourth embodiment, this embodiment is characterized in that the bus lines of a plurality of multi-layer circuit substrates 311 are mounted by using a PCB substrate 327 having a plurality of opening portion 321.

Thirty-Seventh Embodiment

A thirty-seventh embodiment will now be described with reference to Fig. 67.

Fig. 67 is a cross sectional view which illustrates an embodiment in which the mounting structure of the multi-layer circuit substrate according to the twenty-first embodiment is adapted to the head portion of a thermal printer which is the electronic printing apparatus. As contrasted with the thirty-fifth embodiment, this embodiment is characterized in that the bus lines of a plurality of multi-layer circuit substrates 311 are mounted by using a PCB substrate 327 having a plurality of opening portion 321.

Thirty-Eighth Embodiment

A thirty-eighth embodiment will now be described with reference to Fig. 68.

Fig. 68 is a perspective view which illustrates an embodiment in which the mounting structure of the multi-layer circuit substrate according to the twenty-first embodiment is

adapted to the liquid crystal display apparatus which is the electronic optical apparatus. As contrasted with the twenty-eighth embodiment, this embodiment is characterized in that the bus lines of a plurality of multi-layer circuit boards 311 are connected by using Au wires 312 by the wire bonding method.

Thirty-Ninth Embodiment

A thirty-ninth embodiment will now be described with reference to Fig. 69.

Fig. 69 is a perspective view which illustrates an embodiment in which the mounting structure of the multi-layer circuit substrate according to the twenty-first embodiment is adapted to the head portion of a thermal printer which is the electronic printing apparatus. As contrasted with the twenty-ninth embodiment, this embodiment is characterized in that the bus lines of a plurality of multi-layer circuit boards 311 are connected by using Au wires 312 by the wire bonding method.

Fortieth Embodiment

A fortieth embodiment will now be described with reference to Fig. 70.

Fig. 70 illustrates a liquid crystal display apparatus according to the present invention in which a multi-layer substrate 14, on which a semiconductor chip 4 for driving liquid crystal is face-down bonded, is connected to the terminal 18 of a liquid crystal display panel by using the connection member 19 similarly to the first embodiment. The essential portion of the connection portion is arranged similarly to that shown in Fig. 4. However, the multi-layer substrate has projections that are formed in only the portions which are required for wire bonding.

By using the multi-layer substrate according to this embodiment, unnecessary portions can be eliminated in the multi-layer substrate. Further, the distance between the multi-layer substrates is shortened while necessitating a minimum size so that the length of the wire for use in the wire bonding operation is shortened. As a result, generation of defective connection due to breakage of the wire can be reduced and, accordingly, a low cost and reliable liquid crystal display apparatus can be provided.

Forty-First Embodiment

A forty-first embodiment will now be described with reference to Fig. 71.

Fig. 71 illustrates a liquid crystal display apparatus according to the present invention in which a multi-layer substrate 14, on which a semiconductor chip 4 for driving liquid crystal is face-down bonded, is connected to the terminal 18 of a liquid crystal display panel by using the connection member 19 similarly to the first embodiment. The essential portion of the connection portion is arranged similarly to that shown in Fig. 4. However, the upper layer of the multi-layer substrate is smaller than the residual layers, a step portion is formed at the end portion of the multi-layer substrate, and the adjacent multi-layer substrates are connected such that wire bonding is performed in each of the two sections.

As described above, use of the multi-layer substrate according to this embodiment in which wire bonding is performed in each of the two sections enables the wire bonding lands can be integrated. As a result, the size of the multi-layer substrate can be reduced. Therefore, a compact apparatus, the cost of which can be reduced, can be provided.

Forty-Second Embodiment

A forty-second embodiment will now be described with reference to Fig. 72.

Fig. 72 illustrates a liquid crystal display apparatus according to the present invention in which the multi-layer substrates 14 having the semiconductor chips 4 face-down bonded on the surface thereof are connected to the terminal 18 of the liquid crystal display panel by using the connection member 19 similarly to the first embodiment. The essential portion of the connection portion is arranged similarly to that of the first embodiment shown in Fig. 4. However, portion M of the multi-layer substrate shown in Fig. 72 has one or more intermediate layers between the upper layer and the lower layer thereof. The intermediate layer and/or the lower layer has a smaller area than that of the upper layer so that a groove portion is formed.

As described above, use of the multi-layer substrate according to this embodiment arranged such that the intermediate layer and/or the lower layer of the multi-layer substrate except

the upper layer is arranged to have a smaller area than that of the upper area so that a space to which a jig and tool are fastened is formed. As a result, the multi-layer substrate can easily be handled at the time of the machining operations.

Forty-Third Embodiment

A forty-third embodiment will now be described with reference to Figs. 73, 74 and 75.

Fig. 73 is an exploded perspective view which illustrates a liquid crystal display apparatus according to the present invention in which a multi-layer substrate has a semiconductor chip for driving liquid crystal face-down bonded on the surface thereof.

Reference numerals 1, 2 and 3 represent layers of the multi-layer (three layer) substrate according to this embodiment. Reference numeral 1 represents a first layer, 2 represents a second layer and 3 represents a third layer. Similarly to the first embodiment, the semiconductor chip 4 for driving liquid crystal is face-down bonded on the surface of the multi-layer substrate. After bonding has been performed, the periphery of the semiconductor chip 4 and portions between the semiconductor chip 4 and the first layer 1 are molded. The first layer 1 has, on the surface thereof, input lines 5 corresponding to the input pads of the semiconductor chip 4 . The input lines 5 are connected to the bus lines 10 of the second layer 2 via through holes 6. The input lines 5 have, at the leading portions thereof, lands 7 for wire-bonding another multi-layer substrate disposed adjacently and formed similarly.

Further, output lines 8 corresponding to the output pads of the semiconductor chip 4 are formed on the surface of the first layer by patterning. Since the pitch of the panel terminals is longer than the pitch of the output pads of the semiconductor chip 4 , wiring is performed such that the pattern is widened on the first layer 1 to make the output pads coincide with the panel terminals. Further, through holes 9 are formed at the leading portions of the output lines 8 so that the output lines 8 are connected to the connection terminals 13 formed on the reverse side of the first layer for establishing the connection with the panel.

The layers 1, 2 and 3 are ceramic substrates formed by simultaneously sintering alumina substrates at low temperature.

Fig. 74 illustrates the cross section of an essential portion of an embodiment in which the multi-layer substrate according to the embodiment shown in Fig. 73 is connected to a liquid crystal display panel.

Fig. 75 illustrates an essential portion of an embodiment in which the multi-layer substrate according to the embodiment shown in Fig. 73 is connected to a liquid crystal display panel.

As described above, the arrangement of the multi-layer substrate according to this embodiment in which a portion of the multi-layer substrate is removed from the upper surface of the liquid crystal display panel enables the thickness of the liquid crystal display apparatus to be reduced.

Further, the multi-layer substrate having the semiconductor chip for use in the foregoing embodiments mounted thereon can be mounted on another display apparatus or an electronic printing apparatus such that it can be mounted on a plasma display or an EL display apparatus by changing the foregoing semiconductor chip to a semiconductor chip for driving the plasma display or a semiconductor chip for driving the EL. By similarly mounting a semiconductor chip for driving a thermal head on the multi-layer substrate and by similarly connecting the multi-layer substrate to the thermal head, application to an electronic printing apparatus can be realized.

Forty-Fourth Embodiment

Another embodiment of the present invention will now be described with reference to Figs. 76, 77 and 78. Figs. 76 and 77 are perspective views which illustrate a liquid crystal display apparatus according to the present invention which comprises a multi-layer substrate according to the embodiment and having a semiconductor chip for driving liquid crystal which is face-down-bonded on to the surface thereof. Although the material and the constitution of the multi-layer substrate according to this embodiment are the same as those of the multi-layer substrate according to First Embodiment, a fastening hole 432 is formed. Although the drawings illustrate the circular fastening hole 432, the shape may be formed into a rectangle, an ellipse, a square or

an elongated hole.

Fig. 77 illustrates the liquid crystal display apparatus making use of multi-layer substrates 14 and 431a to 431d shown in Figs. 76 and 77. The multi-layer substrates 14 and 431a to 431d having the semiconductor chips 4 mounted on the surfaces thereof are connected to a panel 16. The panel 16, a member formed by integrating a backlight unit 435 and an exterior decoration case 436 and an exterior decoration case 433 are, by a fixing screw 434, fixed to the multi-layer substrates 431a to 431d by way of the fastening hole 432. As a result, the exterior decoration case of the liquid crystal display apparatus according to the present invention is able to also serve as the exterior case of a PC (Personal Computer) or the like. Therefore, the elements, such as the frame and the metal frame and the like that have been required for the conventional liquid crystal display apparatus as individual elements, can be omitted. As a result, the cost of the elements can be reduced. Further, the number of assembling processes can be simplified and the number of machining processes can be decreased.

Although the multi-layer substrates 14 and 431a to 431d and the panel terminal 18 are, similarly to First Embodiment, connected to one another by an adhesive member 19 and bonded and reinforced by a mold 21, the mold 21 may be provided for the side surfaces or the reverse surfaces of the panel 18 and the multi-layer substrates 14 and 431a to 431d in order to improve the strength (strength against vibrations) realized after the foregoing elements have been assembled into the frame. The mold 21 is made of a material selected from a group consisting of epoxy, acrylic, urethane and polyester compound or a mixture of two or more of these of a solvent, a photo-setting or a mixture type thereof.

Since the positional accuracy between the pattern of the multi-layer substrate and the fastening cut portion can be made to be ± 0.1 mm or less, the positional accuracy between the panel pattern and the fastening hole can be maintained at ± 0.2 mm or less. Sine the foregoing fastening hole is used to assemble the elements to the exterior decoration case 436 which is the case, the position reproducibility with respect to the backlight unit

435 and that of the exterior decoration case 433 with respect to a panel display can be maintained and improved. Further, the elements can be reworked and reassembled easily if the fastening screw 434 is used to assemble the elements. If a plastic and rivet-like element having a flange is used, assembling and fixing can be performed by simply pushing the rivet-like element. Therefore, assembling can easily be performed. The backlight 435 and the exterior decoration case 436 may be fixed by a method using a double-coated tape or a fastening claw.

Forty-Fifth Embodiment

Another embodiment of the present invention will now be described with reference to Figs. 79, 80 and 81. As shown in Figs. 79 and 81, the sizes of the multi-layer substrates 437a to 437d are designed to be larger than that of the end surface of a glass terminal 18 so that the fastening cut portion is made project over the end surface of the glass terminal 18 and it is fixed. Although the material and the structure of the multi-layer substrate are the same as those of the multi-layer substrate according to First Embodiment, the fastening cut portion 438 is formed. Although the fastening cut portion 438 is formed into a semicircular shape in this embodiment, it may be formed into a partial or full rectangle, square, rhomboid, ellipse or an elongated hole. If the fastening cut portion is disposed at the central portion of the multi-layer substrates 437a to 437d to form the shape to be laterally symmetrical with respect to the central line in the direction of the longitudinal side of the multi-layer substrate, the standardization of the elements can be realized such that the four different elements can be replaced by four same elements.

Fig. 80 illustrates a liquid crystal display apparatus according to the present invention that makes use of the multi-layer substrates 437a to 437d shown in Fig. 79. The multi-layer substrates 14 and 437a to 437d having the semiconductor chips 4 mounted on the surfaces thereof are connected to a panel 16. The panel 16, a member formed by integrating a backlight unit 435 and an exterior decoration case 436 and an exterior decoration case 433 are, by a fixing screw 434, fixed to the multi-layer substrates 431a to 431d by way of the fastening cut portion 438.

As a result, the exterior decoration case of the liquid crystal display apparatus according to the present invention is able to also serve as the exterior case of a PC (Personal Computer) or the like. Therefore, the elements, such as the frame and the metal frame and the like that have been required for the conventional liquid crystal display apparatus as individual elements, can be omitted. Further, the standardization of the elements can be realized by forming the fastening cut portions 438 of the multi-layer substrates 437a to 437d to be in a uniform shape. As a result, the cost of the elements can be reduced. Further, the assembling processes can be simplified and the number of machining processes can be decreased because the number of elements can be decreased.

Fig. 81 illustrates the cross section of a portion in which the multi-layer substrates 437a to 437d of the liquid crystal display apparatus according to the present invention are connected. Although the multi-layer substrates 14 and 437a to 437d and the panel terminal 18 are bonded and reinforced by an adhesive member 19 and a mold 21, the mold 21 may be provided for the end surface of the panel terminal 18 and the side surfaces or the reverse surfaces of the multi-layer substrates 14 and 437a to 437d in order to improve the strength (strength against vibrations) realized after the foregoing elements have been assembled into the frame. The mold is made of a material selected from a group consisting of epoxy, acrylic, urethane and polyester compound or a mixture of two or more of these of a solvent, a photo-setting or a mixture type thereof.

Since the positional accuracy between the pattern of the multi-layer substrate and the fastening cut portion can be made to be ± 0.1 mm or less, the positional accuracy between the panel pattern and the fastening cut portion can be maintained at ± 0.2 mm or less. Sine the foregoing fastening hole is used to assemble the elements to the exterior decoration case 436 which is the case, the position reproducibility with respect to the backlight unit 435 and that of the exterior decoration case 433 with respect to a panel display can be maintained and improved. Further, the elements can be reworked and reassembled easily if the fastening screw 434 is used to assemble the elements. If a

plastic and rivet-like element having a flange is used, assembling and fixing can be performed by simply pushing he rivet-like element. Therefore, assembling can easily be performed. The backlight 435 and the exterior decoration case 436 may be fixed by a method using a double-coated tape or a fastening claw.

Forty-Sixth Embodiment

An embodiment of the present invention will now be described with reference to Figs. 82, 83, 84, 85, 86, 87, 88 and 89.

Fig. 82 illustrates an embodiment of a multi-layer substrate 6000 of a liquid crystal display apparatus according to the present invention in which three semiconductor chips for driving liquid crystal are face-down-bonded on the surface of one multi-layer substrate.

Fig. 83 is a perspective view which illustrates the multi-layer substrate 6000 shown in Fig. 82. Pad pitch P1 on the output side on each of semiconductor chips 1100, 1200 and 1300 is 80 μm and pitch P2 of a panel terminal is 50 μm, where a relationship P1 > P2 is held. The foregoing panel terminal pitch P2 = 50 μm is a fine connection pitch required for a 6-inch class VGA-color liquid crystal display apparatus.

Reference numerals 1000, 2000, 3000, 4000 and 5000 represent layers of the multi-layer (composed of five layers) substrate according to this embodiment. Reference numeral 1000 represents a first layer, 2000 represents a second layer, 3000 represents a third layer, 4000 represents a fourth layer and 5000 represents a fifth layer. The semiconductor chips 1100, 1200 and 1300 are face-down-bonded on to the surface of the first layer 1000 by a known method (for example, a method in which the Au bumps of the semiconductor are connected to the substrate by making use of Ag paste, or a method making use of an anisotropic conductive film or a flip-flop chip method making use of soldering bumps). After bonding has been performed, molds 20 (omitted from illustration) are applied to the peripheries of the semiconductor chips 1100, 1200 and 1300 and the spaces among the semiconductor chips 1100, 1200 and 1300 and the surface of the first layer 1000 for the purpose of preventing corrosion and reinforcing the elements. The molds are made of material selected from a group consisting

of epoxy, acrylic, urethane and polyester compound or a mixture of two or more of these of a solvent, a photo-setting or a mixture type thereof.

Fig. 84 is a plan view which illustrates circuit lines, through holes and penetrating holes of the first layer 1000.

Fig. 85 is a plan view which illustrates circuit lines, through holes and penetrating holes of the second layer 2000.

Fig. 86 is a plan view which illustrates circuit lines, through holes and penetrating holes of the third layer 3000.

Fig. 87 is a plan view which illustrates circuit lines, through holes and lands of the fourth layer 4000.

Fig. 88 is a plan view which illustrates circuit lines, through holes and connection terminals of the fifth layer 5000.

On the surface of the first layer 1000, input lines 1110, 1210 and 1310 corresponding to input pads of 1100, 1200 and 1300 are formed by patterning. Further, the input lines 1110, 1210 and 1310 (however, input lines 1110-1, 1110-N, 1210-1, 1210-N, 1310-1 and 1310-N are excluded) are connected to a bus line 2020 of the second layer 2000 by way of their through holes 1120, 1220 and 1320. In addition, the bus line 2020 of the second layer 2000 is connected to a bus line 4020 of the fourth layer 4000 by way of a through hole 2030 of the second layer 2000 and a through hole 3030 of the third layer 3000. Since the input lines 1110-1, 1110-N, 1210-1, 1210-N, 1310-1 and 1310-N are cascade-connected, they are wired in a manner different from the manner for wiring the residual lines. That is, the input line 1110-1 of the semiconductor chip 1100 is connected to a line 4020 via a through hole 1120-1 of the first layer 1000 and a through hole 2120 of the second layer 2000 and a through hole 3120 of the third layer 3000. The input line 1210-1 of the semiconductor chip 1200 is connected to a line 3020 of the third layer 3000 via a through hole 1220-1 of the first layer 1000 and a through hole 2220 of the second layer 2000. The input line 1210-N is connected to a line 3020 of the third layer 3000 via a through hole 1220-N of the first layer 1000 and a through hole 2220 of the second layer 2000. The input line 1310-1 of the semiconductor chip 1300 is connected to a line 3020 via a through hole 1320-1 of the first layer 1000 and a through hole

2320 of the second layer 2000. The input line 1310-N of the semiconductor chip 1300 is connected to a line 3020 of the third layer 3000 via a through hole 1320-N of the first layer 1000 and a through hole 2320 of the second layer 2000. Further, the line 3020 is connected to a line 4020 of the fourth layer 4000 via a through hole 3120 of the third layer 3000. The line 4020 has a land 4040 for establishing a wire bonding connection with another multi-layer substrate. Through holes 1010, 2010 and 3010 are formed in the first, second and third layers 1000, 2000 and 3000 to correspond to the land 4040 so that wire bonding is facilitated.

The first layer 1000 has, on the surface thereof, output lines 1130, 1230 and 1330 corresponding to the output pads of the semiconductor chips 1100, 1200 and 1300 and formed by patterning, the output lines 1130, 1230 and 1330 being connected to a line 5050 and a connection terminal 5060 via through holes 1140, 1240 and 1340 of the first layer 1000, through holes 2140, 2240 and 2340 of the second layer 2000, through holes 3140, 3240 and 3340 of the third layer 3000 and through holes 4140, 4240 and 4340 of the fourth layer 4000 and through holes 5140, 5240 and 5340 of the fifth layer 5000. Since the pitch of the terminals of the panel is smaller than the pitch of the output pads of the semiconductor chips 1100, 1200 and 1300 , the wiring pattern is narrowed on the first layer 1000 to make the output pads correspond to the terminals of the panel. Although this embodiment is so arranged that the through holes 1140, 1240, 1340, 2140, 2240, 2340, 3140, 3240, 3340, 4140, 4240 and 4340 are disposed to form a line, they may be disposed to form zigzag shape composed of plural lines. The alignment between the pitch of the output pads and the pitch of the terminals of the panel may be performed over a plurality of layers.

The first, second, third, fourth and fifth layers 1000, 2000, 3000, 4000 and 5000 are ceramic substrates made by simultaneously sintering alumina substrates at a low temperature and each having a thickness of 0.25 mm. The input lines 1110, 1210, 1310, 1110-1, 1210-1, 1310-1, 1110-N, 1210-N, 1310-N, the output lines 1130, 1230 and 1330 and the lines 2020, 3020, 4020 and 5050 are made of material obtained by sintering metal paste

such as Au, Ag, AgPd or Cu. Also the through holes 1120, 1220, 1320, 1120-1, 1220-1, 1320-1, 1120-N, 1220-N, 1320-N, 1140, 1240, 1340, 2030, 2120, 2220, 2320, 2340, 3030, 3120, 3140, 3240, 3340, 4140, 4240, 4340, 5140, 5240 and 5340 are made of material obtained by sintering metal paste, such as Au, Ag, AgPd or Cu. The foregoing elements are formed by patterning by a known printing method for each layer, followed by stacking the layers and by sintering them to be formed into an integrated shape. The thickness of the metal subjected to patterning and sintered is usually about 0.001 mm to about 0.05 mm, the thickness being permitted to be about 0.05 mm to about 0.2 mm in order to reduce the resistance value.

Depending upon the pitch of wiring and the dimension accuracy, the input lines 1110, 1210, 1310, 1110-1, 1210-1, 1310-1, 1110-N, 1210-N, 1310-N and the output lines 1130, 1230 and 1330 on the surface of the first layer 1000 and the line 5050 and the connection terminal 5060 on the reverse side of the fifth layer 5000 may be formed by printing metal paste, such as Au, Ag, AgPd or Cu, onto the entire surface of the first layer 1000 followed by photolithographic patterning. The thickness of the pattern thus-formed is about 0.001 mm to about 0.2 mm. The pattern may be formed by photolithography or plating after a thin film has been formed by evaporating or sputtering Au, Ag or Cu. The thickness of the pattern thus-formed may be about 0.0005 mm to about 0.1 mm.

Although the multi-layer substrate according to this embodiment is composed of the five layers, the number of layers may be determined arbitrarily. Further, one or more ground layers may be formed at an intermediate position in order to eliminate noise or prevent static electricity.

In the foregoing case where the relationship P1 > P2 is held such that the pad pitch P1 on the outside of the semiconductor chip is 80 μm and the connection pitch P2 of the panel terminals is 50 μm, the problems experienced with the conventional example, in which a plurality of semiconductor chips for driving liquid crystal are mounted on a liquid crystal display apparatus by TCPs, can be overcome, the problems being problems raised in that the adjacent TCPs undesirably overlap or the substrate having the

bus line cannot easily be connected to the input terminal. However, use of the multi-layer substrate according to this embodiment prevents the overlap of the adjacent multi-layer substrates. Therefore, the semiconductor chips for driving liquid crystal can be mounted on a small area. As a result, a liquid crystal display apparatus can be provided which exhibits a large capacity (the VCA or XGA specification), reduced weight, small thickness and small size can be provided to serve as a display apparatus for small-size PDA (Personal Digital Assistance) information terminal equipment which is expected to be widely used in the future.

Further, the structure in which the three semiconductor chips for driving liquid crystal on one multi-layer substrate enables the input and output lines to efficiently be wired as compared with a structure comprising three multi-layer substrates on each of which one semiconductor chip for driving liquid crystal is mounted. In addition, the semiconductor chips can efficiently be disposed, resulting in that the area required for the multi-layer substrates can be decreased and the element cost can be reduced. Moreover, the process for decomposing (dicing or breaking) the multi-layer substrate and the process for setting and resetting the multi-layer substrate for bonding and molding it can be reduced. As a result, the cost can be reduced, resulting in that a low-cost liquid crystal display apparatus can be provided.

Fig. 89 illustrates an embodiment in which the multi-layer substrate according to the embodiment shown in Fig. 82 is connected to a liquid crystal display panel. In this embodiment, the color liquid crystal display-type panel 16 (for example, 640 x 3 x 480 dot display) has four multi-layer substrates 6000 (on which three 160-output-semiconductor chips for driving liquid crystal are mounted) disposed on the side X and two multi-layer substrates 14 (on which one 240-output-semiconductor chip for driving liquid crystal is mounted) disposed on the side Y such that the substrates are connected to a panel terminal 18. In Fig. 89, the panel lines and the lines on the multi-layer substrate are omitted. Connection terminals 13 and 5060 of the multi-layer substrates 14 and 6000 and the panel terminal 18 are

connected to one another by a connection member 19 similarly to First Embodiment. A conductive member 19 establishes the electrical connection and somewhat secures the panel to the multi-layer substrates 14 and 6000.

The connection member 19 for use in this embodiment is made of an anisotropic conductive film mainly composed of conductive particles and an adhesive agent. The conductive particles are composite metal particles of Ni, Au, Ag, Cu, Pb or Sn or a any mixture made by mixing, alloying or soldering, or particles made by plating Ni, Au, Cu or Fe or a mixture of two or more of these on to plastic particles (polystyrene, polycarbonate or acryl) or carbon particles. The adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or compound of two or more of these materials. If the anisotropic conductive film is disposed between the panel terminal 18 and the connection terminals 13 and 5060 of the multi-layer substrates 14 and 6000 and if the anisotropic conductive film is a thermo-hardening agent or a blended agent of a thermoplastic agent and a thermo-hardening agent, a heating and pressuring head is abutted against the multi-layer substrates 14 and 6000 so that the agent is hardened and connected. If the anisotropic conductive film is an ultraviolet hardening type adhesive, a pressuring head is abutted against the multi-layer substrates 14 and 6000 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminal 18 (adjacent to the glass) to harden the ultraviolet hardening type film.

Alternatively, as the connection member 19, an anisotropic conductive adhesive agent mainly composed of conductive particles and an adhesive agent is used. The conductive particles are sole soldering particles, sole Ni, Au, Ag, Cu, Pb or Sn particles or a mixture or alloy of two or more of these, complex metal particles made by plating, particles formed by plating sole Ni, Co, Pd, Au, Ag, Cu, Fe, Sn or Pb or a mixture of two or more of these materials on plastic particles (polystyrene, polycarbonate or acryl or the like) or carbon particles. The foregoing adhesive agent is a sole styrene butadiene styrene (SBS), epoxy, acryl, polyester or urethane adhesive agent or a mixture or

compound of two or more of these materials. The anisotropic conductive adhesive agent is a fluid or paste agent and applied to the portion in which the panel terminal 16 is connected by a known method, for example, printing or a dispensing method using a dispenser. If the anisotropic conductive adhesive agent is a thermo-hardening agent or a blended agent of a thermoplastic agent and a thermo-hardening agent, a heating and pressuring head is abutted against the multi-layer substrates 14 and 6000 so that the agent is hardened and connected. If the anisotropic conductive film is an ultraviolet hardening type film, a pressuring head is abutted against the multi-layer substrates 14 and 6000 and ultraviolet rays are applied to the anisotropic conductive film from a position adjacent to the panel terminal 18 (adjacent to the glass) to harden the ultraviolet hardening type film.

In order to protect the exposed portion of the panel terminal 18, a molding 21 (omitted from illustration) is placed. The molding 21 also serves to fix the multi-layer substrates 14 and 6000 to the panel. The molding 21 is made of sole epoxy, acryl, urethane or polyester material or a mixture or compound of two or more of these materials of any one of solvent type, thermo-hardening type, or light hardening type or a mixture thereof.

The bus lines between adjacent multi-layer substrates 14 and between the multi-layer substrates 6000 are connected by wire bonding with wires 15 via the lands 7 and 4040. The input lines on either side of the multi-layer substrates 14 and 6000 positioned at ends on the side X and side Y of the panel are wire-bonded to a relay substrate 7000 by the wires 15. Further, a connection member 8000 for receiving signals and electric power from outside is connected to the relay substrate 7000. The connection member 8000 has one or more wiring pattern layers (omitted from illustration) and may have electronic parts or the like. The wires 15 may be made of metal such as Au, Al or Cu or the like or their alloy (alloy containing Be, Si or Mg or the like included). In order to protect the wire-bonded portion and the wire portion and the like from corrosion to mechanically reinforce the same, the molds 21 (omitted from illustration) are

similarly applied. The width of the wire-bonded portion is so determined as to be narrower than the width of the multi-layer substrate, resulting in that the wire-bonded portion can be mounted in a satisfactorily compact manner.

Since this embodiment is so arranged that three semiconductor chips for driving liquid crystal are bonded on to one multi-layer substrate, the number of connection portions required to connect the multi-layer substrates to one another can be reduced by eight (from 11 places to 3 places) as compared with a case where semiconductor chips for driving liquid crystal, each of which is bonded on to one multi-layer substrate, are connected to one another are used. As a result, the number of the wires 15 can be decreased and the number of wire bonding processes can be decreased.

As described above, use of the multi-layer substrate according to this embodiment enables the lines to be wired in the cross manner in the same multi-layer substrate as contrasted with the conventional TAB method using individual bus substrate to wire the bus lines in the cross manner. Therefore, the overall size can be reduced as compared with the TAB method by raising the density of the lines wired on the substrate. Further, the cost can be reduced because individual bus lines are not used.

Since the conventional COG method has the arrangement that the cross wiring of the bus lines is performed on the panel substrate, a wide area is required to wire the bus lines. Further, metal lines must be used to reduce the resistance value of the wired lines, resulting in an enlargement of the cost. However, use of the multi-layer substrate according to this embodiment enables the space required to wire the bus lines and the cost to be reduced as compared with the COG method.

In the case where the relationship P1 > P2 is held such that the pad pitch P1 on the output side of the semiconductor chip is 80 μm and the connection pitch P2 of the panel terminals is 50 μm, the overlap of the adjacent multi-layer substrates can be prevented and the semiconductor chips can be mounted on a small area. As a result, a liquid crystal display apparatus can be provided which exhibits a large capacity (the VCA or XGA specification), reduced weight, small thickness and small size

can be provided to serve as a display apparatus for small-size PDA (Personal Digital Assistance) information terminal equipment which is expected to be widely used in the future.

As described above, the present invention is arranged so that the input and output lines of the semiconductor device, the bus lines and the connection terminals are formed on the laminated substrate, and a plurality of semiconductor devices are mounted and connected to the electrodes of the display device. Therefore, the drive control circuit substrate can be omitted, and the number of the mutual connection lines for the semiconductor devices can be decreased. Therefore, the reliability can be improved and the size of the apparatus can be reduced. Further, semiconductor device outputs are supplied for corresponding colors so that an effect can be obtained in that the quality of display can be improved.

Although the invention has been described in its preferred form with a certain degree of particularly, it is understood that the present disclosure of the preferred form has been changed in the details of construction and the combination and arrangement of parts may be resorted to without departing from the spirit and the scope of the invention as hereinafter claimed.

CLAIMS:

1. A liquid crystal display apparatus comprising a liquid crystal panel having mounted thereon a plurality of semiconductor chips for driving liquid crystal, said liquid crystal display apparatus comprising:

at least one multi-layer substrate having at least one of said semiconductor chips mounted thereon and composed of an upper surface having an input line pattern to said at least one chip and an output line pattern from said at least one chip, a reverse surface and at least one intermediate layer formed between said upper surface and said reverse surface, wherein

said at least one intermediate layer has a portion of said input lines and/or output lines as a circuit pattern, and said at least one multi-layer substrate having said lines connected to one another via through holes is electrically connected to a panel terminal.

2. The apparatus according to claim 1, wherein a plurality of semiconductor chips are mounted on said at least one multi-layer substrate.

3. The apparatus according to claim 1 or 2, wherein face bonding or wire bonding is used as means for mounting said semiconductor chip(s) on the surface of said multi-layer substrate according.

4. The apparatus according to claim 1, 2 or 3, wherein an anisotropic conductive film is used to electrically connect said output lines of said multi-layer substrate and said panel terminal.

5. The apparatus according to any one of claims 1 to 4 comprising a plurality of said multi-layer substrates, wherein wire bonding, a heat seal connection or a flexible

substrate connection is used for establishing electrical connection among said plurality of multi-layer substrates.

6. The apparatus according to any one of claims 1 to 4 comprising a plurality of said multi-layer substrates, wherein lines on said liquid crystal panel are used for establishing electrical connection among said plurality of multi-layer substrates.

7. The apparatus according to claim 6, wherein said lines are disposed in said panel terminal portion and on the inside of a panel cell.

8. The apparatus according to claim 6, wherein the connection between said lines on said liquid crystal panel and said input lines of said multi-layer substrate and the connection between said output lines of said multi-layer substrate and said panel terminal are collectively established.

9. The apparatus according to claim 8, wherein said connection is established by an anisotropic conductive film.

10. The apparatus according to claim 9, wherein said anisotropic conductive film comprises an adhesive agent layer and conductive particles dispersed therein, the thickness of the adhesive agent layer is smaller than the particle size of the conductive particles.

11. A liquid crystal display apparatus having a line electrode group and a column electrode portion formed on a display substrate thereof said electrode portions forming a plurality of pixels, and display drive signals are supplied from a semiconductor device to said electrode portions to perform color pixel display, said liquid crystal display apparatus comprising:

a laminated substrate having bus lines and connection terminals formed thereon; and



semiconductor devices mounted on said laminated substrate, wherein output lines of said semiconductor devices independently provided for each color electrode are connected to electrode terminals extended from said display substrate.

12. The apparatus according to claim 11, wherein said semiconductor devices are mounted on the surface of said laminated substrate.

13. The apparatus according to claim 11, wherein said semiconductor devices formed into a rod-like shape and having input and output terminals running in parallel and facing each other are mounted on said laminated substrate.

14. A structure for mounting a semiconductor device wherein a semiconductor device having an output terminal on at least a main output terminal side thereof and an input terminal on a side thereof facing said main output terminal side is used, and said semiconductor device is mounted on a predetermined pattern of a laminated circuit substrate having at least an output circuit pattern and an input circuit pattern, said structure comprising:

a bump formed on a terminal of said laminated substrate, said bump being [electrically and/or mechanically] connected to another electronic device.

15. A structure for mounting a semiconductor device wherein a semiconductor device having an output terminal on at least a main output terminal side thereof and an input terminal on a side thereof facing said main output terminal side is used, and said semiconductor device is mounted on a predetermined pattern of a laminated circuit substrate having at least an output circuit pattern and an input circuit pattern, said structure comprising:

a terminal formed in a side surface portion of said laminated substrate, said terminal used to mount said laminated substrate on an electronic device so that the plane of

said laminated substrate and the plane of said electronic device are positioned substantially perpendicularly to one another.

16. The structure according to claim 15, wherein the connection between said laminated substrate and said electronic device is established by using an anisotropic conductive film.

17. An electro optical apparatus comprising a structure as defined in any one of claims 14 to 16.

18. An electronic printing apparatus comprising a structure as defined in any one of claims 14 to 16.

19. A multi-layer substrate having a semiconductor device mounted thereon, said multi-layer substrate being composed of an upper layer having an input line pattern to said semiconductor device and an output line pattern from said semiconductor device, a lower layer having an output terminal to be connected to an external terminal and at least one intermediate layer formed between said upper layer and said lower layer said at least one intermediate layer having a portion of an input line and/or an output line as a circuit pattern, said lines being connected via through holes, said multi-layer substrate further comprising:

an opening portion formed in at least one of said layers .

20. A method of mounting a semiconductor device on the surface of a multi-layer substrate as defined in claim 19, said method comprising the steps:

passing said semiconductor through the opening portion formed in the upper layer of said multi-layer substrate; and

mounting said semiconductor on the surface of an intermediate layer adjacent to the upper layer by employing face down bonding or wire bonding.



21. The method of claim 20, wherein, when a plurality of said multi-layer substrates is provided, bus lines for input signals to said multi-layer substrates are collectively connected by using an FPC, or a PCB substrate having a plurality of opening portions, or by wire bonding.

22. The apparatus according to claim 1 wherein a projection or a pit is provided in at least a portion of a side of said at least one multi-layer substrate.

23. The apparatus according to claim 1 wherein an arbitrary one of the plural layers of said multi-layer substrate is smaller than the other layers.

24. The according to claim 1 wherein said multi-layer substrate has a fastening hole or a fastening cut portion formed therein.

* C L M S *

ABSTRACT OF THE DISCLOSURE (Fig. 1)

LIQUID CRYSTAL DISPLAY APPARATUS, STRUCTURE FOR MOUNTING SEMICONDUCTOR DEVICE, METHOD OF MOUNTING SEMICONDUCTOR DEVICE, ELECTRONIC OPTICAL APPARATUS AND ELECTRONIC PRINTING APPARATUS

A liquid crystal display apparatus is provided which needs a small, thin and compact area thereof for mounting semiconductor chips for driving liquid crystal and, accordingly, a reduced cost. Semiconductor chips (4) for driving liquid crystal are mounted on the surfaces (the first layers (1)) of multi-layer substrates in a face-down manner, each of the surfaces having input lines (5) to the chips (4) and output lines (8) from the chips. The input lines have lands (7) for connecting the multi-layer substra-tes to each other. At least one intermediate layer (2) is formed between the upper surface (1) and the reverse surface (3), the intermediate layer having bus lines (10). The bus lines and the input lines of the first layer are connected to one another via through holes (6). The output lines of the first layer and the terminals (13) of the third layer are connected to one another via through holes of the first, second and the third layers (9, 11, 12).

FIG. 1

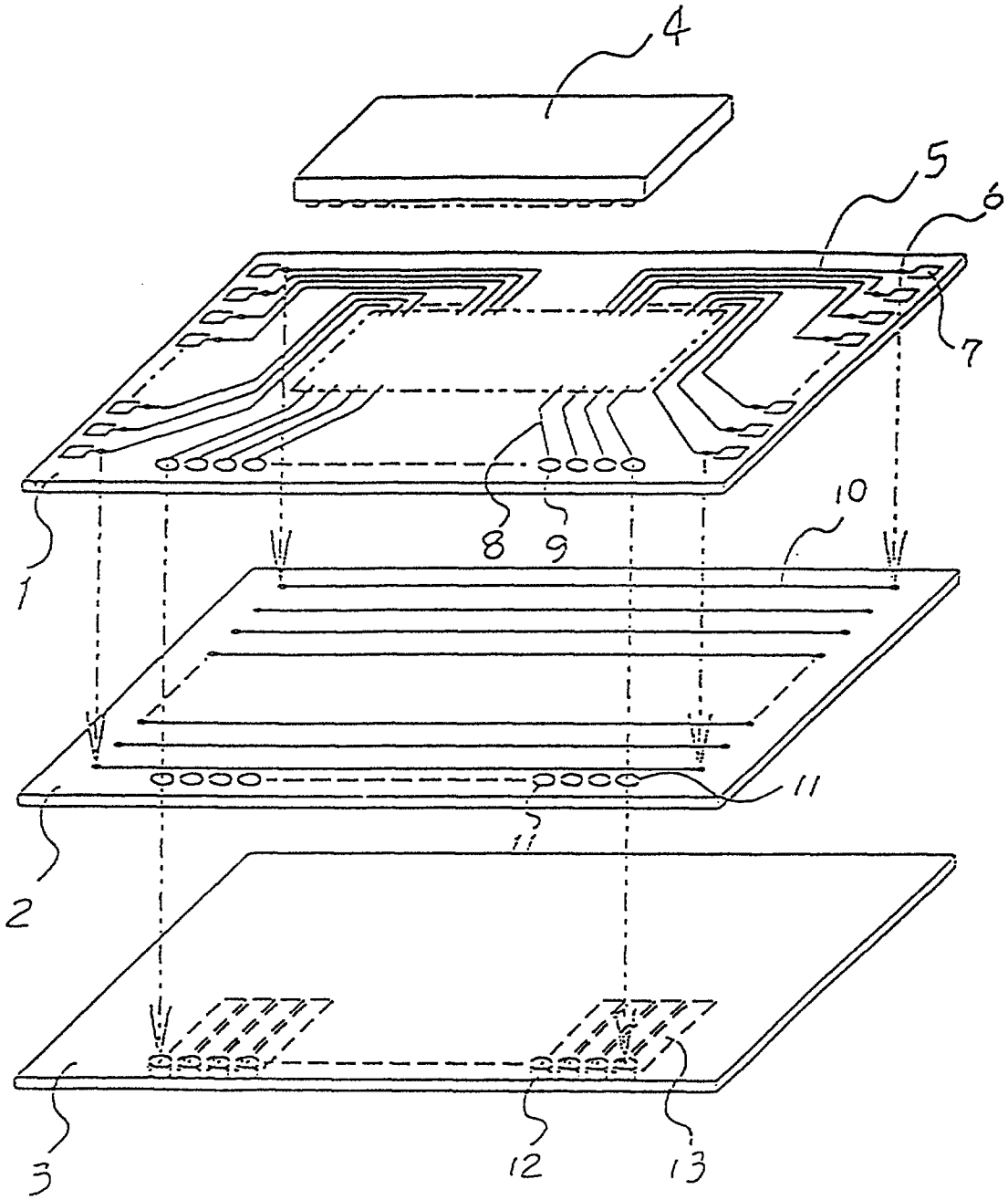


FIG. 2

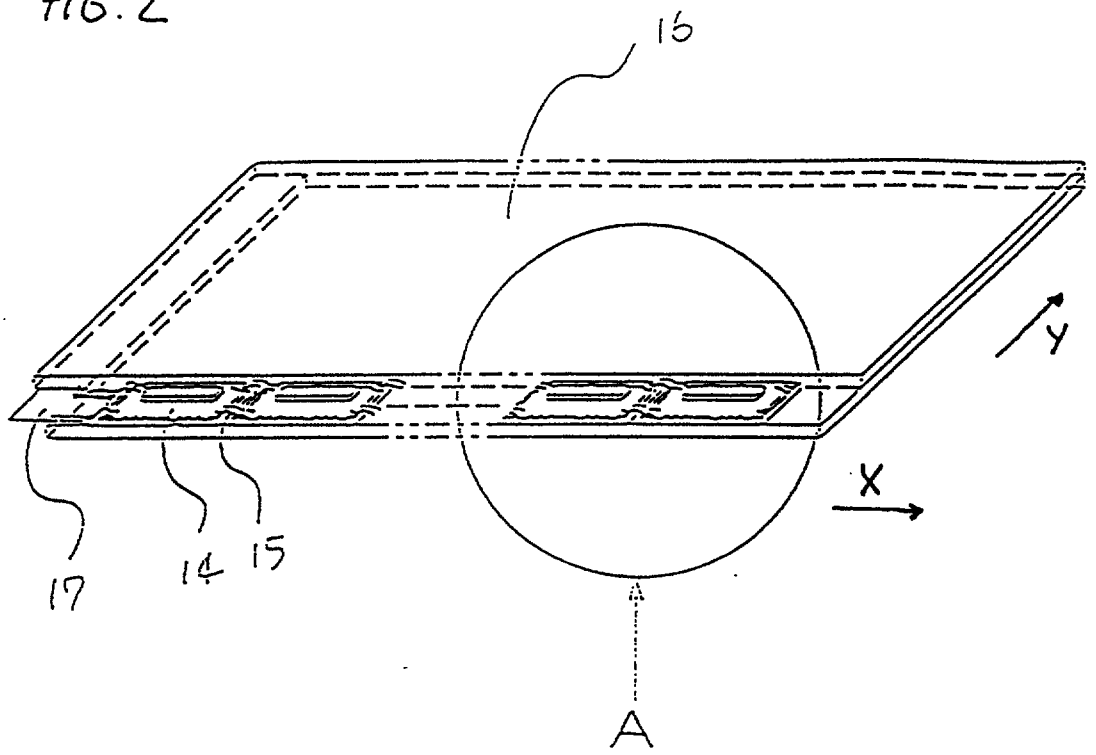


FIG. 6

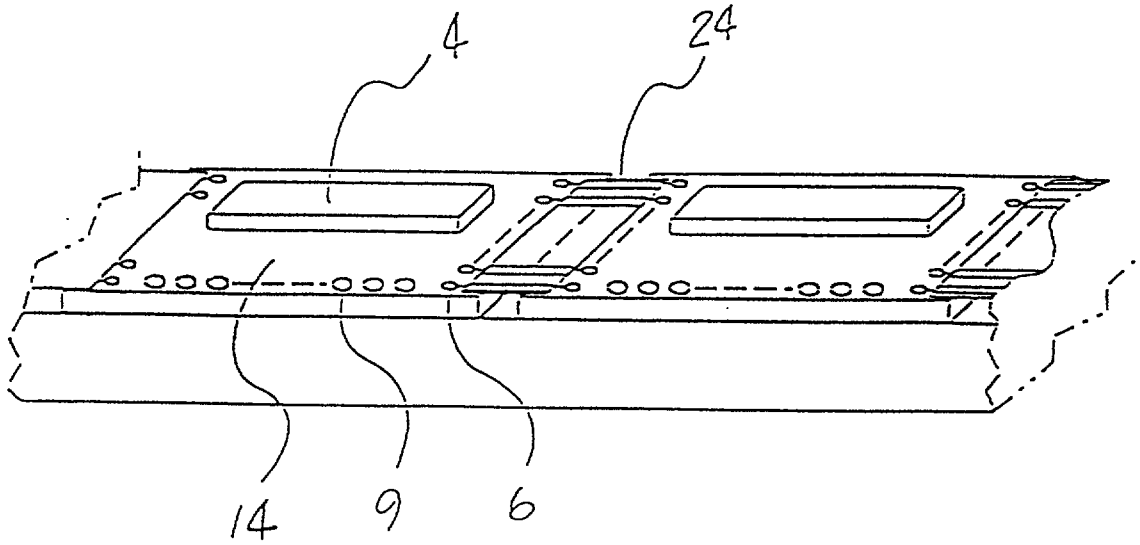


FIG. 3

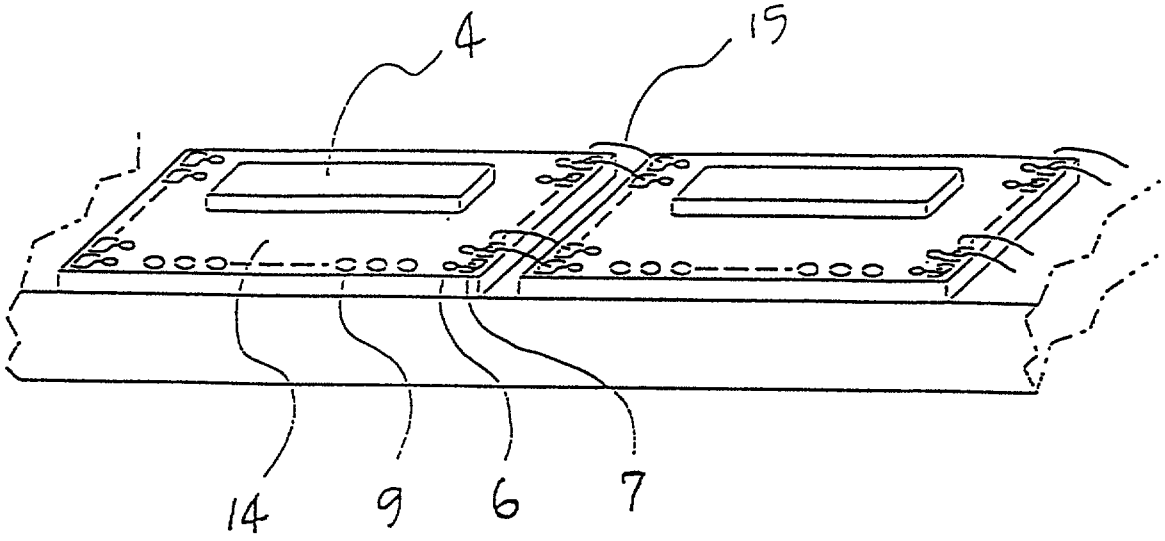


FIG. 4

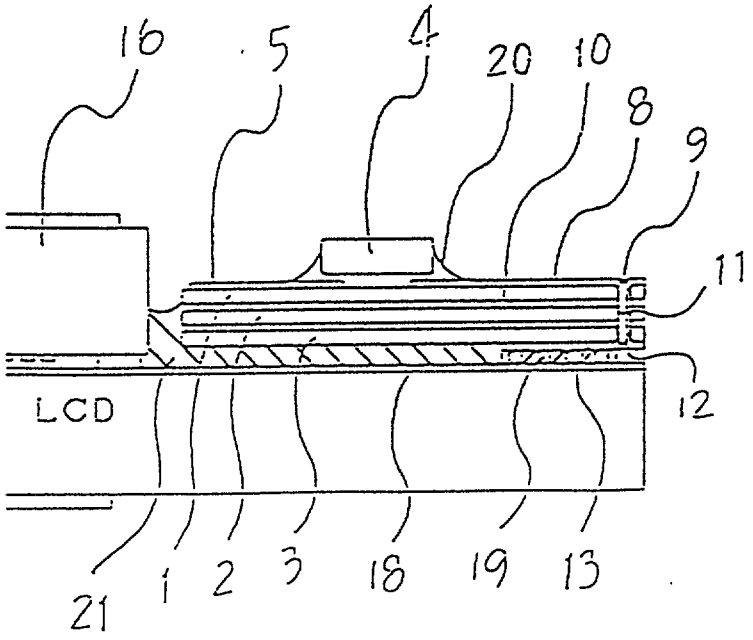


FIG. 5

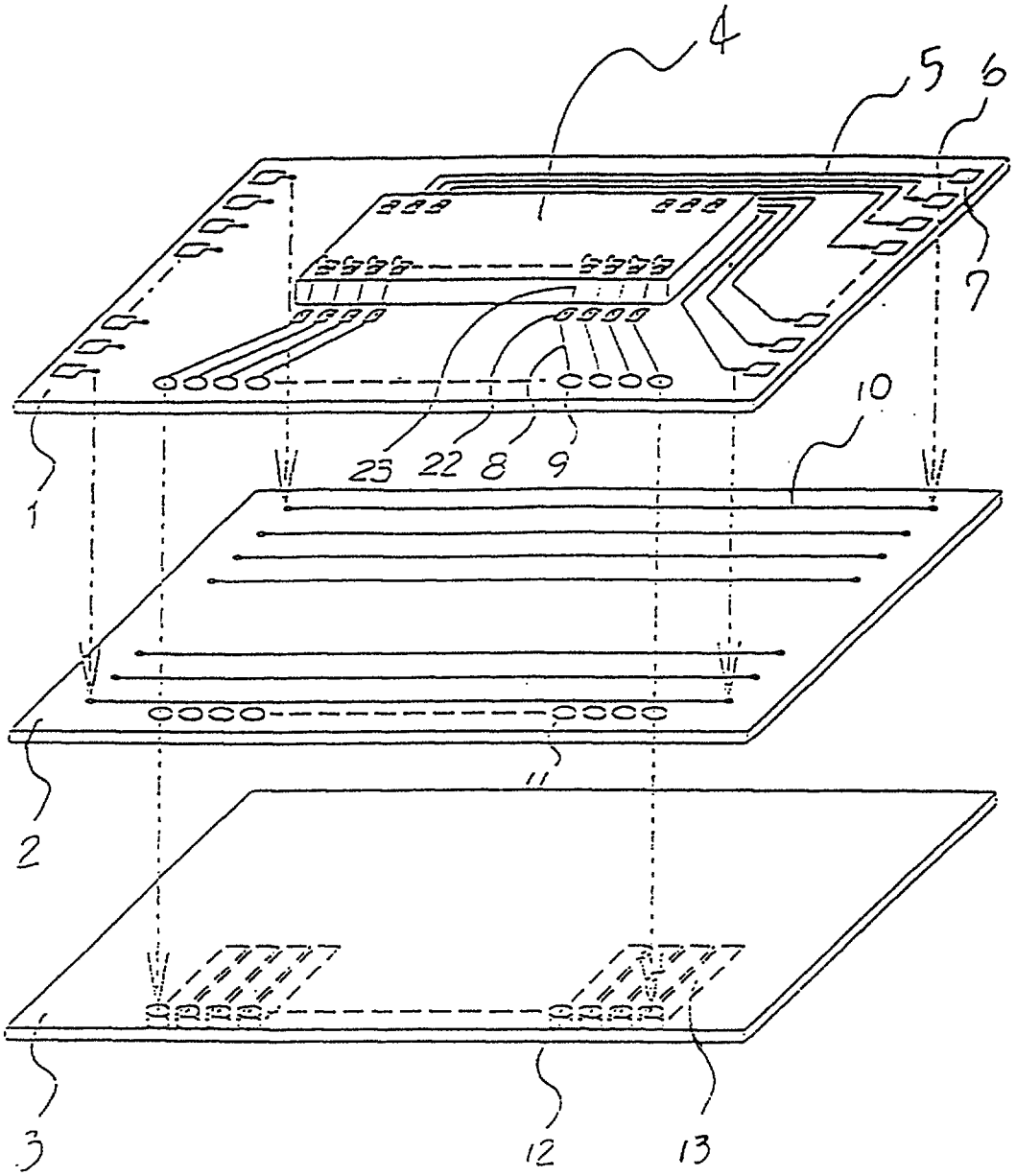


FIG. 7

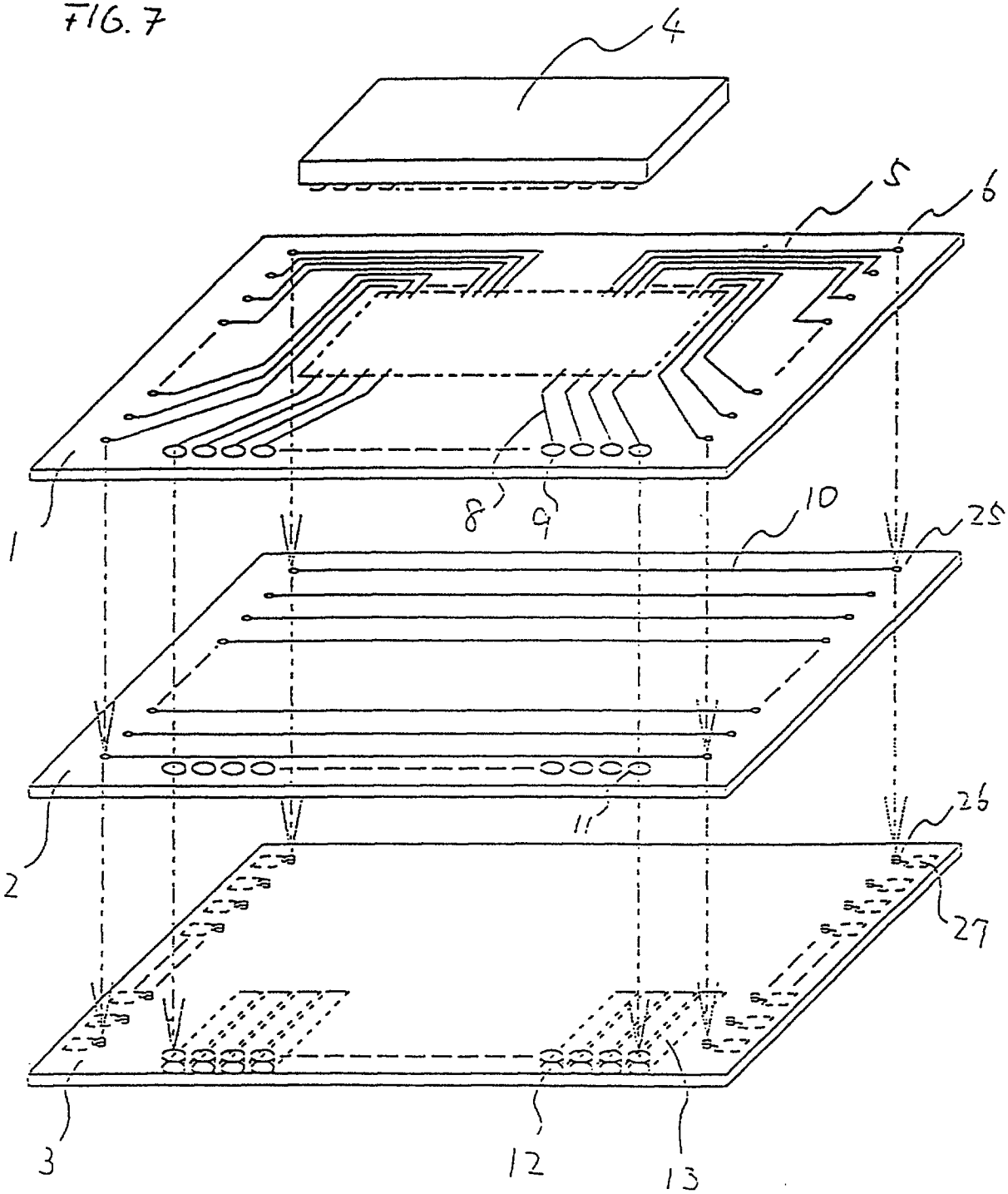


FIG. 8

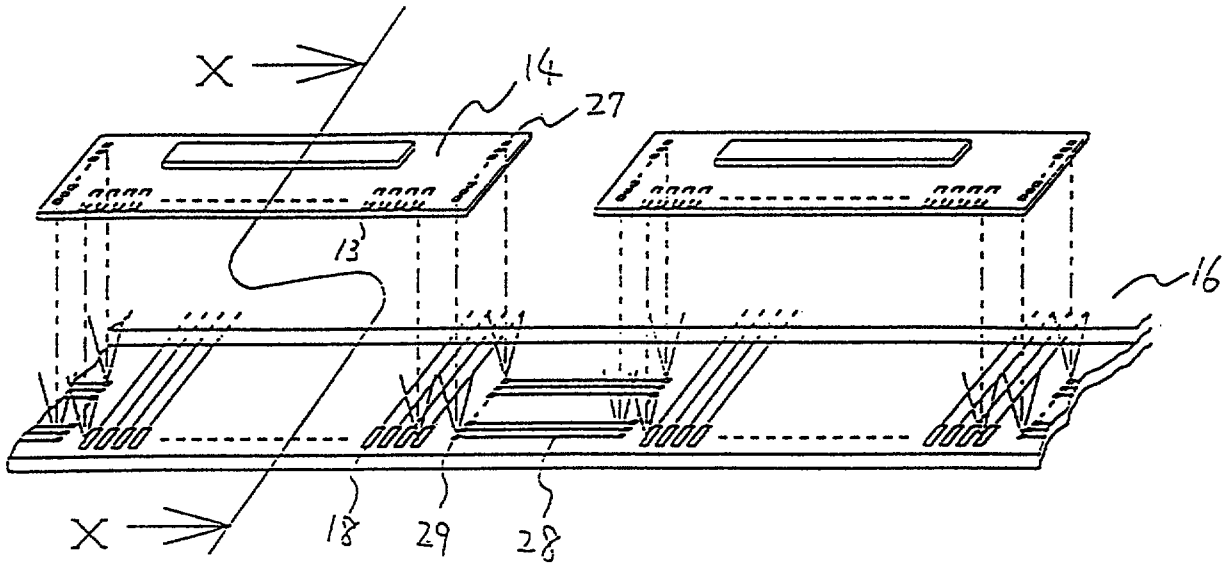


FIG. 9

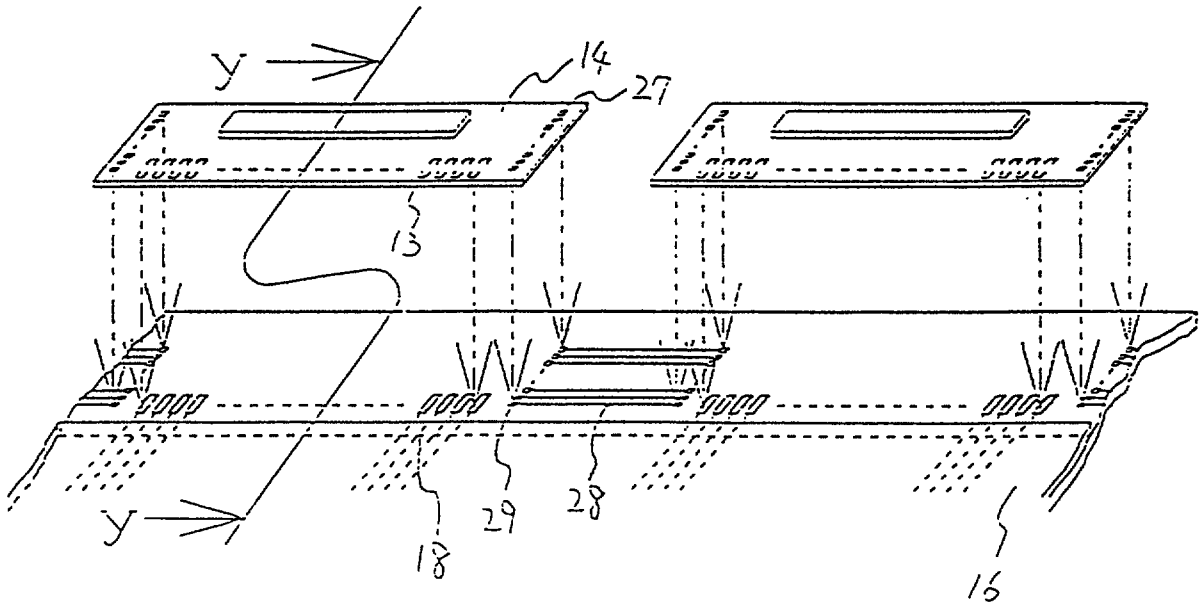


FIG. 10

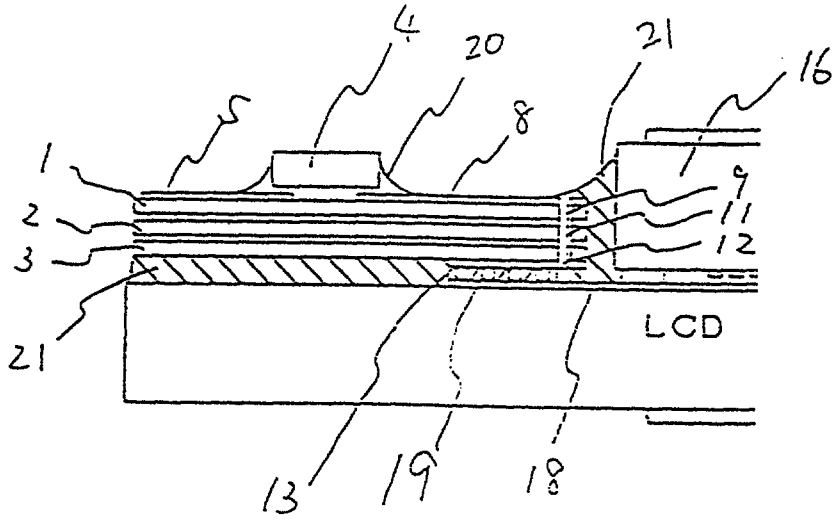


FIG. 14

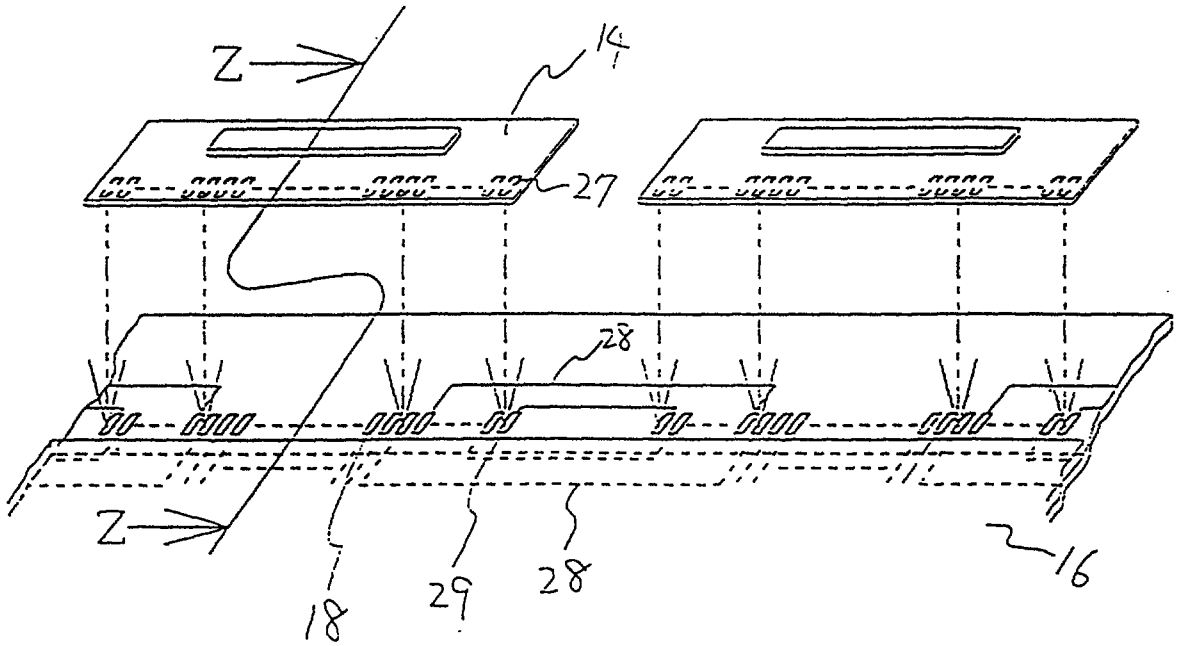


FIG. 11

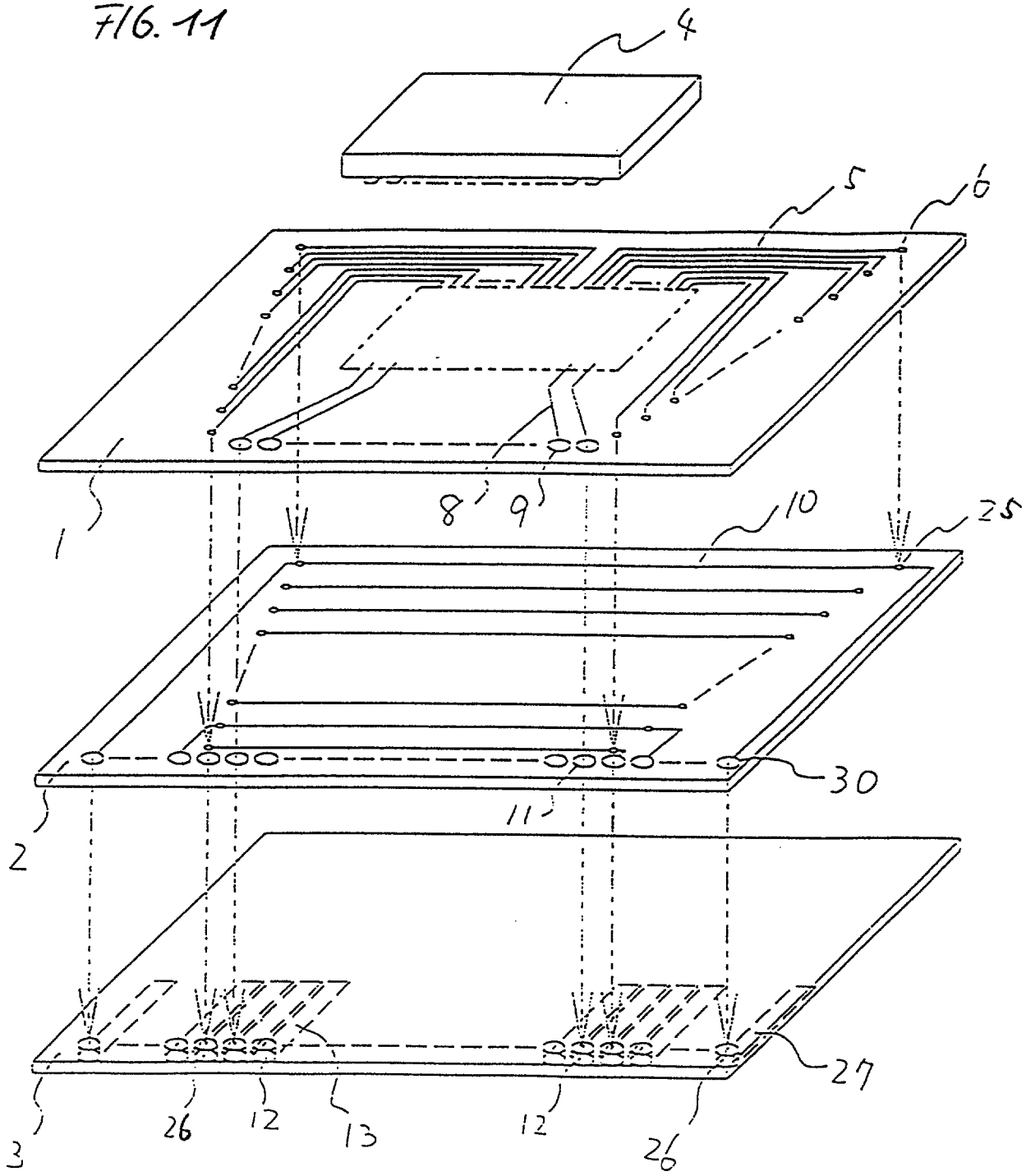


FIG. 12

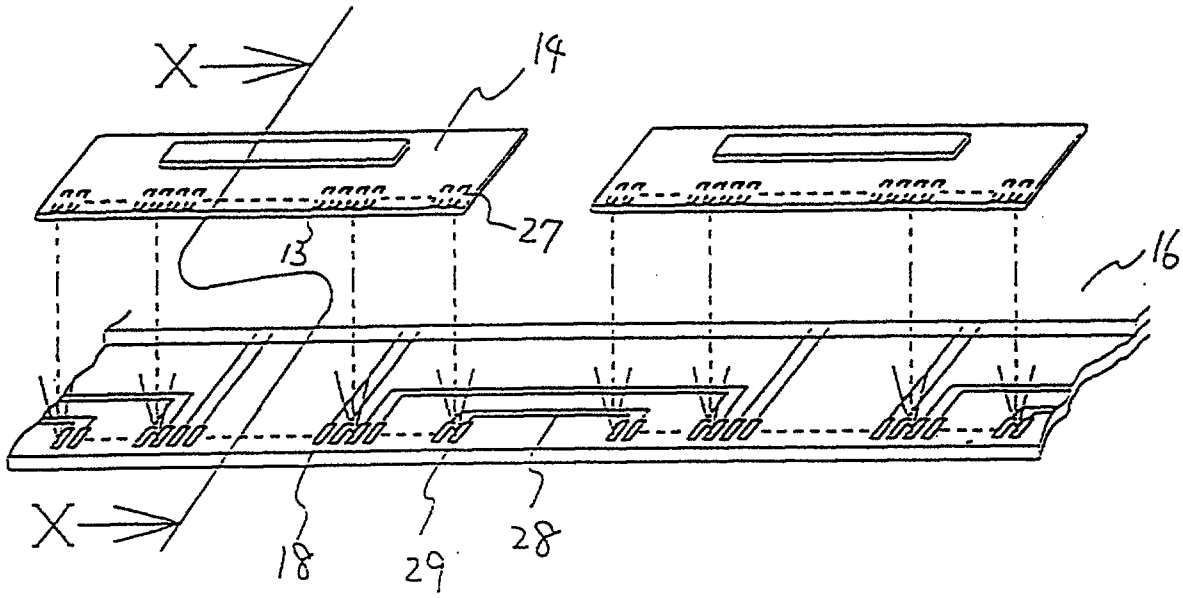


FIG. 13

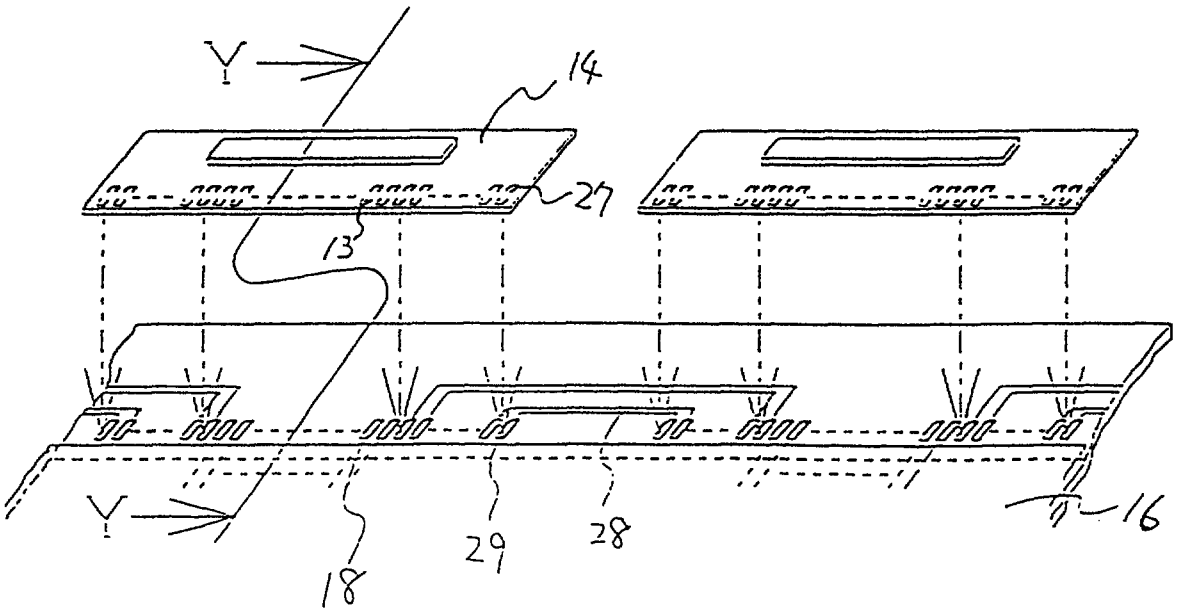


FIG. 15

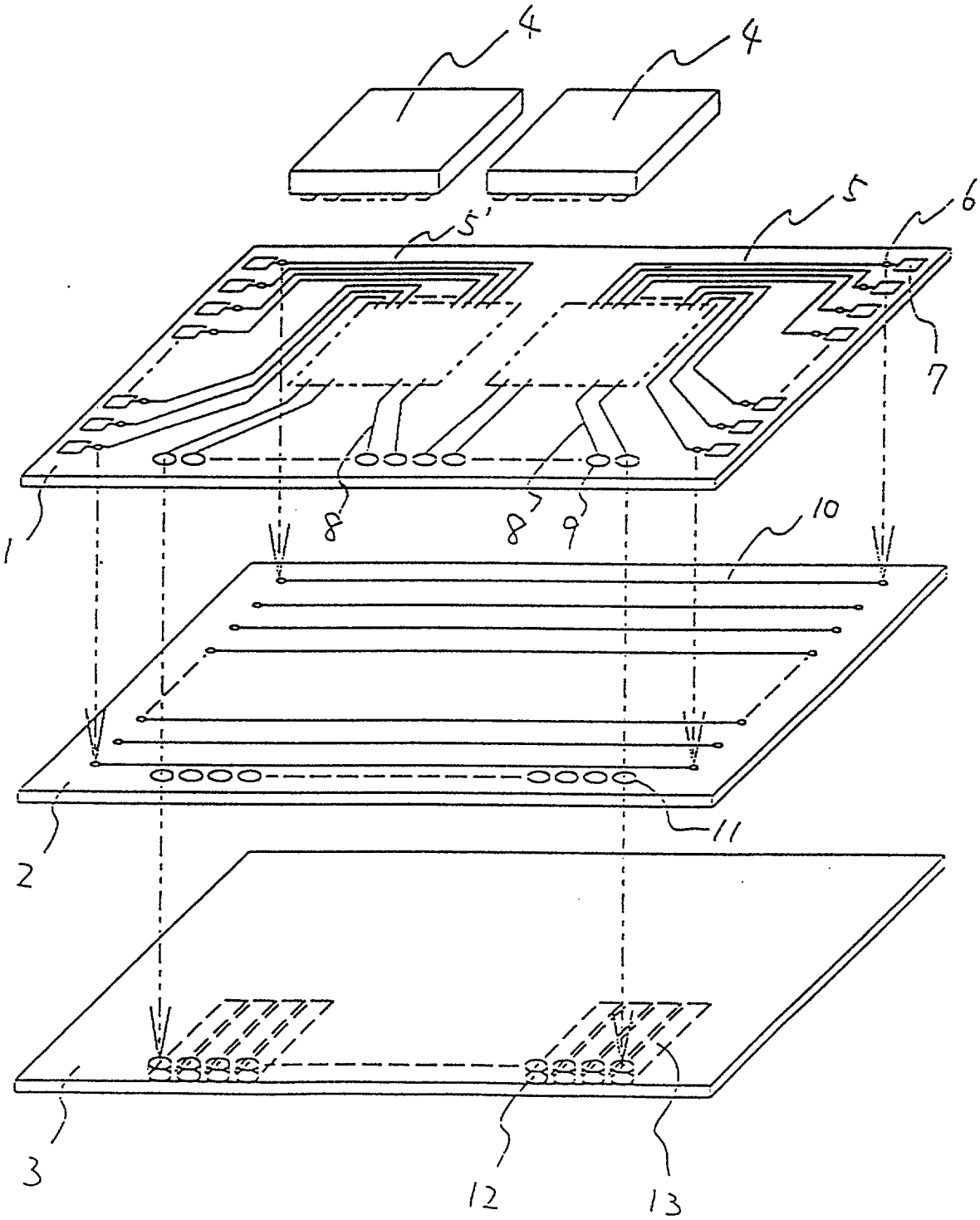


FIG. 16

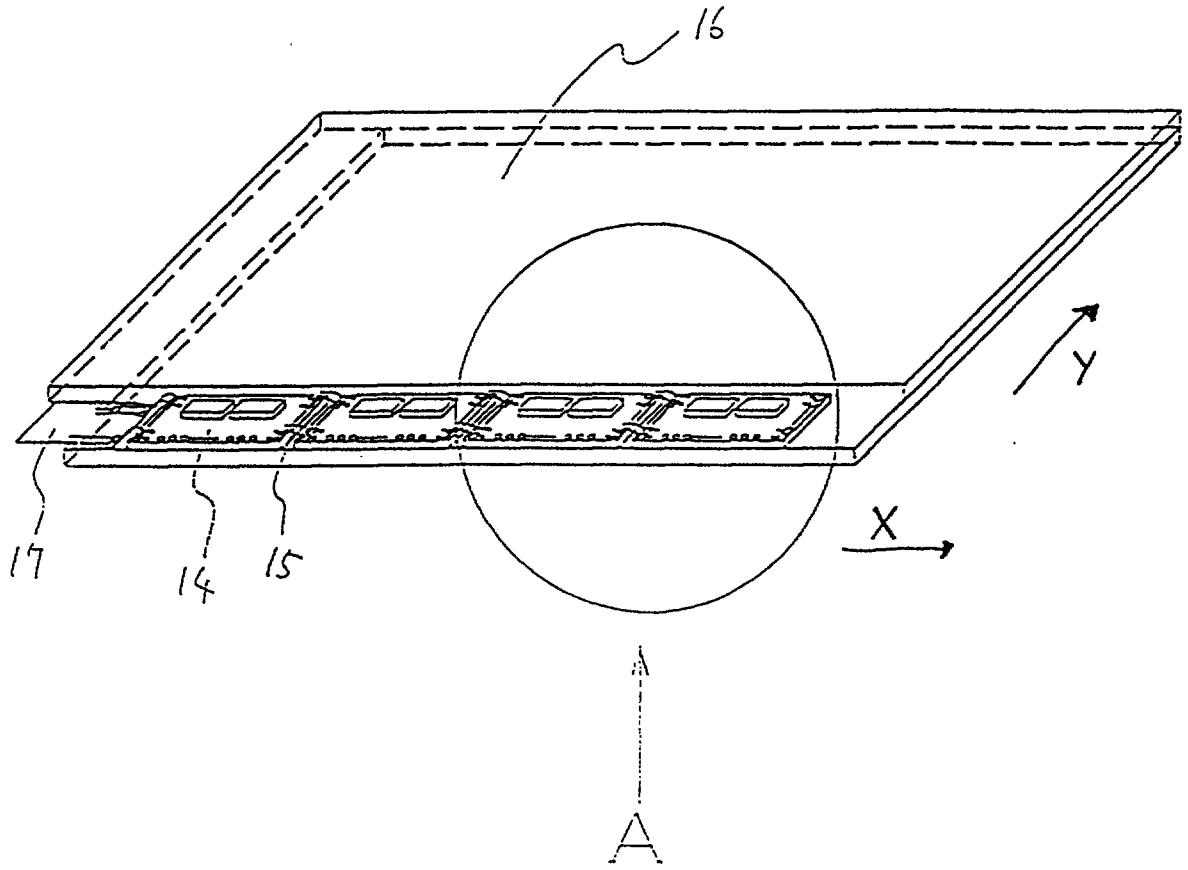


FIG. 20

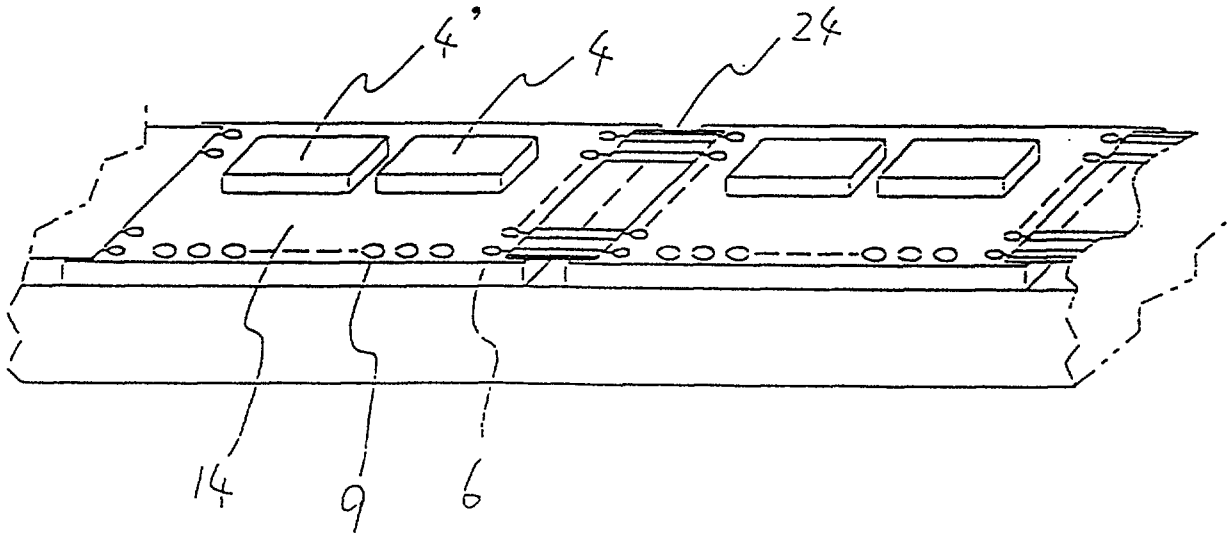


FIG.17

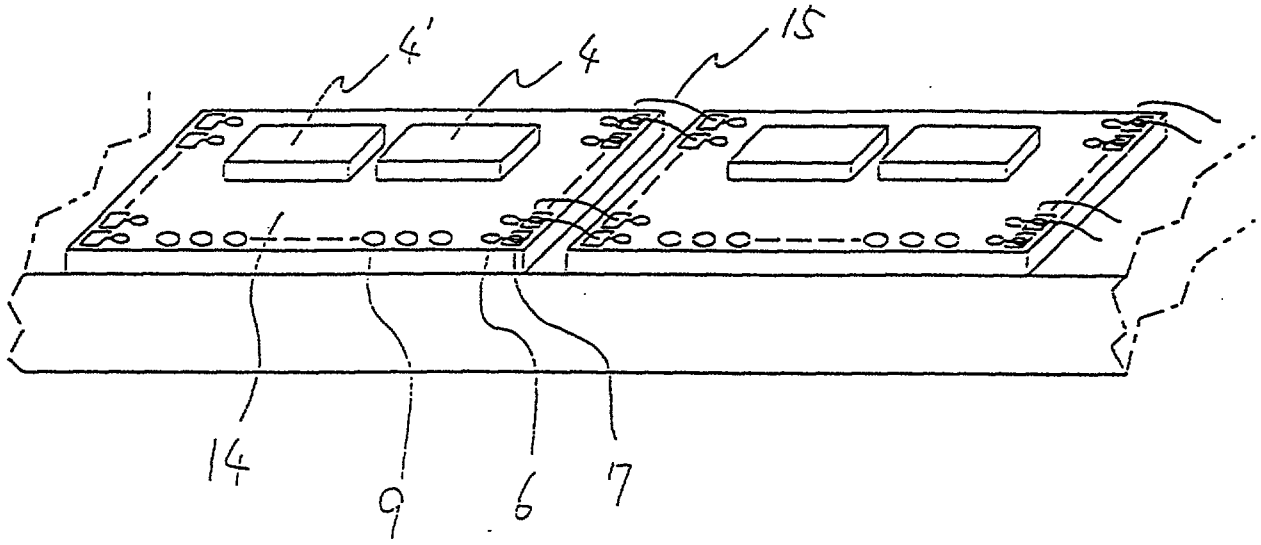


FIG.18

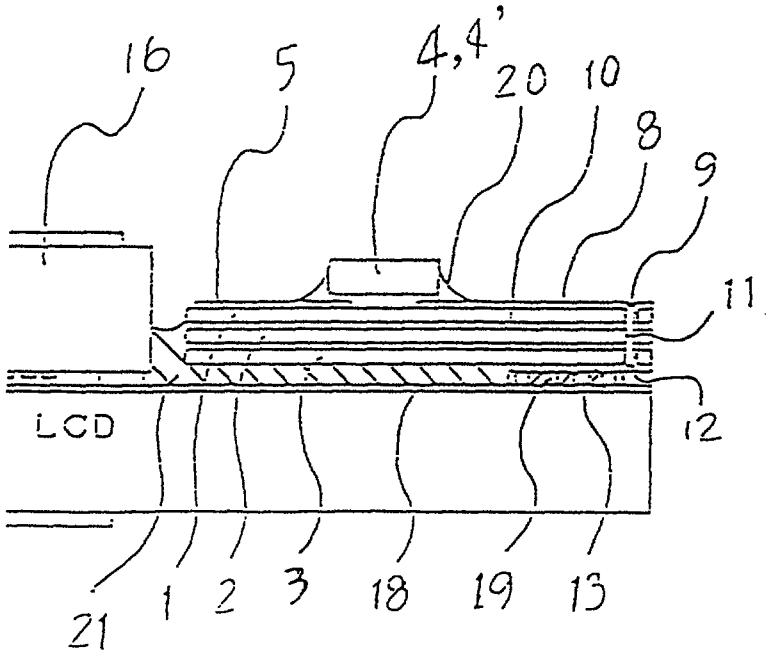


FIG. 19

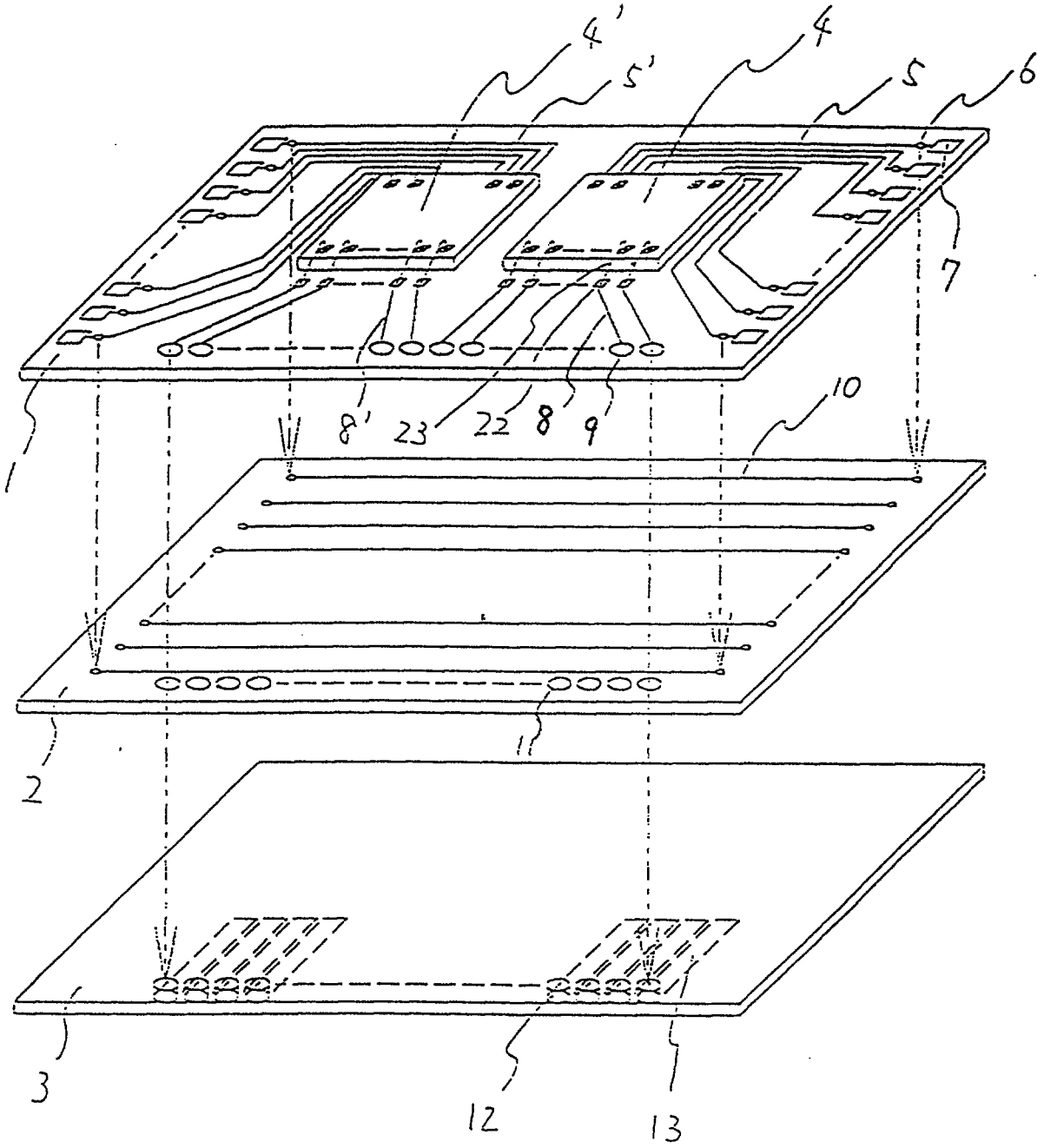


FIG. 21

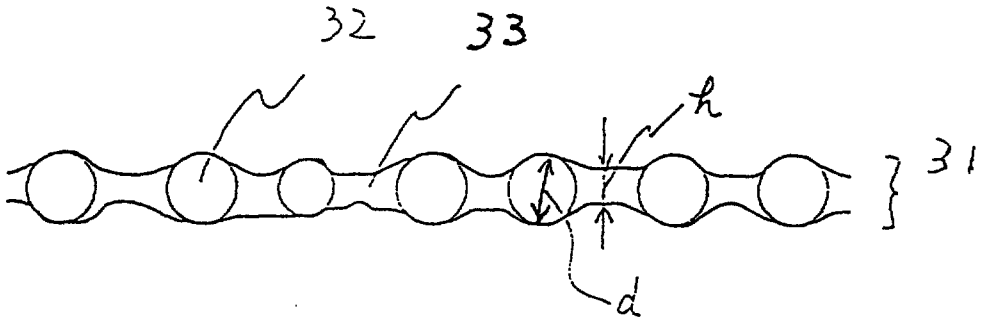


FIG. 22

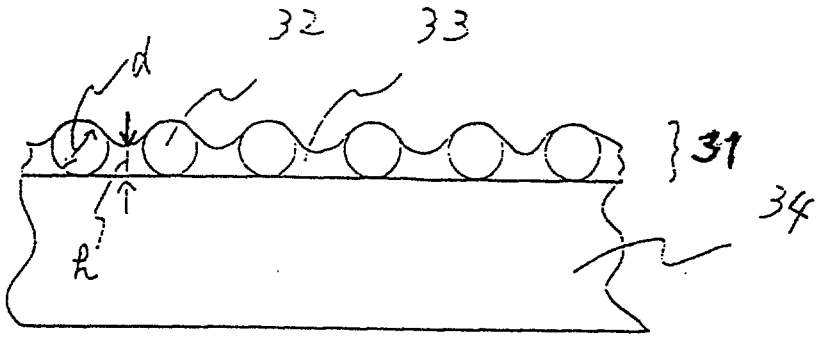


FIG. 23

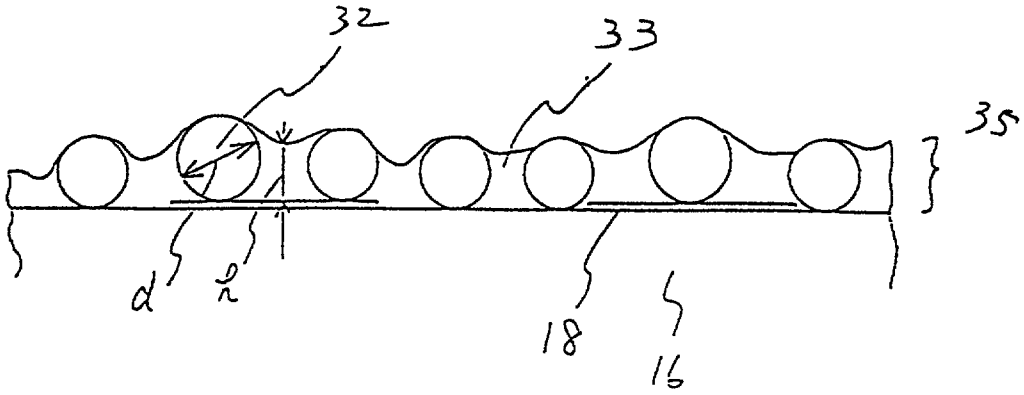


FIG. 24

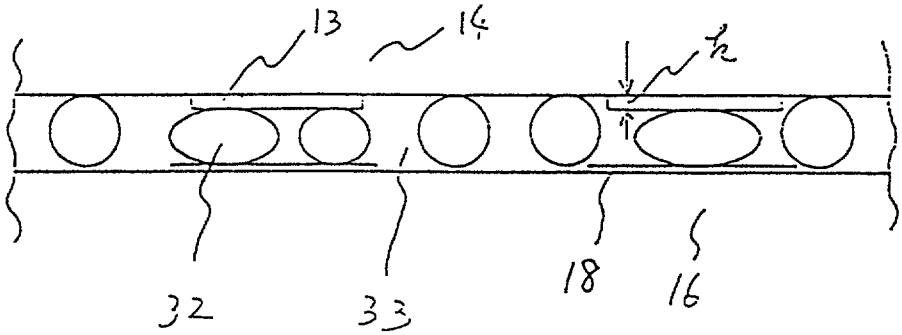


FIG. 25

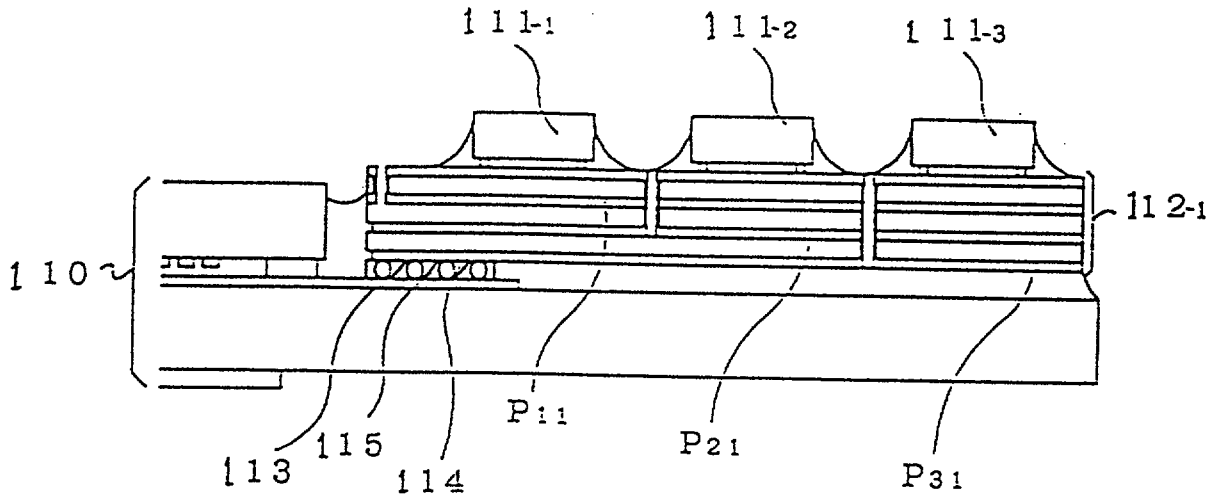

111-1
111-2
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112-1
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113
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114
P11
P21
P31

FIG. 26

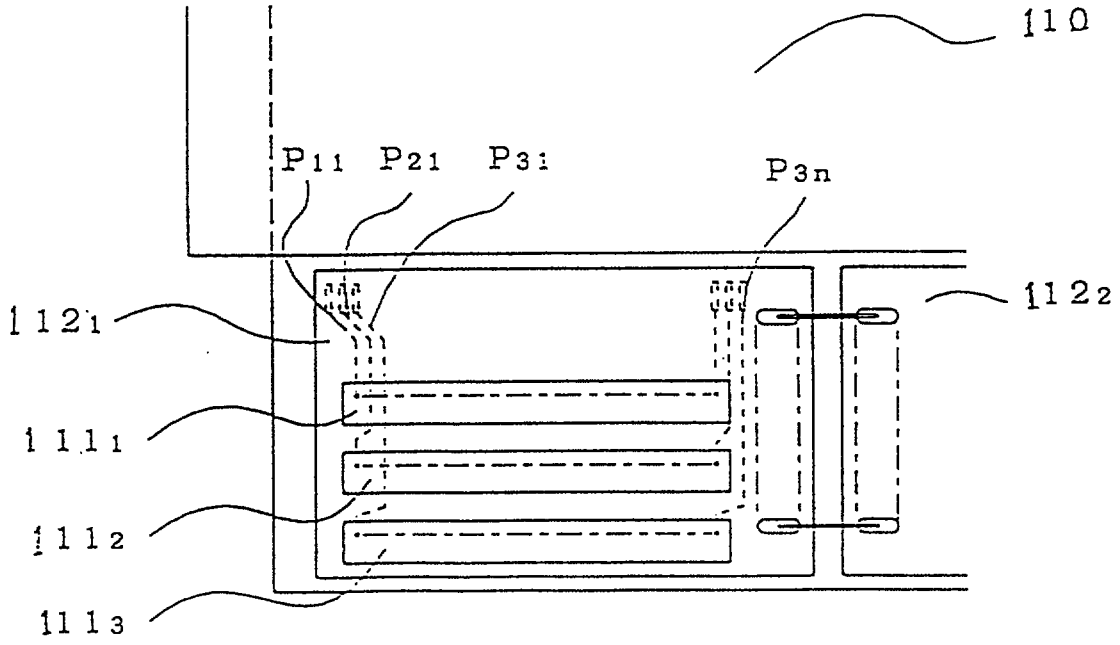

110
P11
P21
P31
P3n
112₁
112₂
111₁
111₂
111₃

FIG. 27

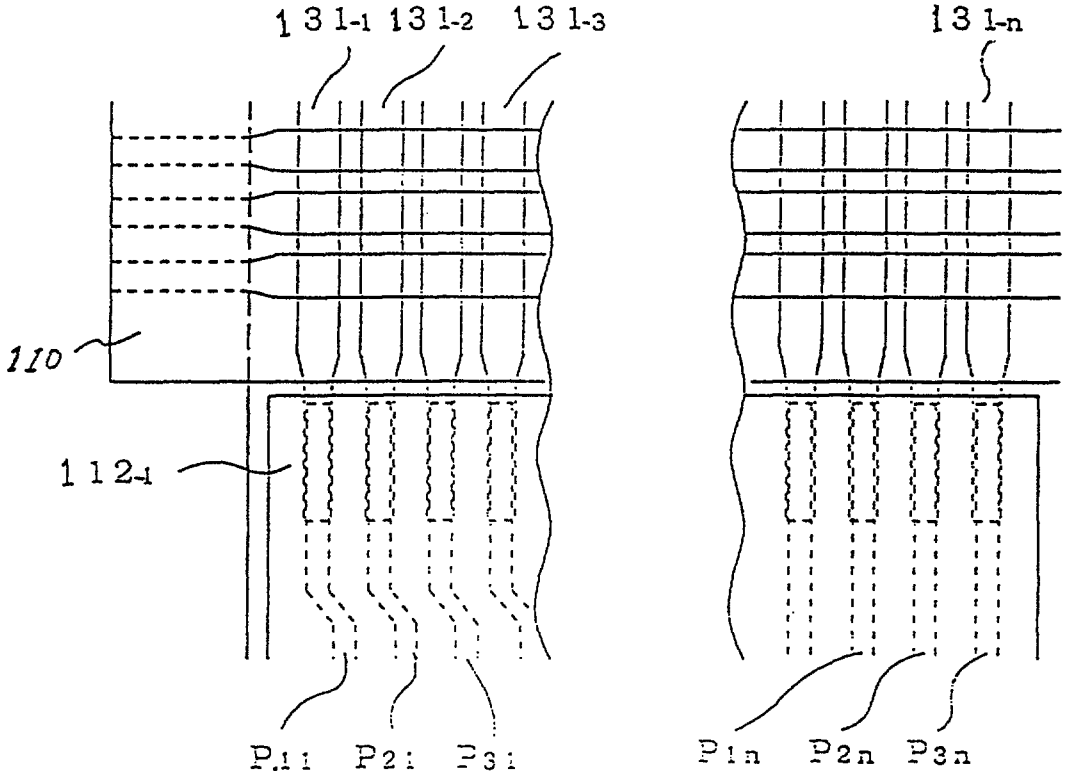

131-1
131-2
131-3
131-n
110
112-1
P11
P21
P31
P1n
P2n
P3n

FIG. 28

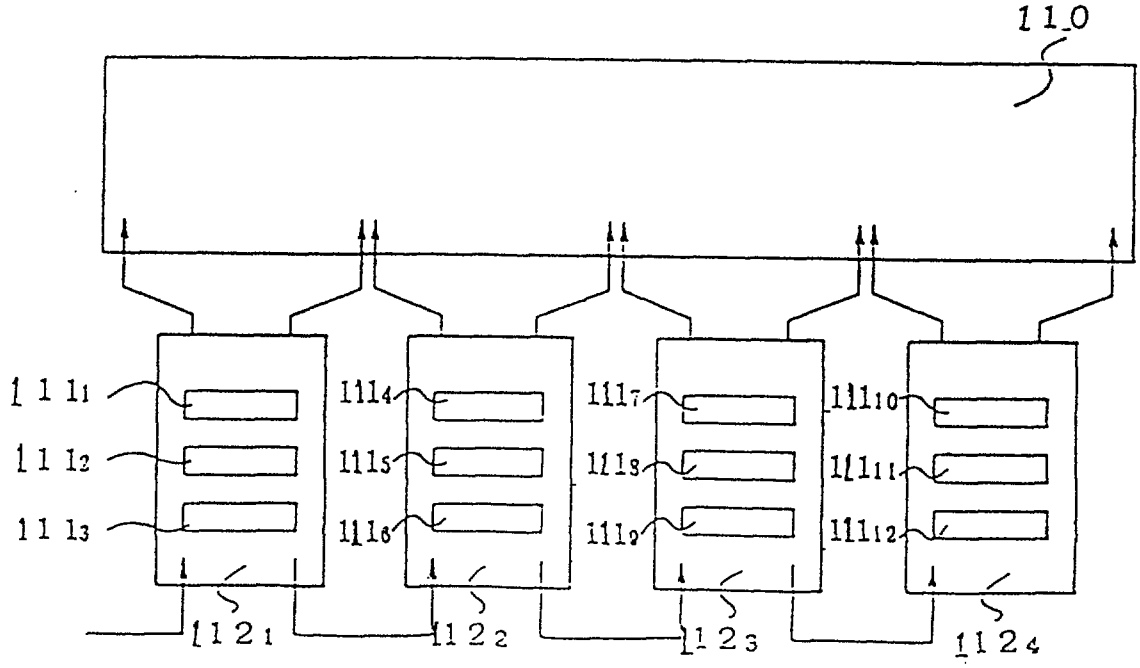

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FIG. 29

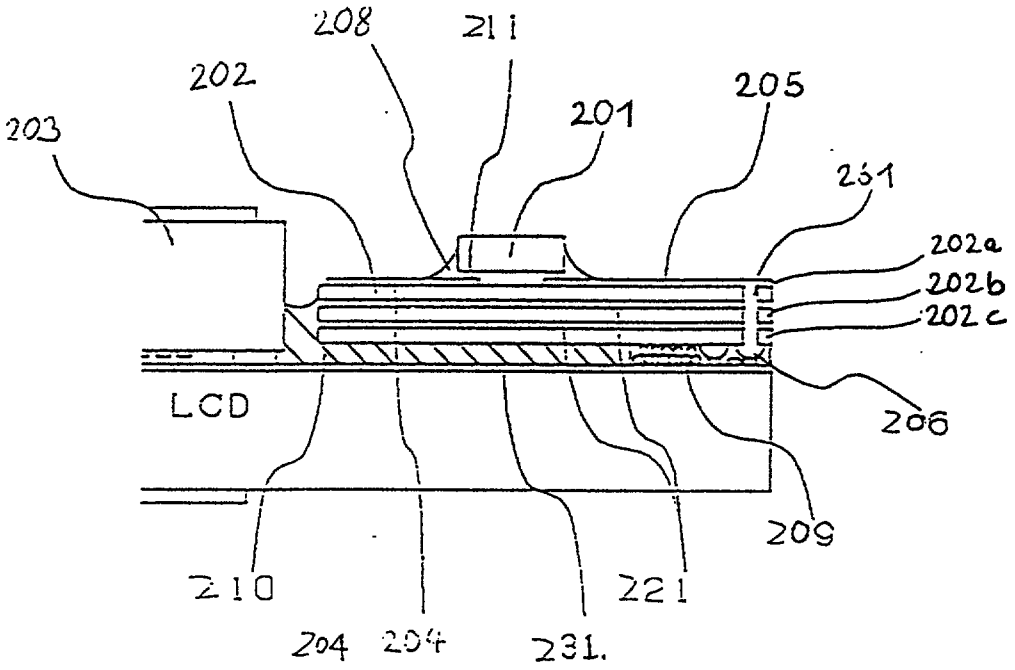

208
211
202
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251
202a
202b
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LCD
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FIG. 30

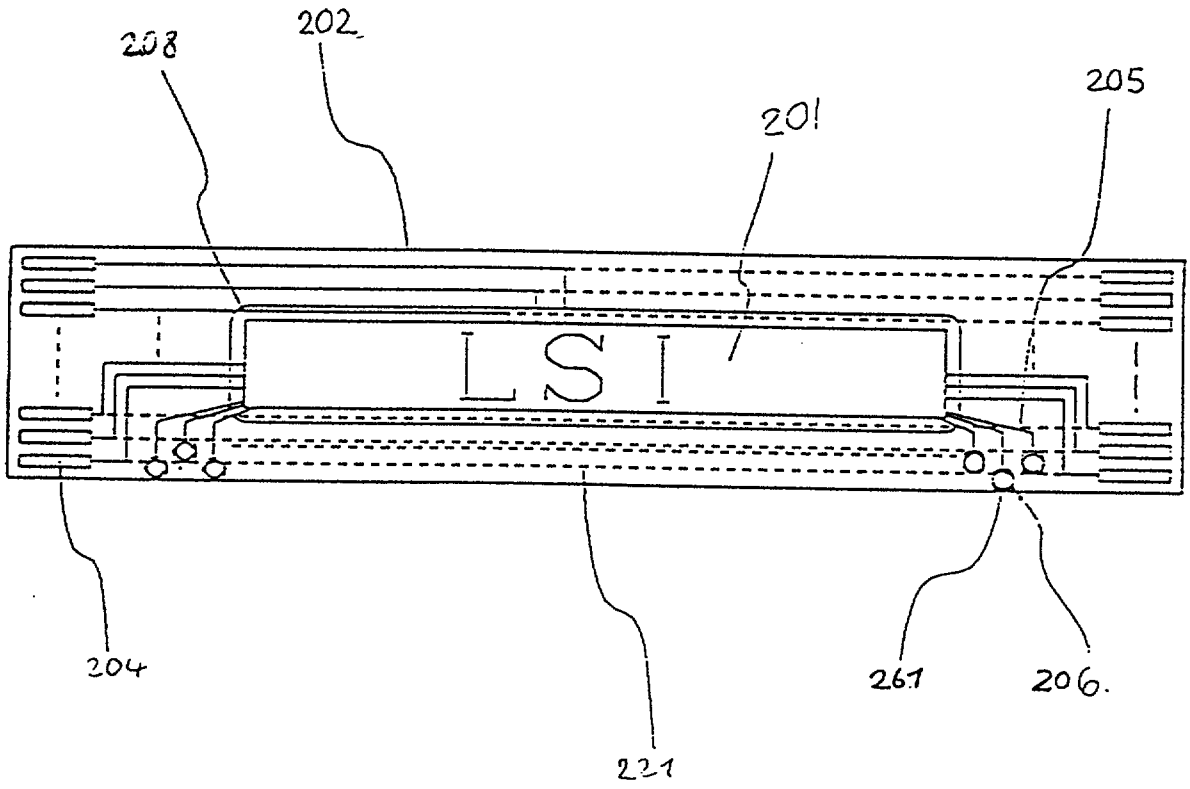

208
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FIG. 31

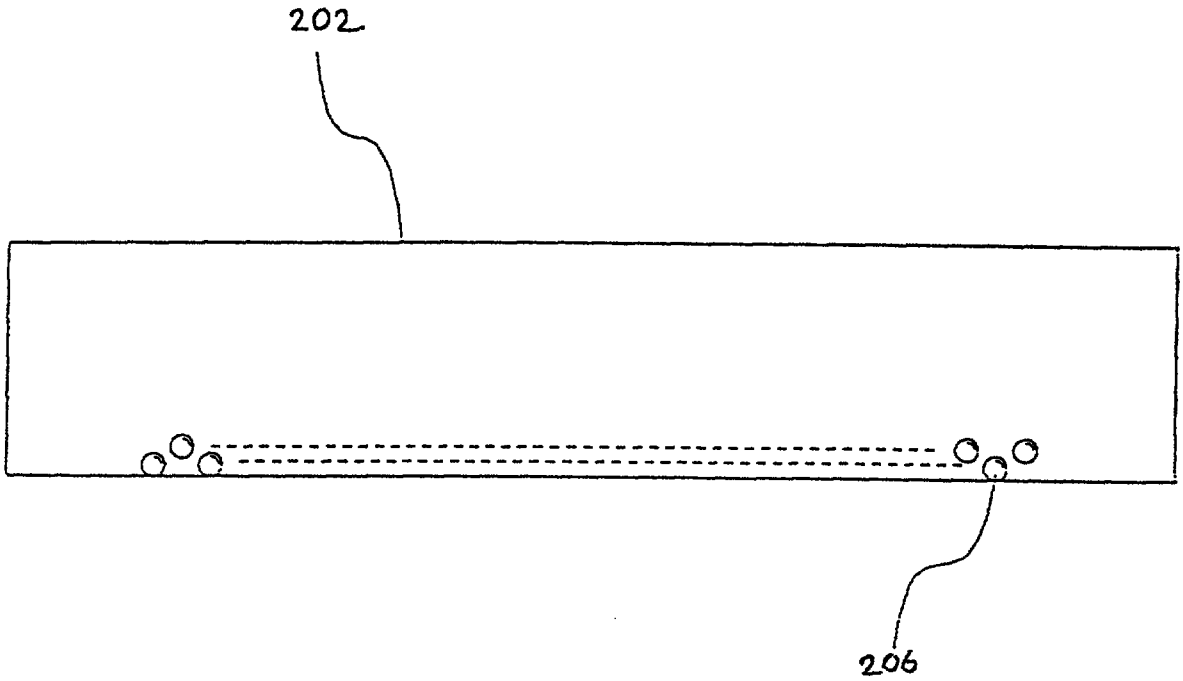


FIG. 32

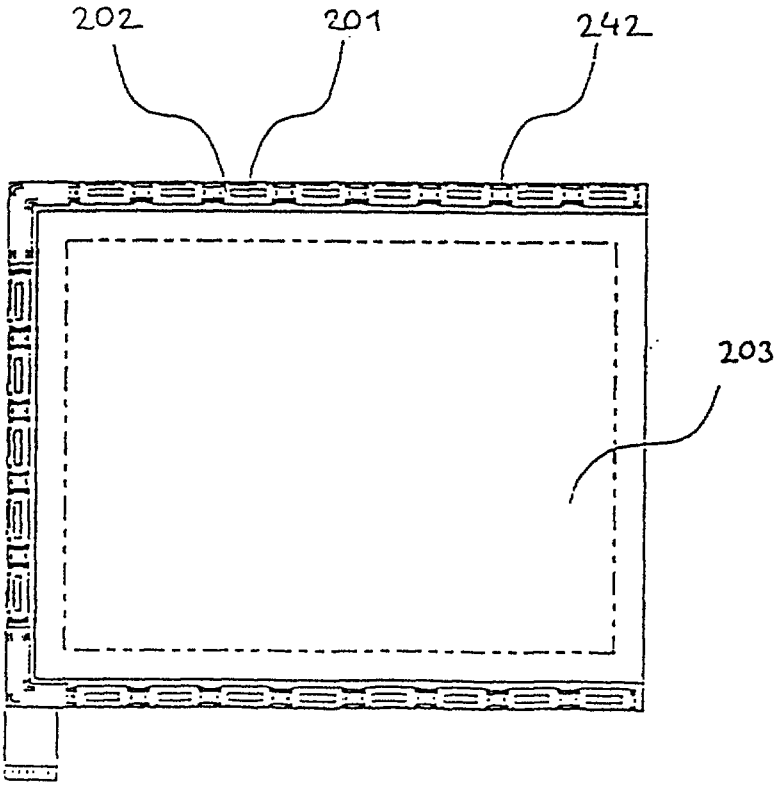


FIG.33

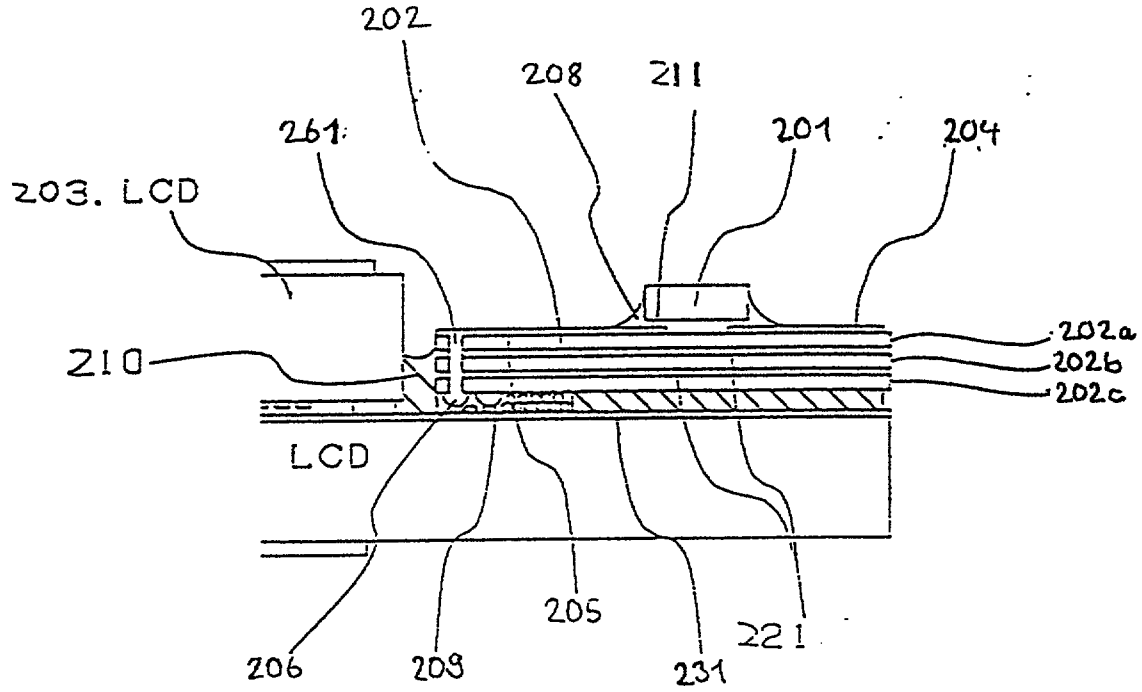

202
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203. LCD
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LCD
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FIG.34

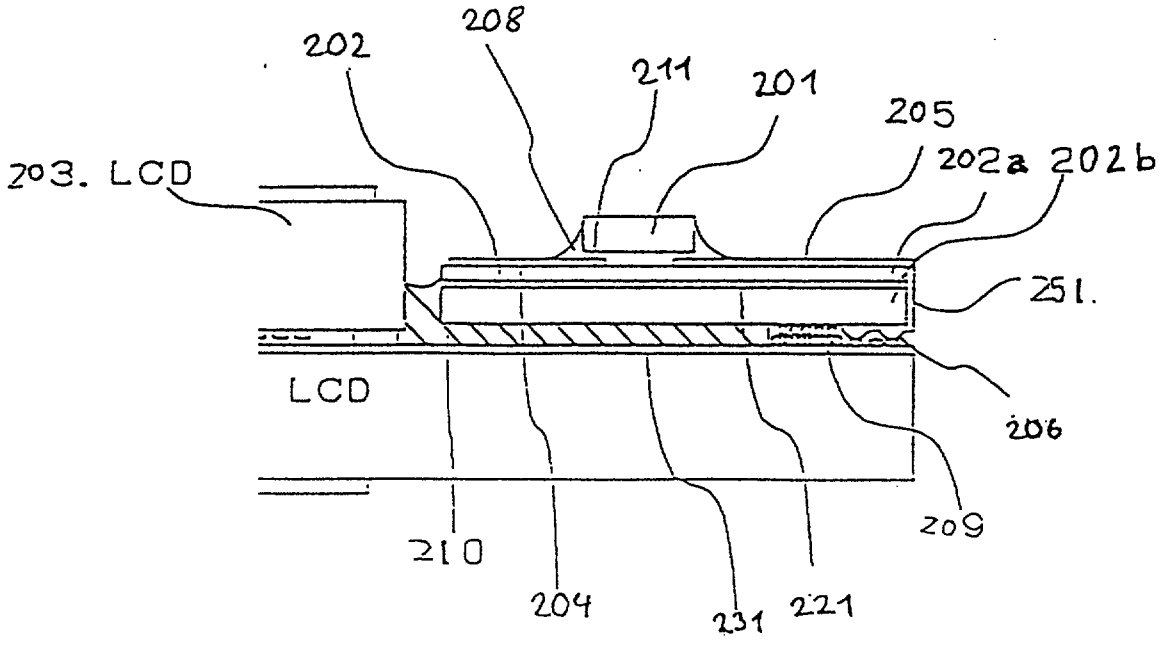

208
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203. LCD
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LCD
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FIG. 35

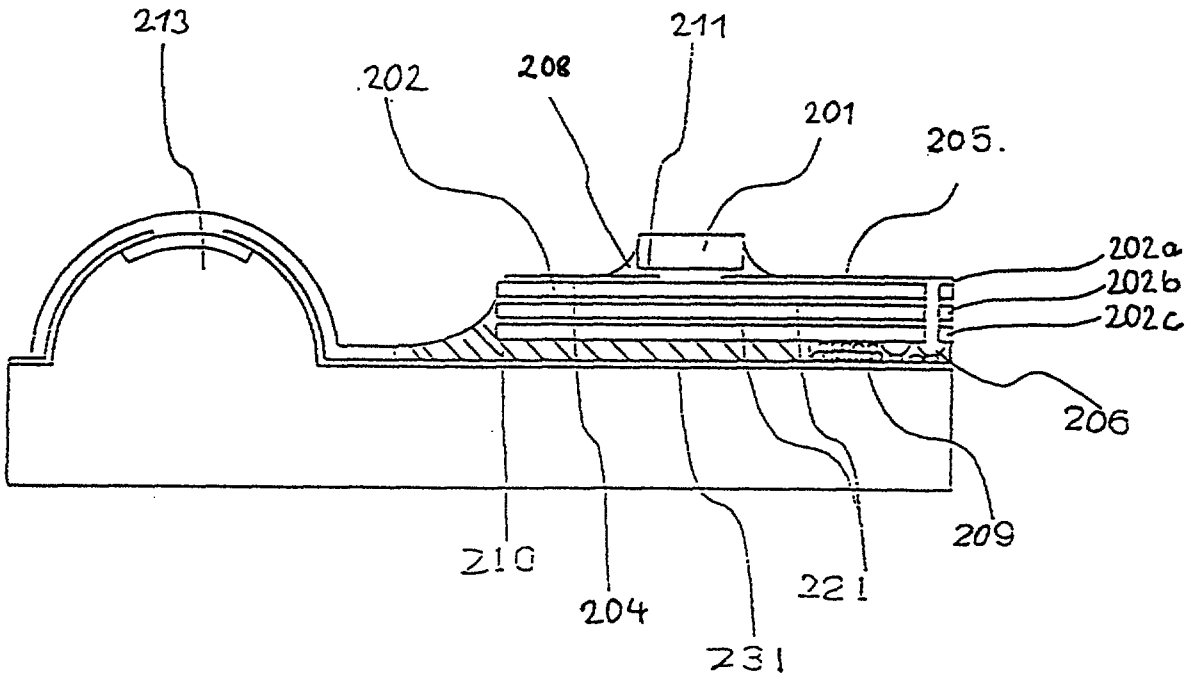

213
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FIG. 36

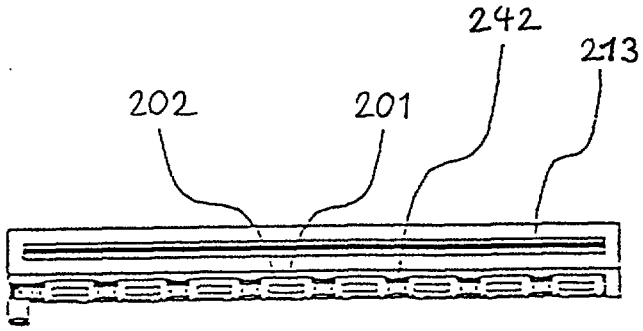

242
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FIG.37

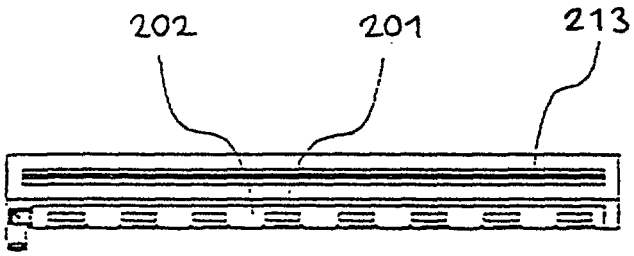

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FIG.38

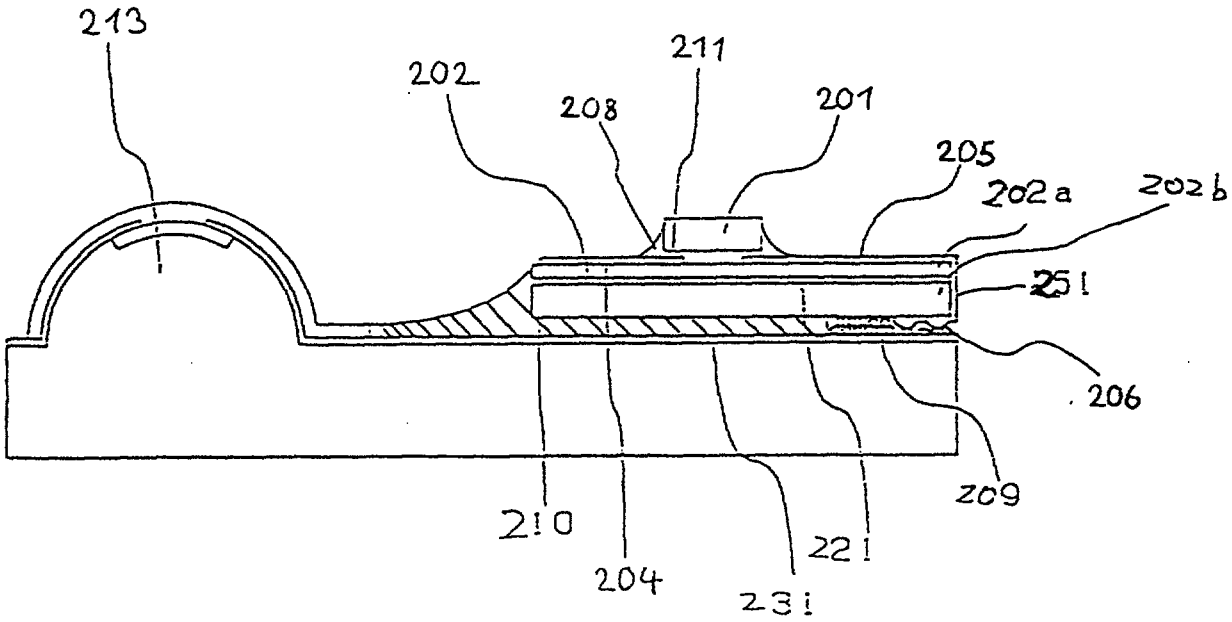

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FIG.39

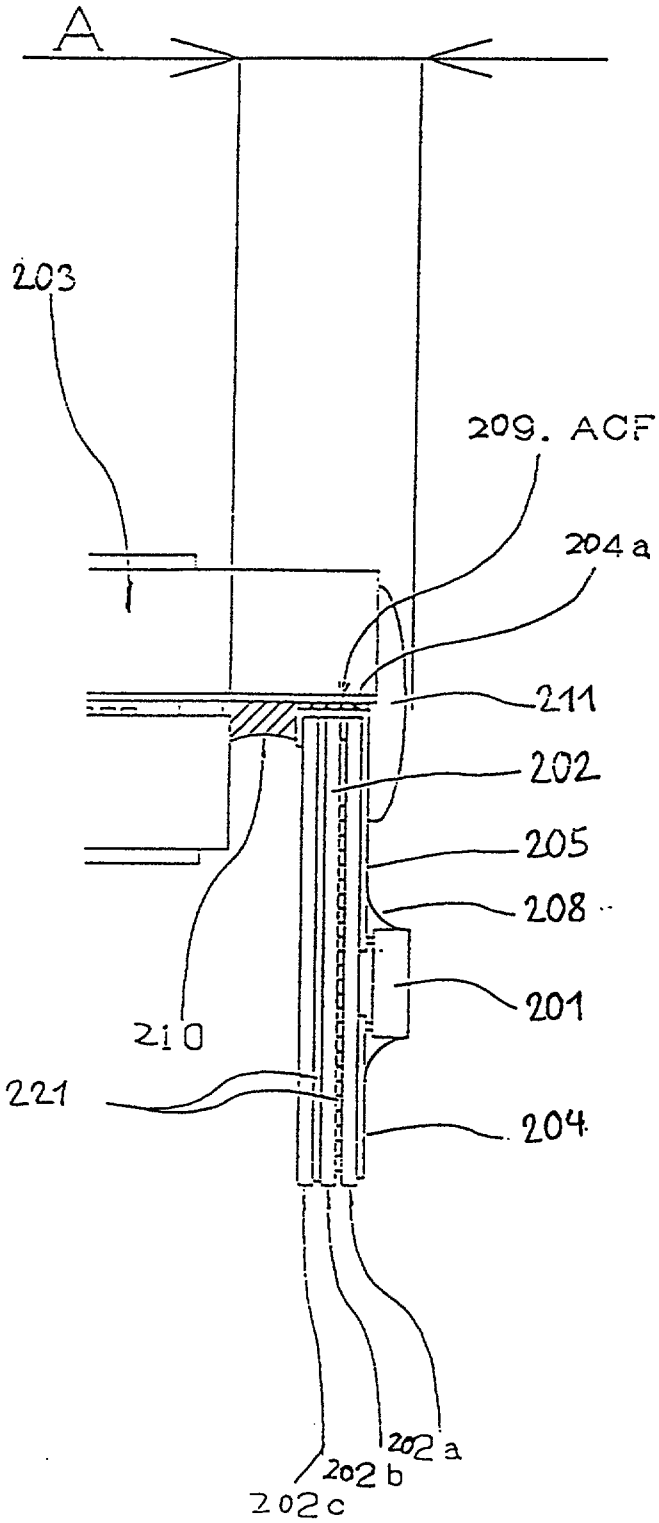

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FIG. 40

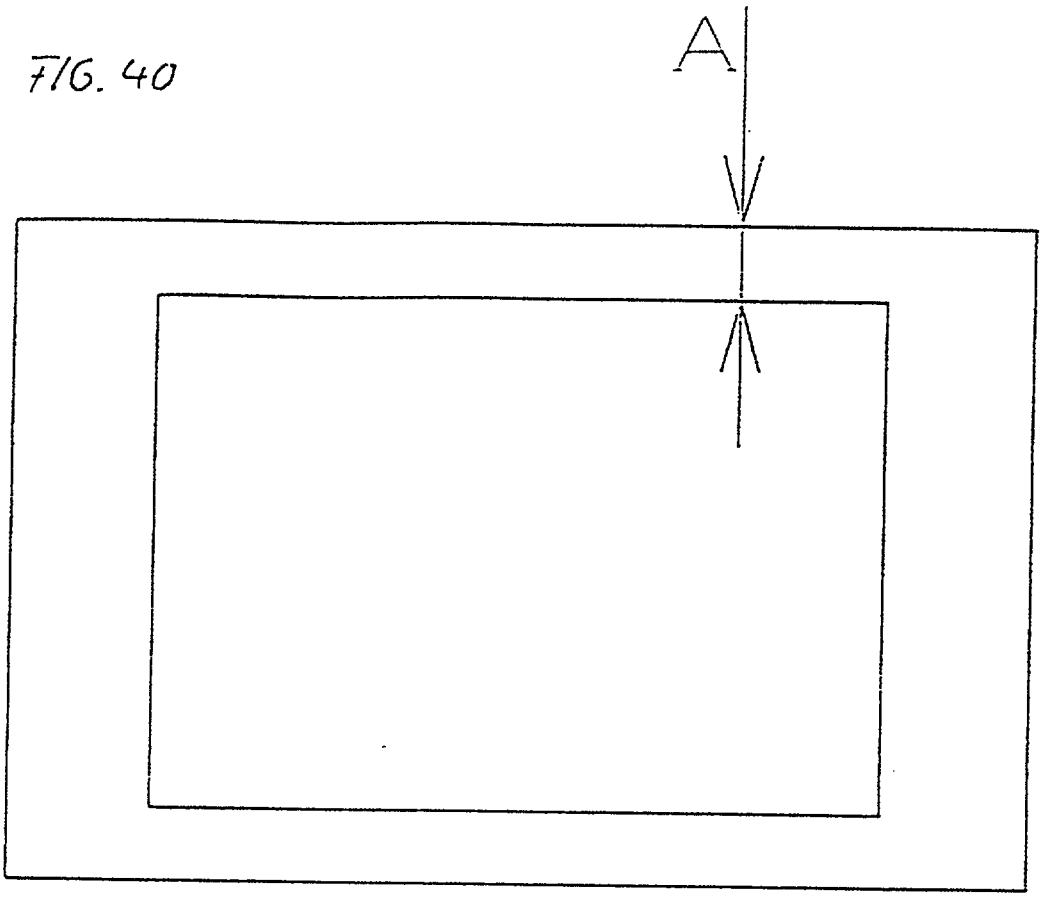


FIG. 41

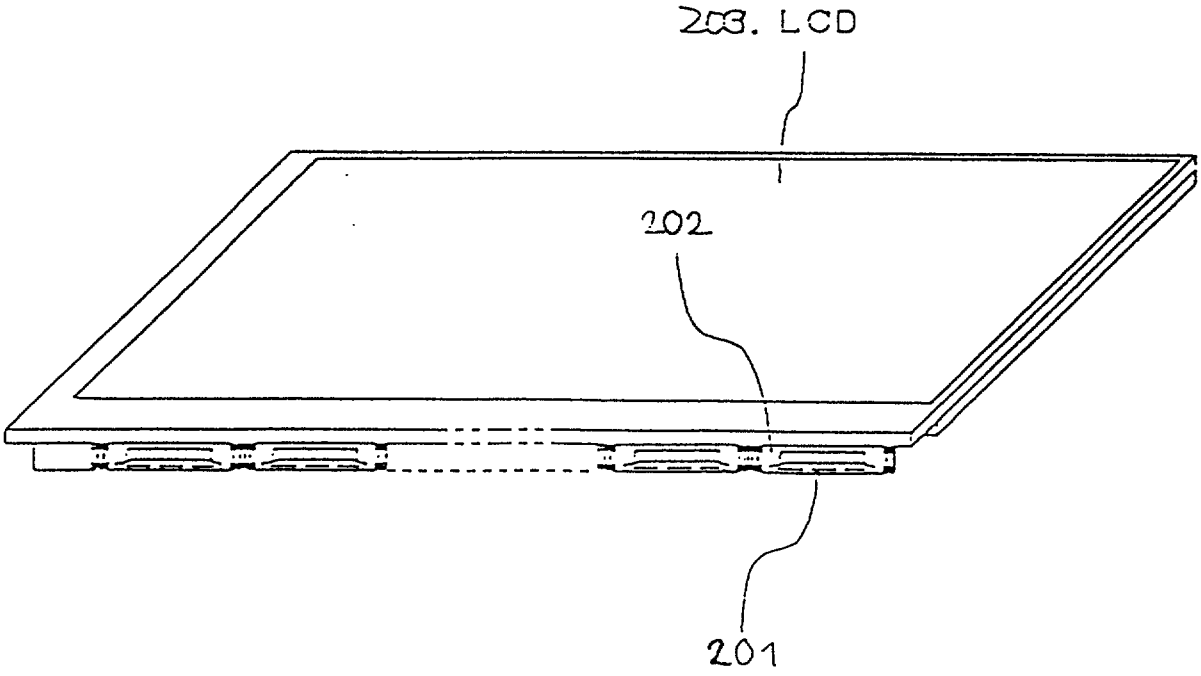


FIG. 42

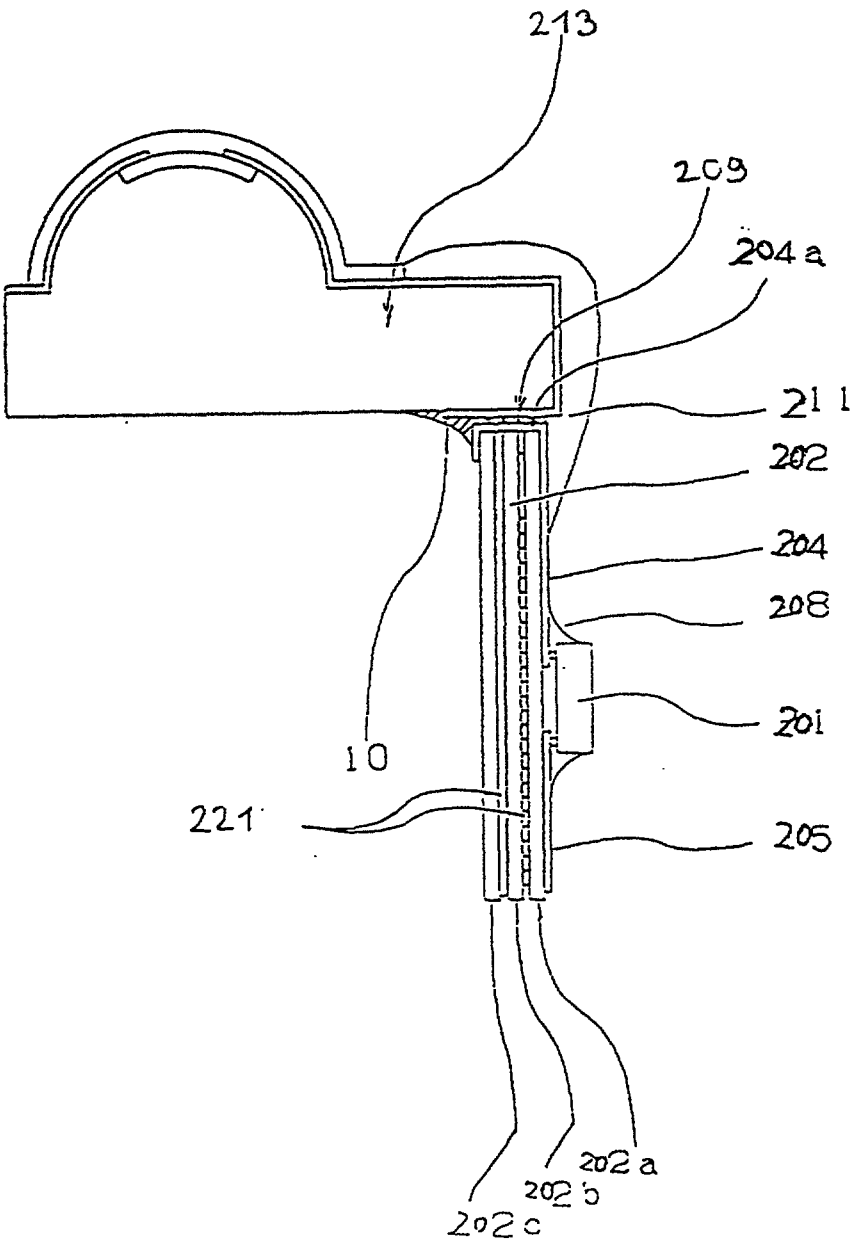


FIG. 43

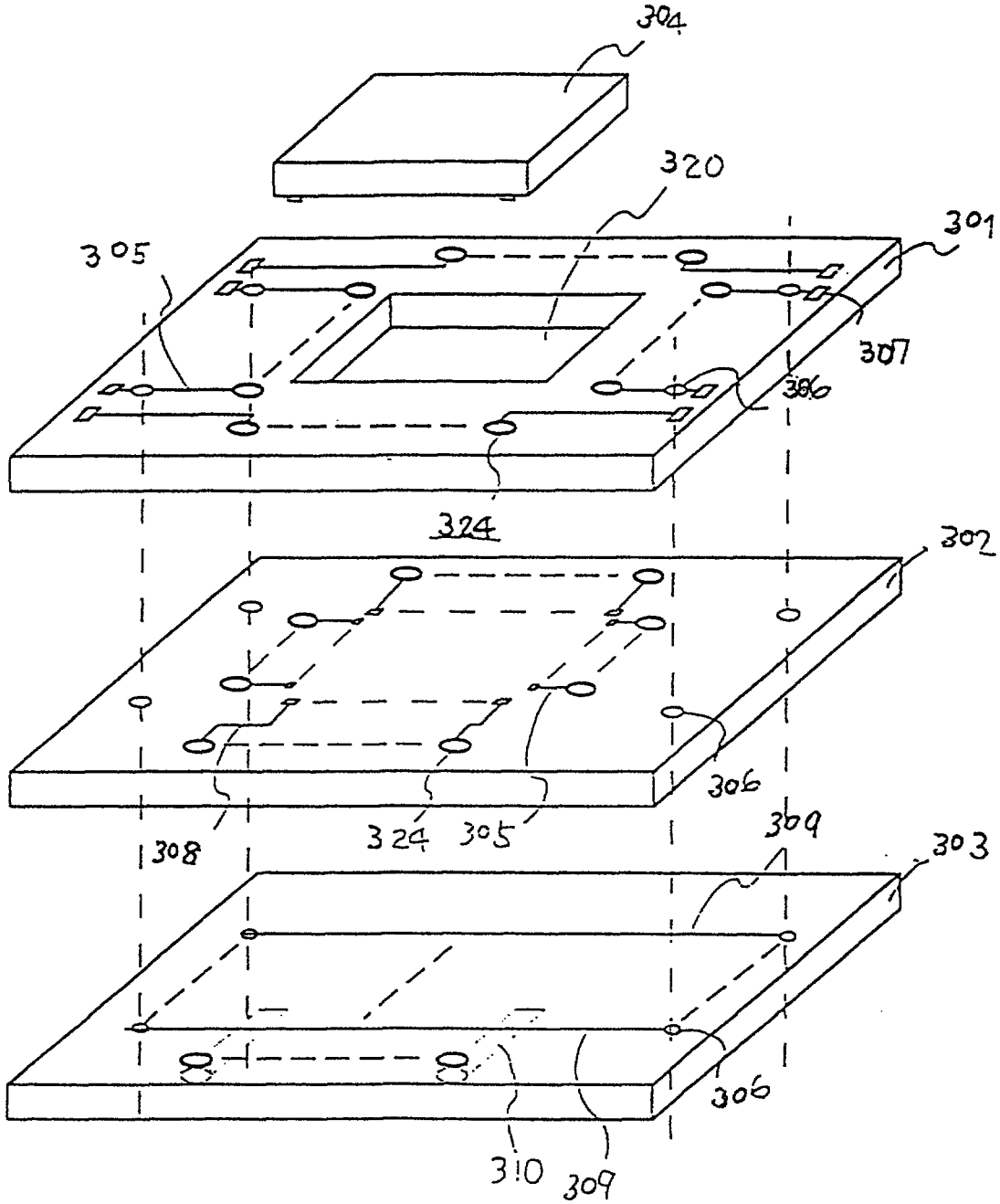

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FIG. 44

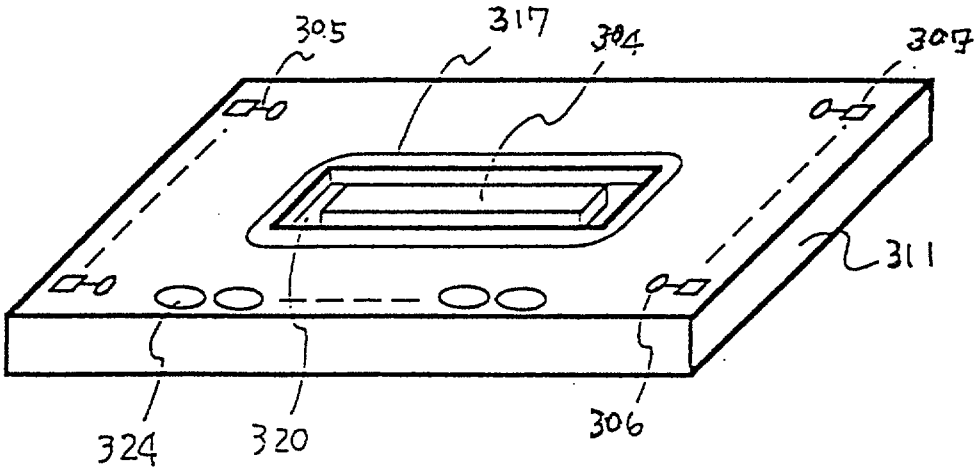


FIG. 45

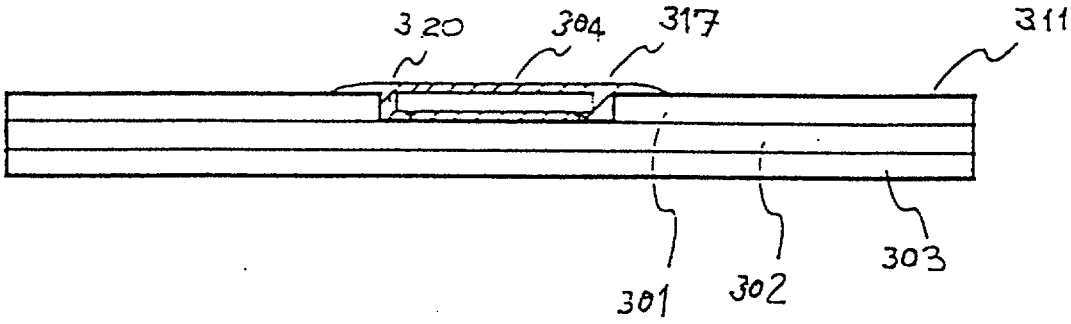


FIG. 46

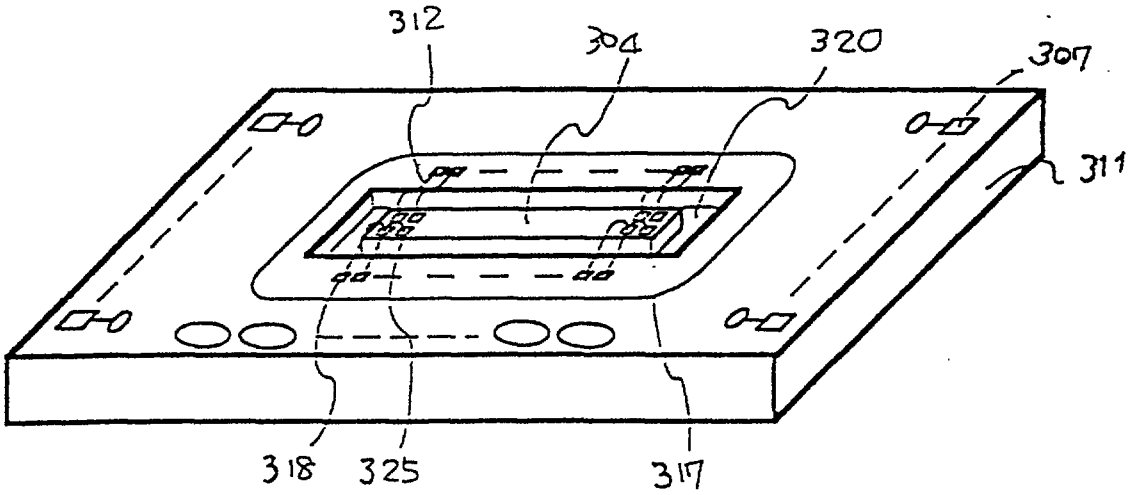


FIG. 47

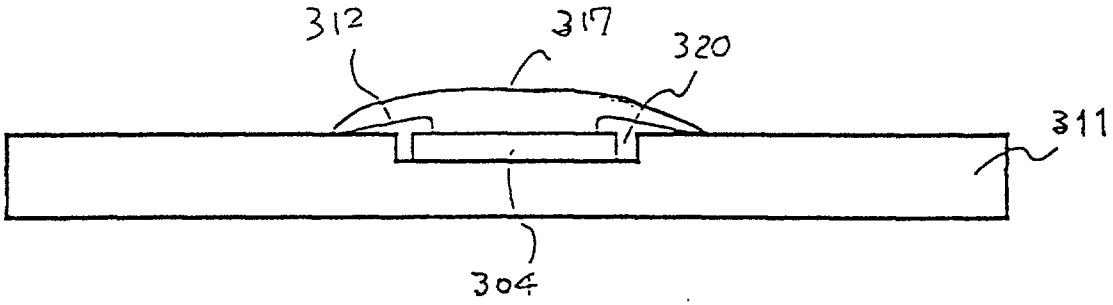


FIG. 48

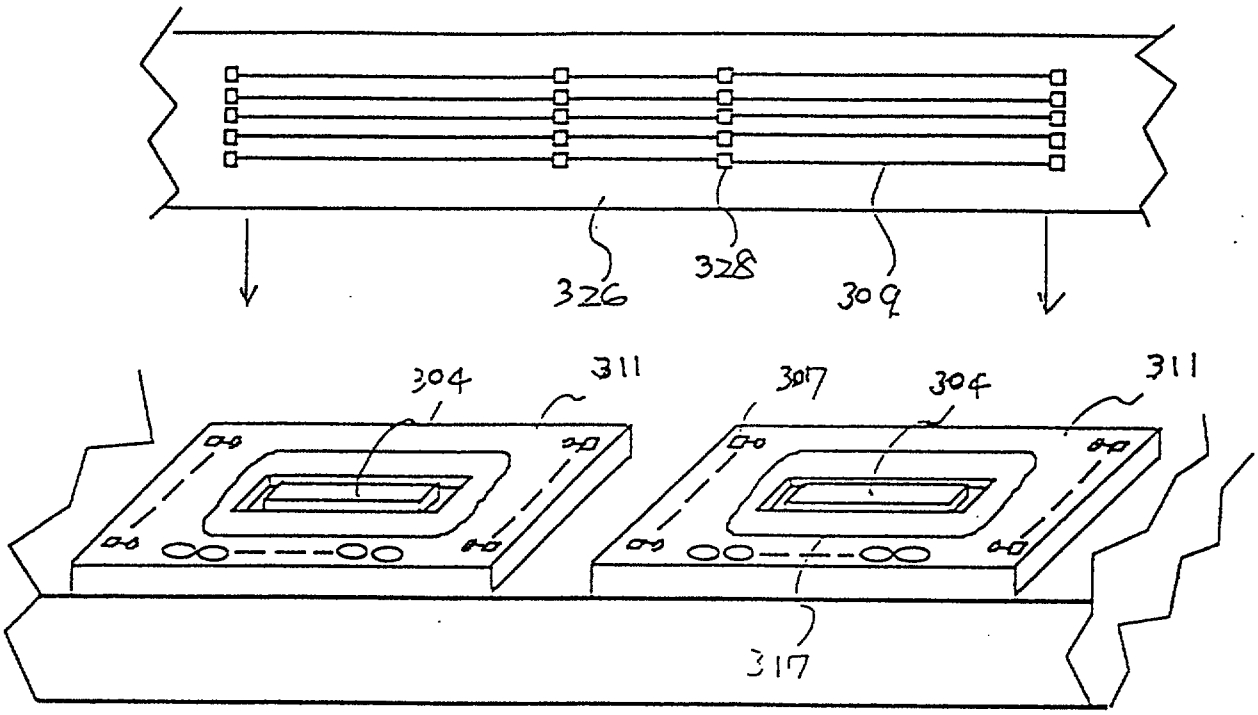


FIG. 49

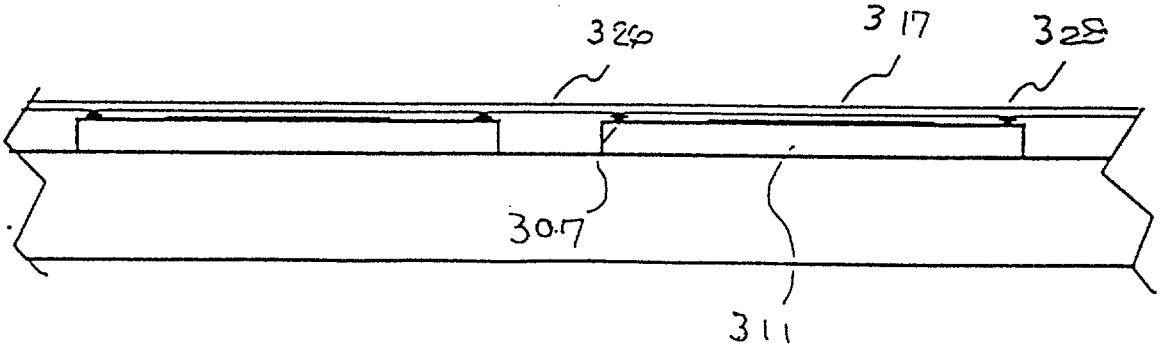


FIG. 50

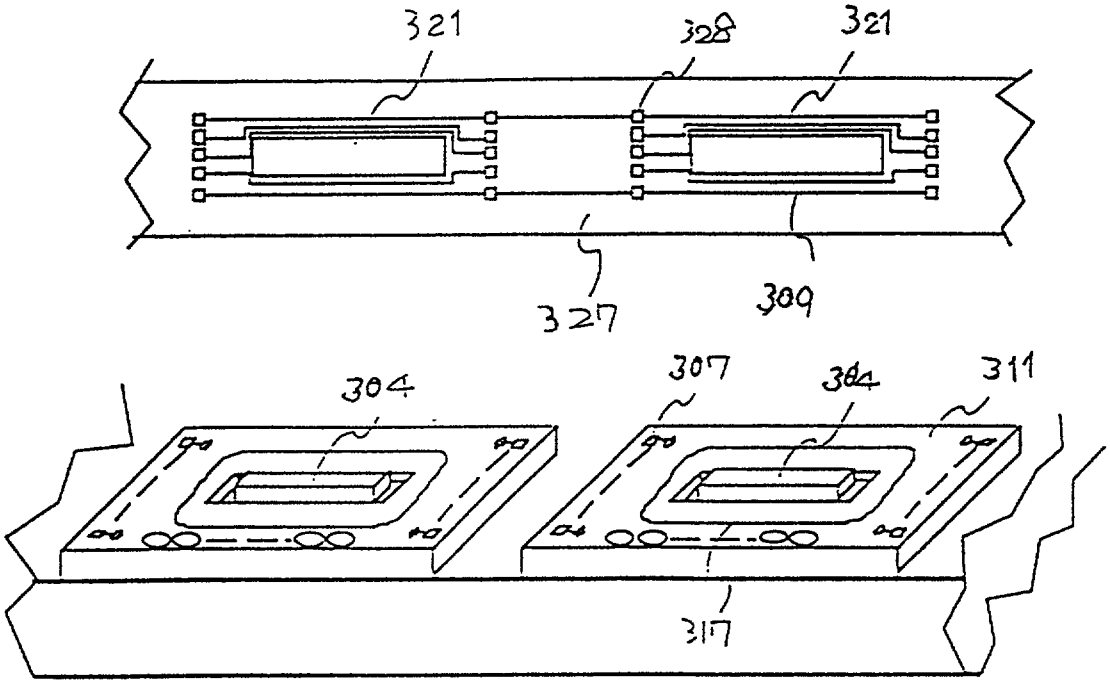


FIG. 51

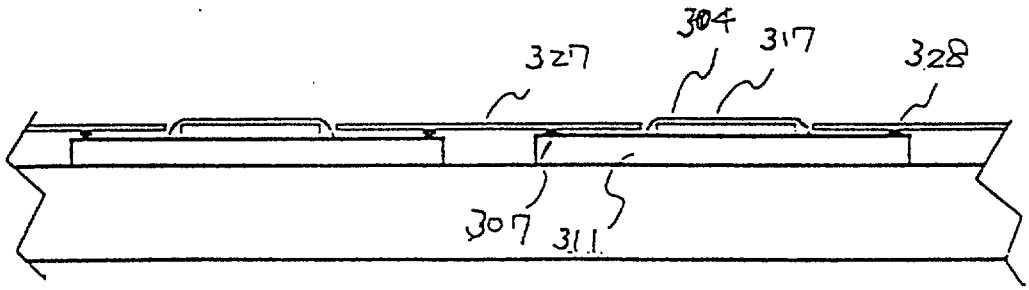


FIG. 52

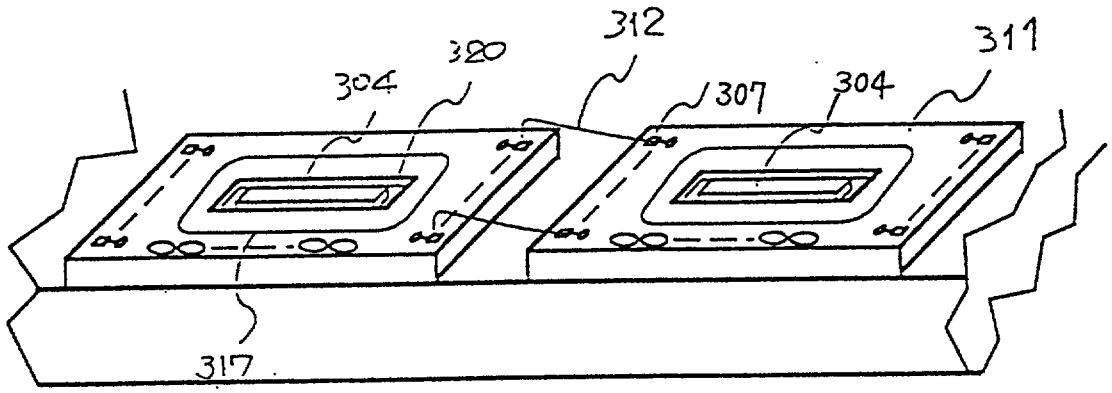

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FIG. 57

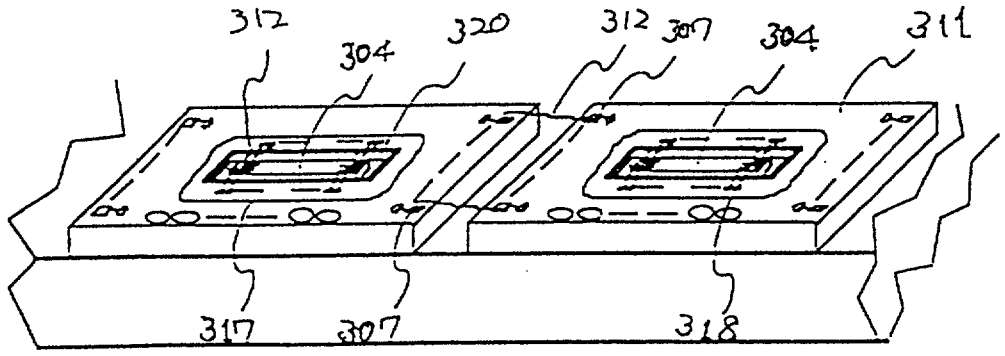

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FIG.53

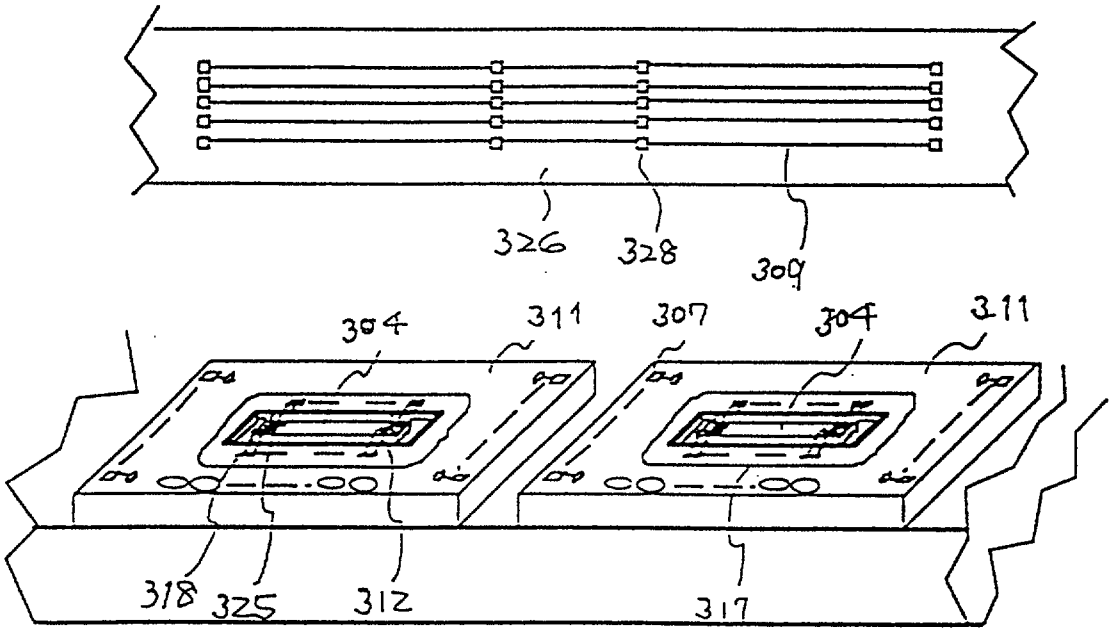

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FIG.54

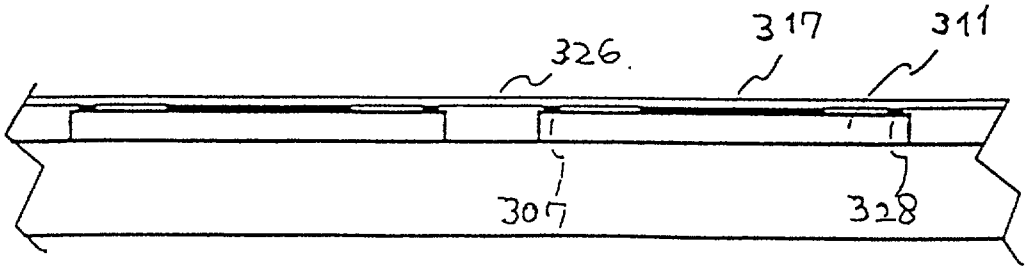

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FIG. 55

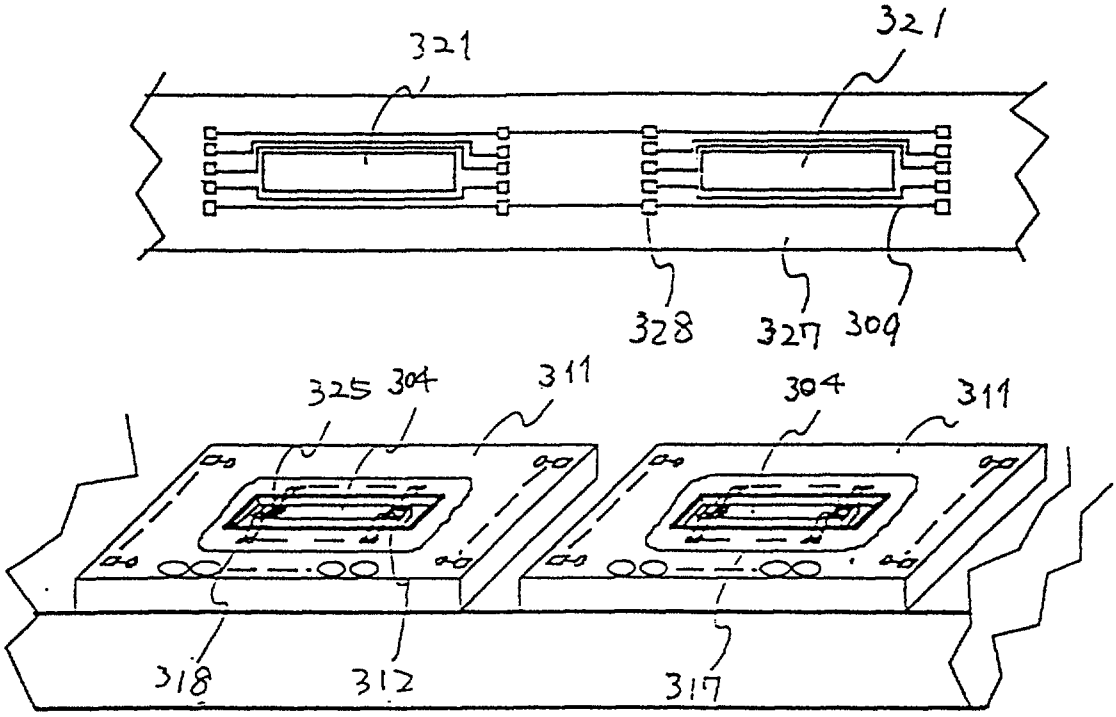

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FIG. 56

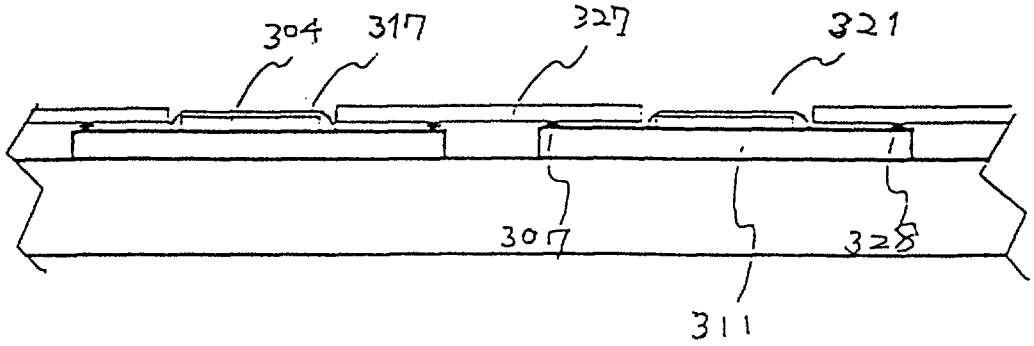

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FIG. 58

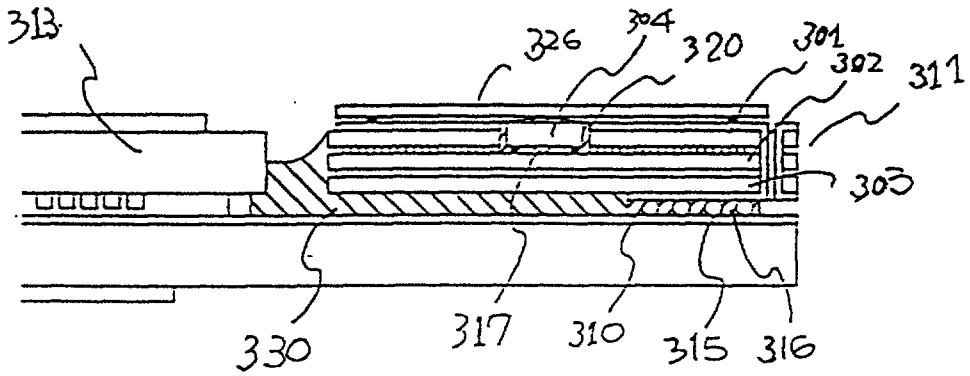

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FIG. 59

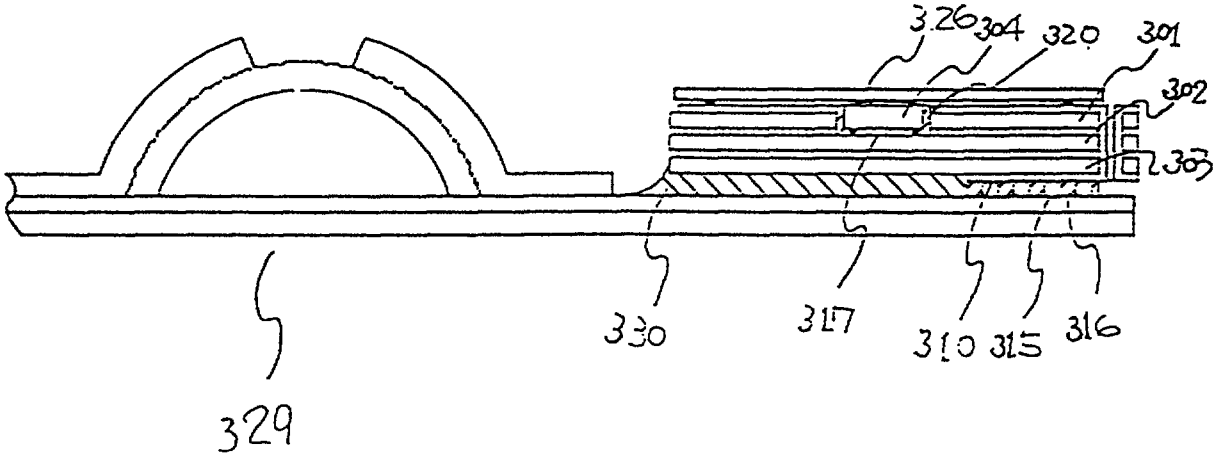

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FIG. 60

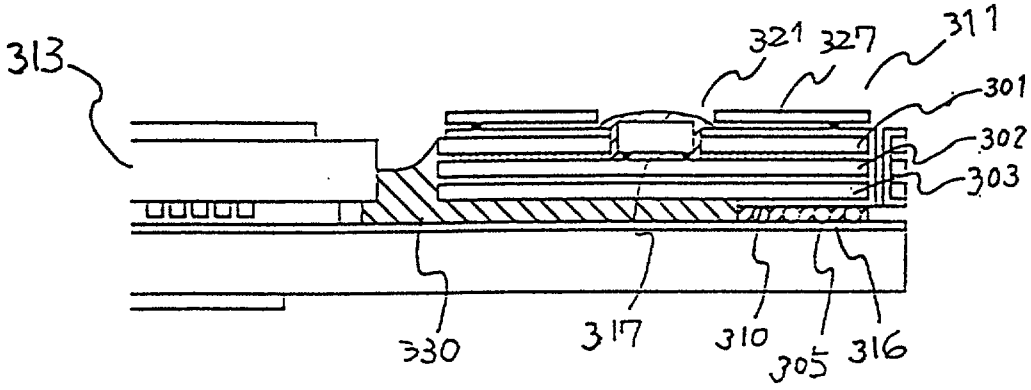

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FIG. 61

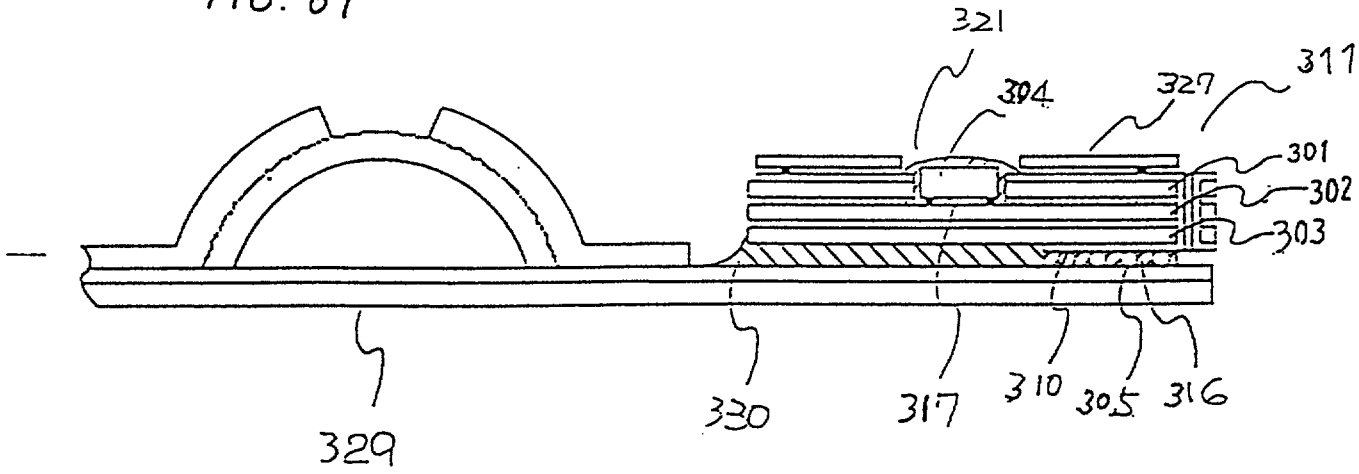

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FIG. 62

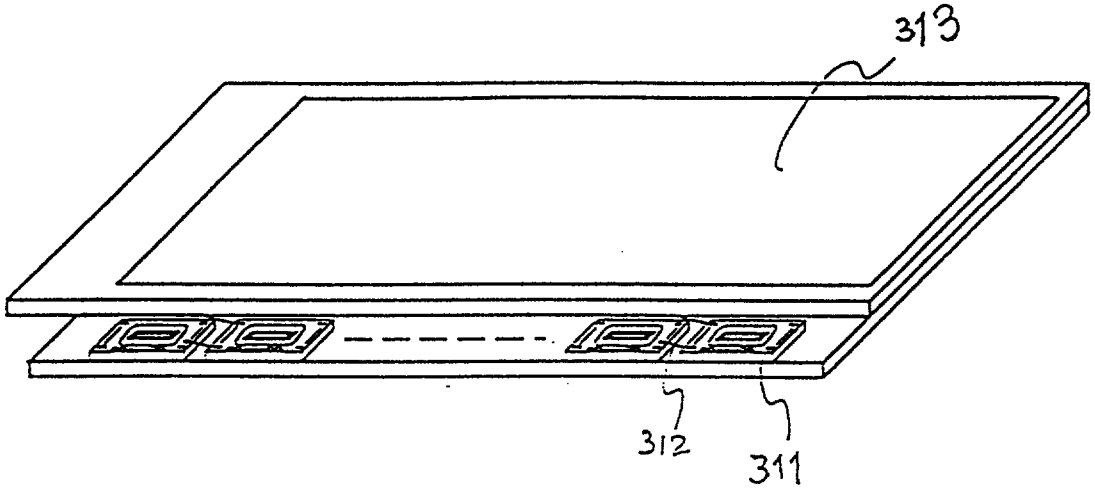


FIG. 63

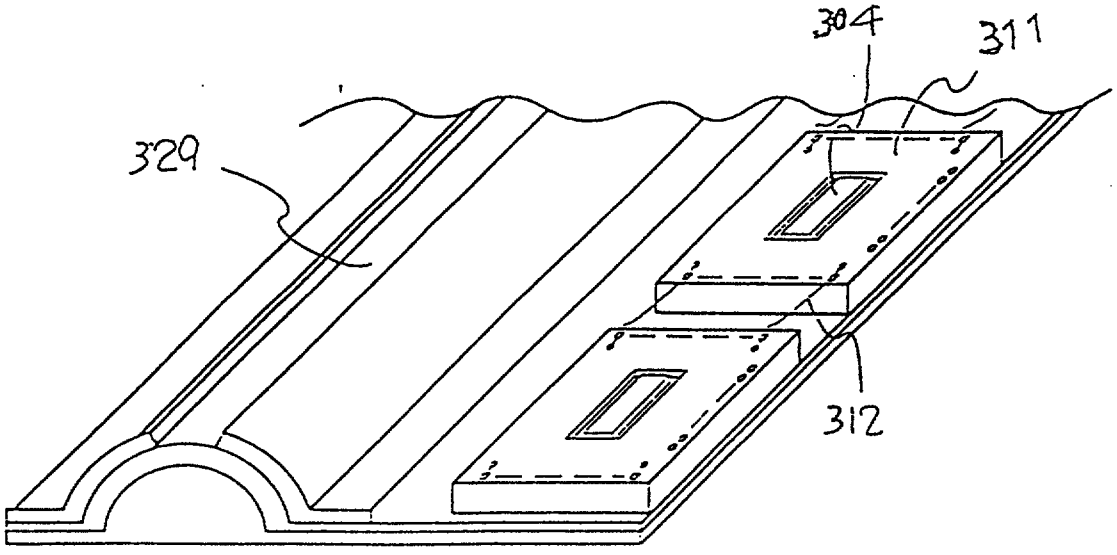


FIG. 64

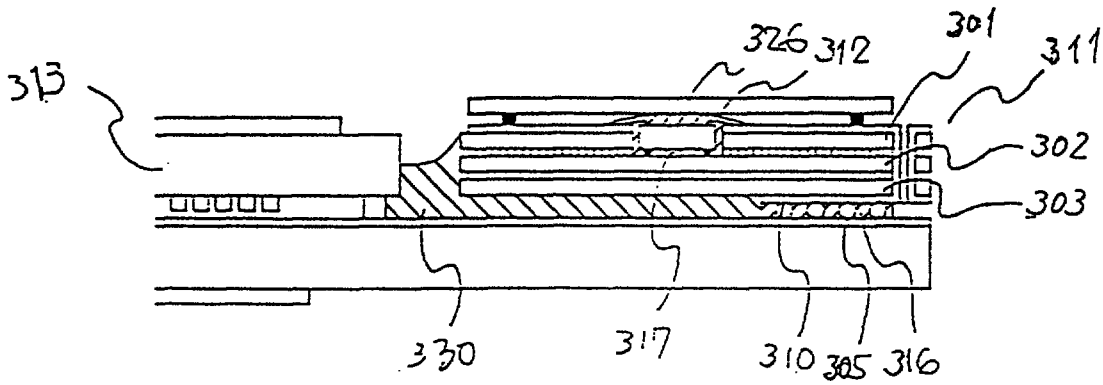

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FIG. 65

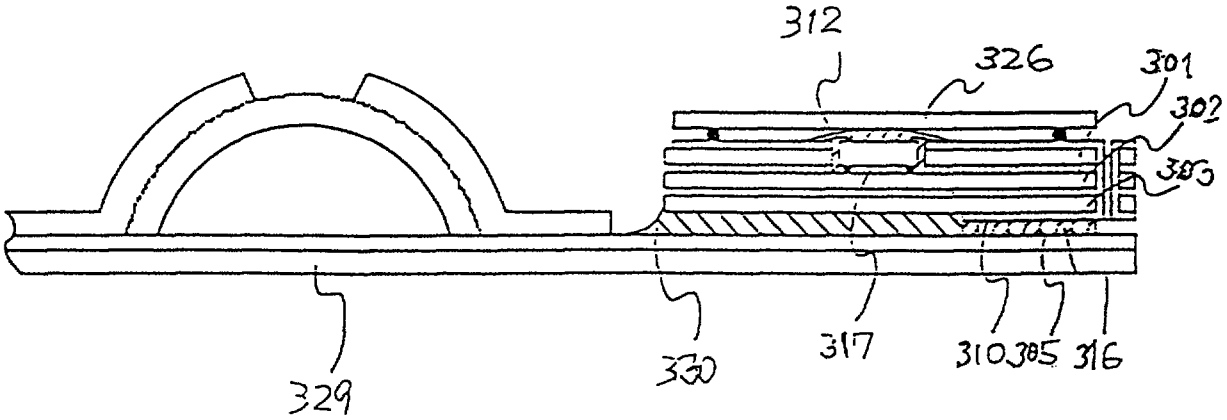

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FIG. 66

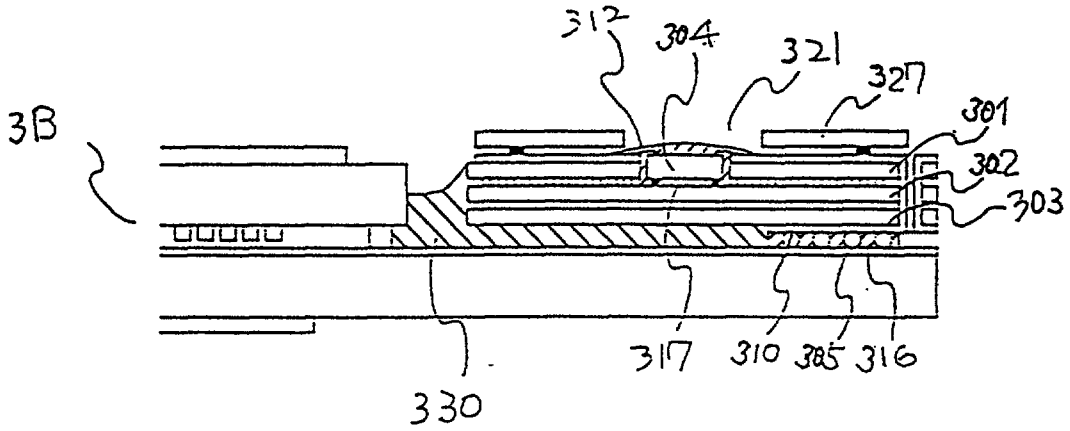

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FIG. 67

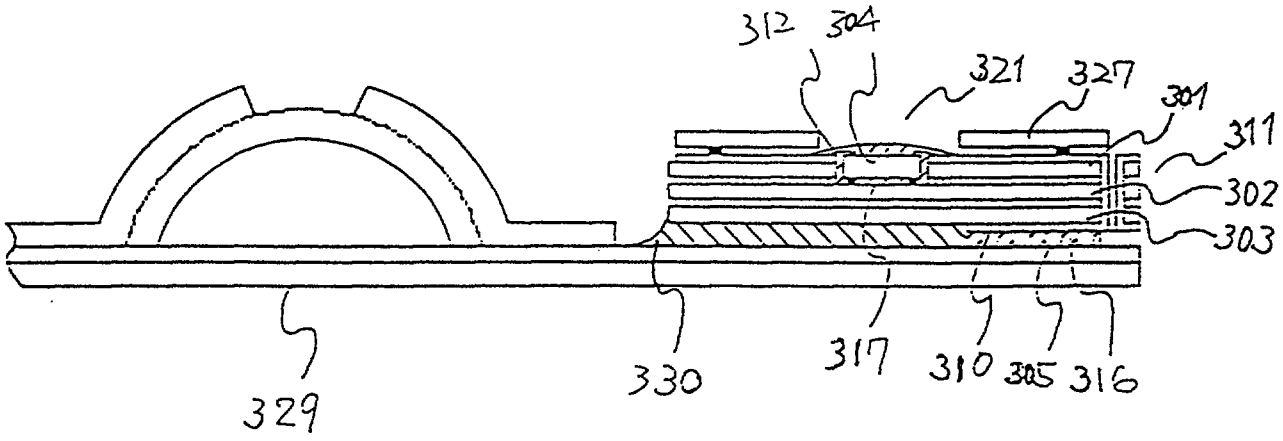

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316

FIG. 68

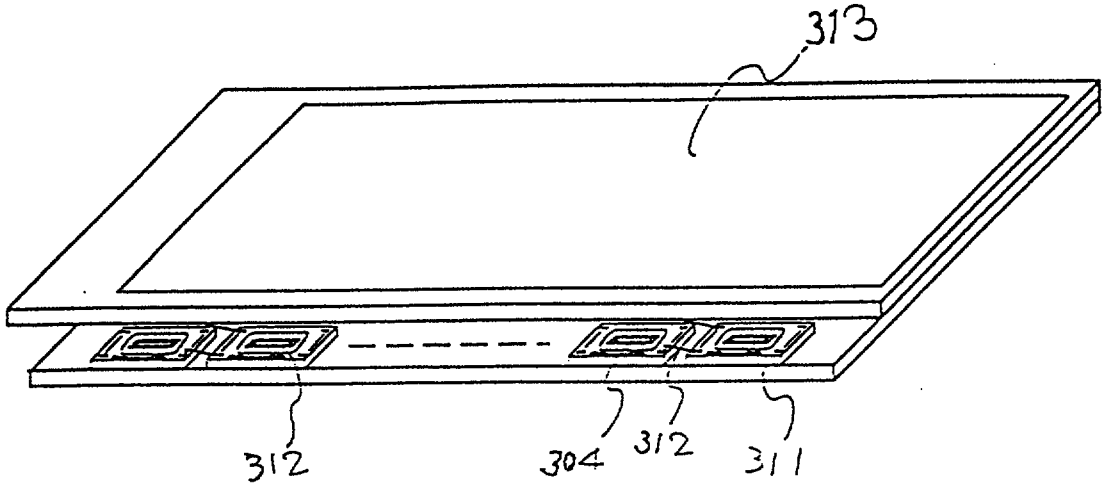


FIG. 69

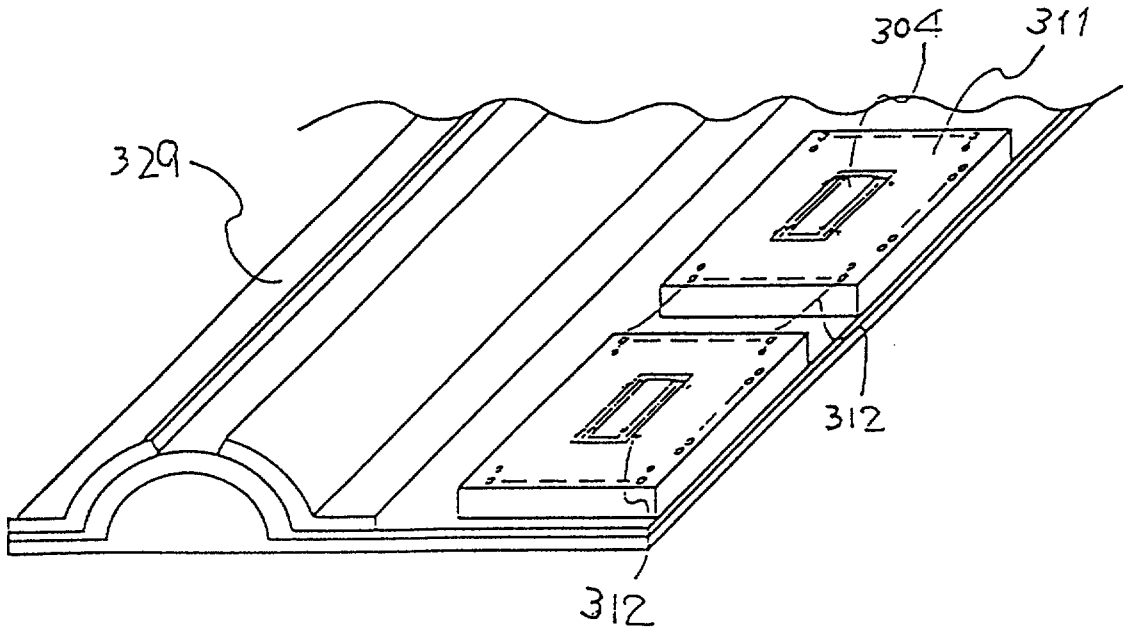


FIG. 70

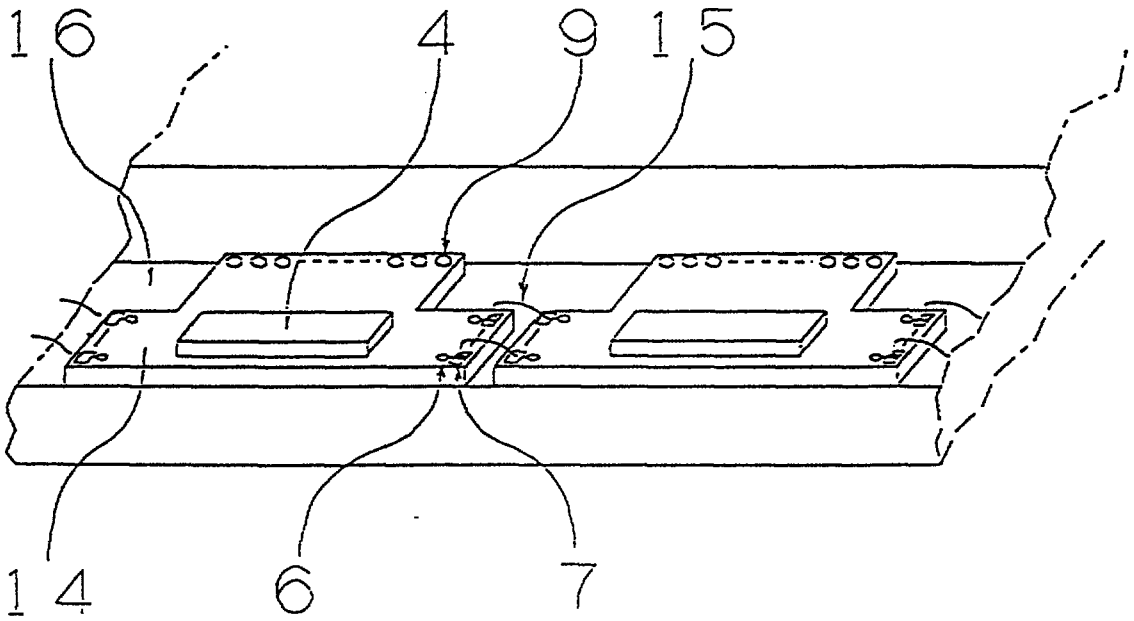


FIG. 79

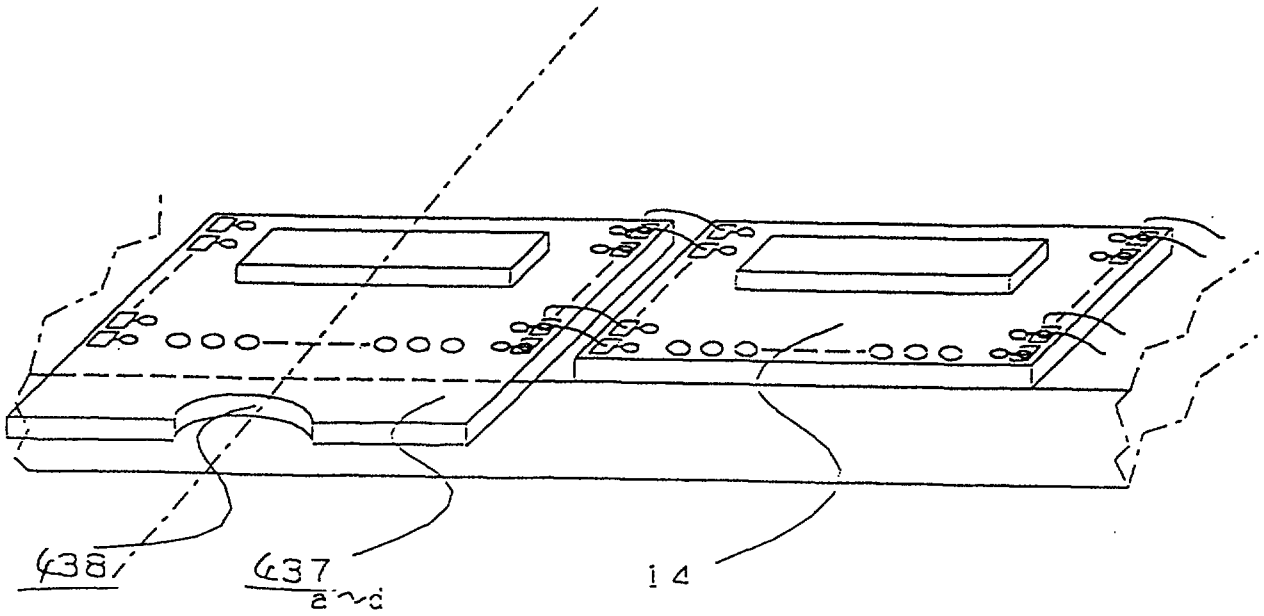


FIG.71

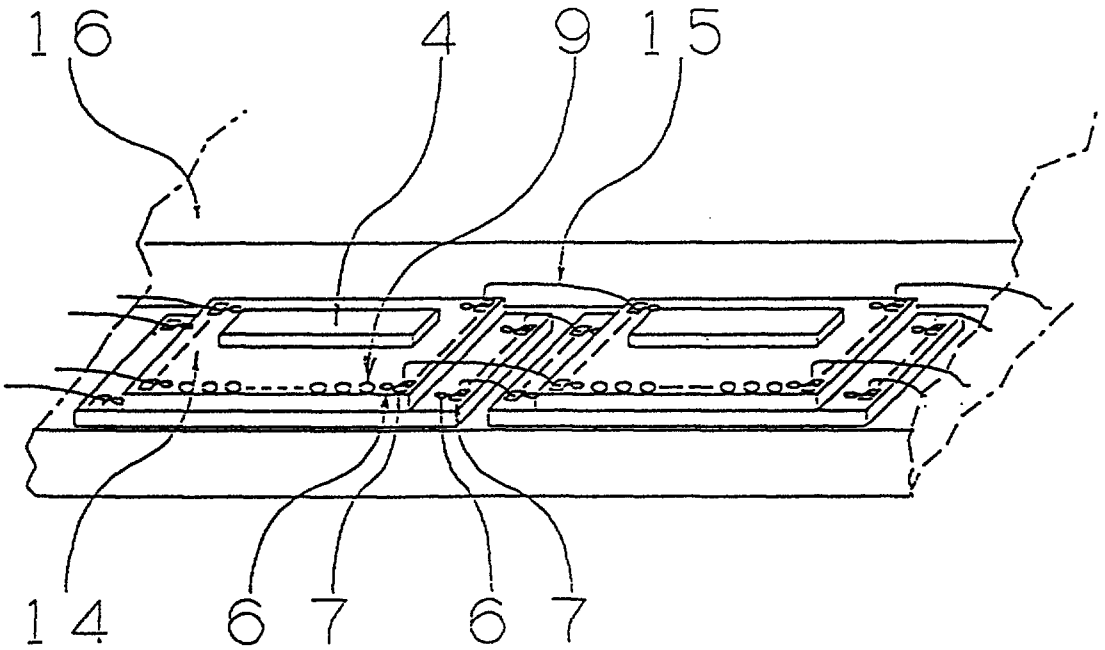


FIG.72

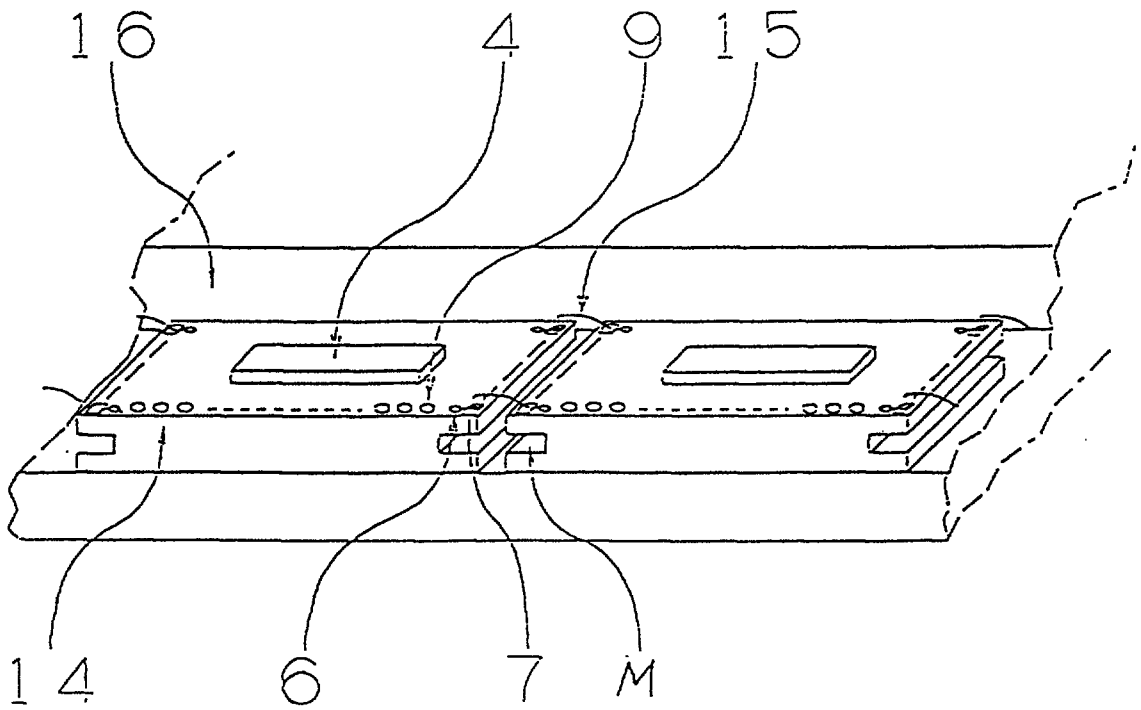


FIG. 73

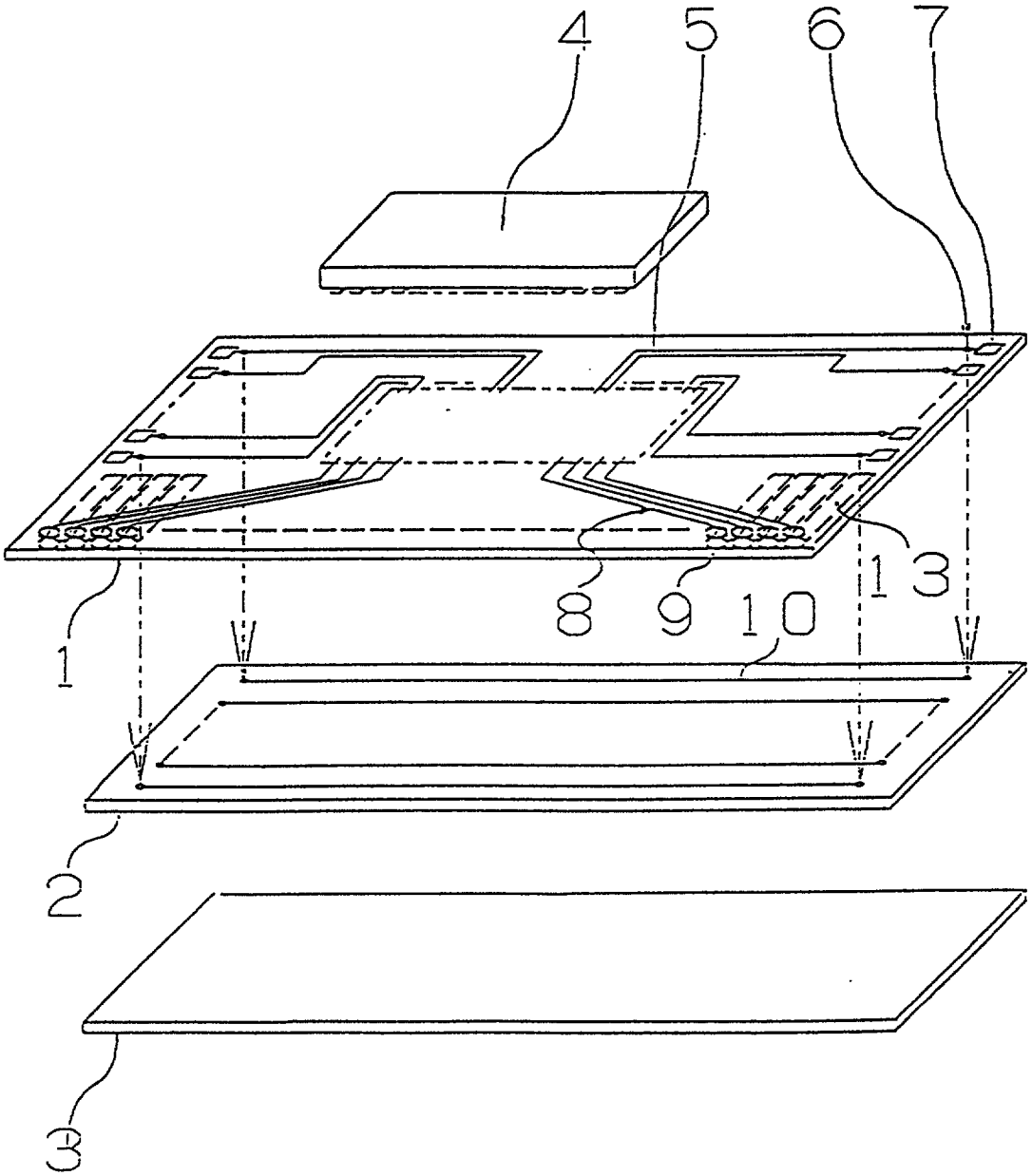


FIG. 74

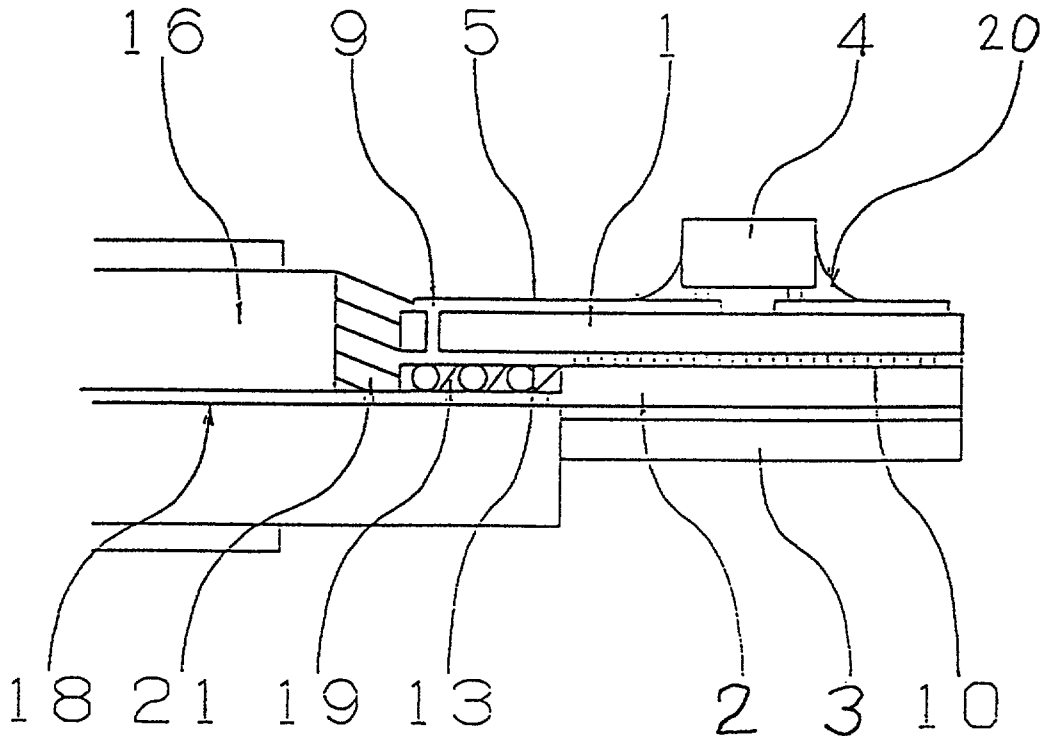


FIG. 75

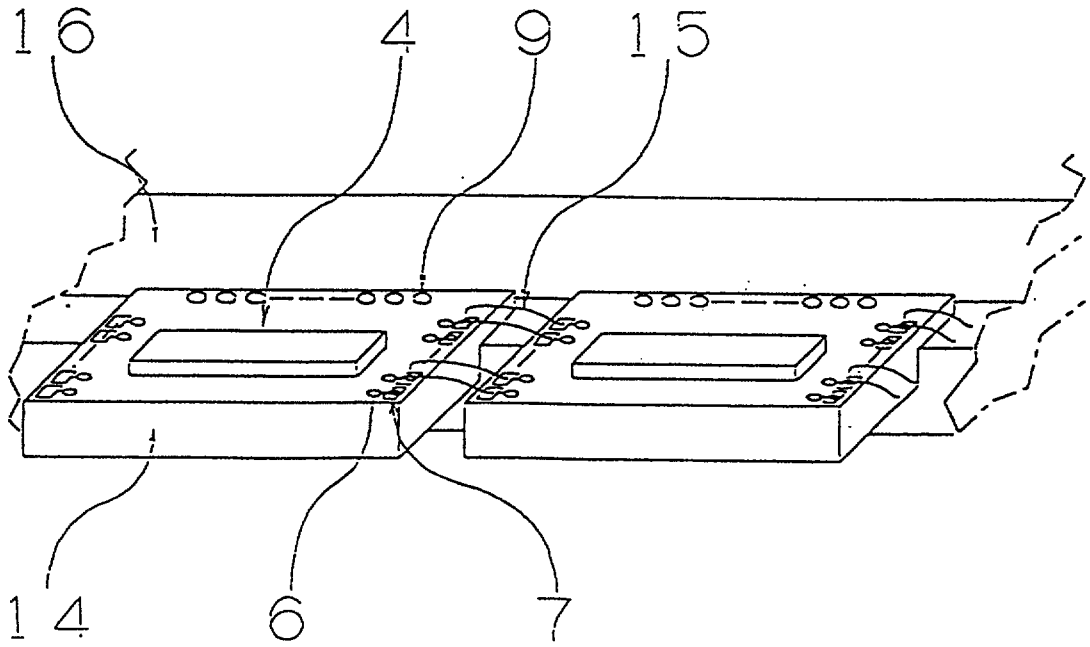


FIG. 76

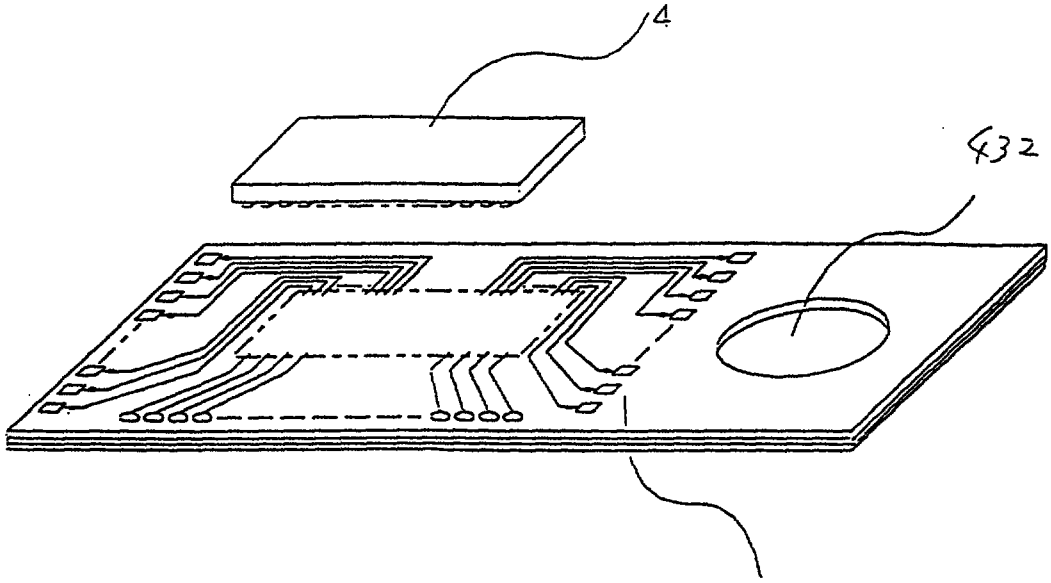


FIG. 77

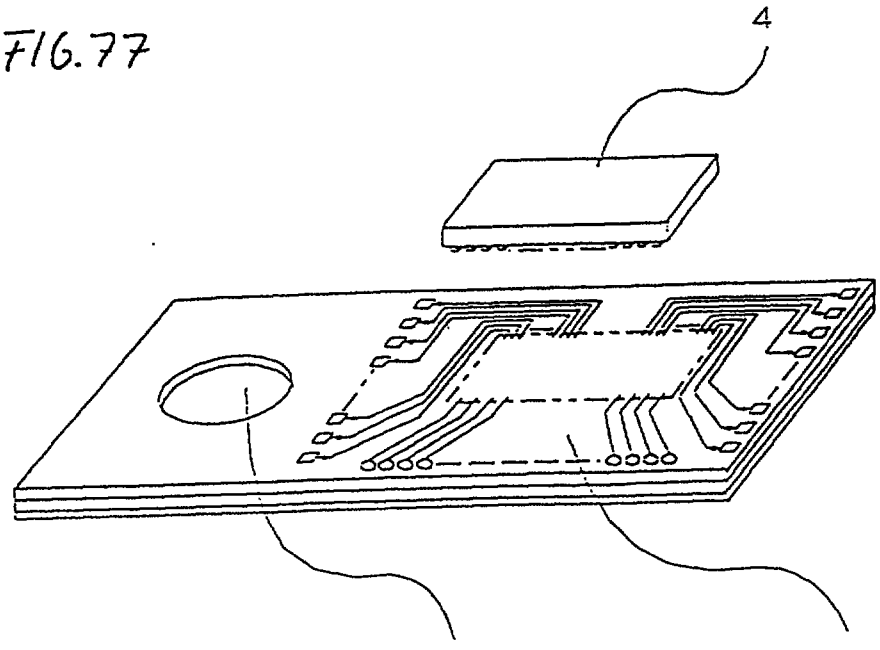


FIG. 78

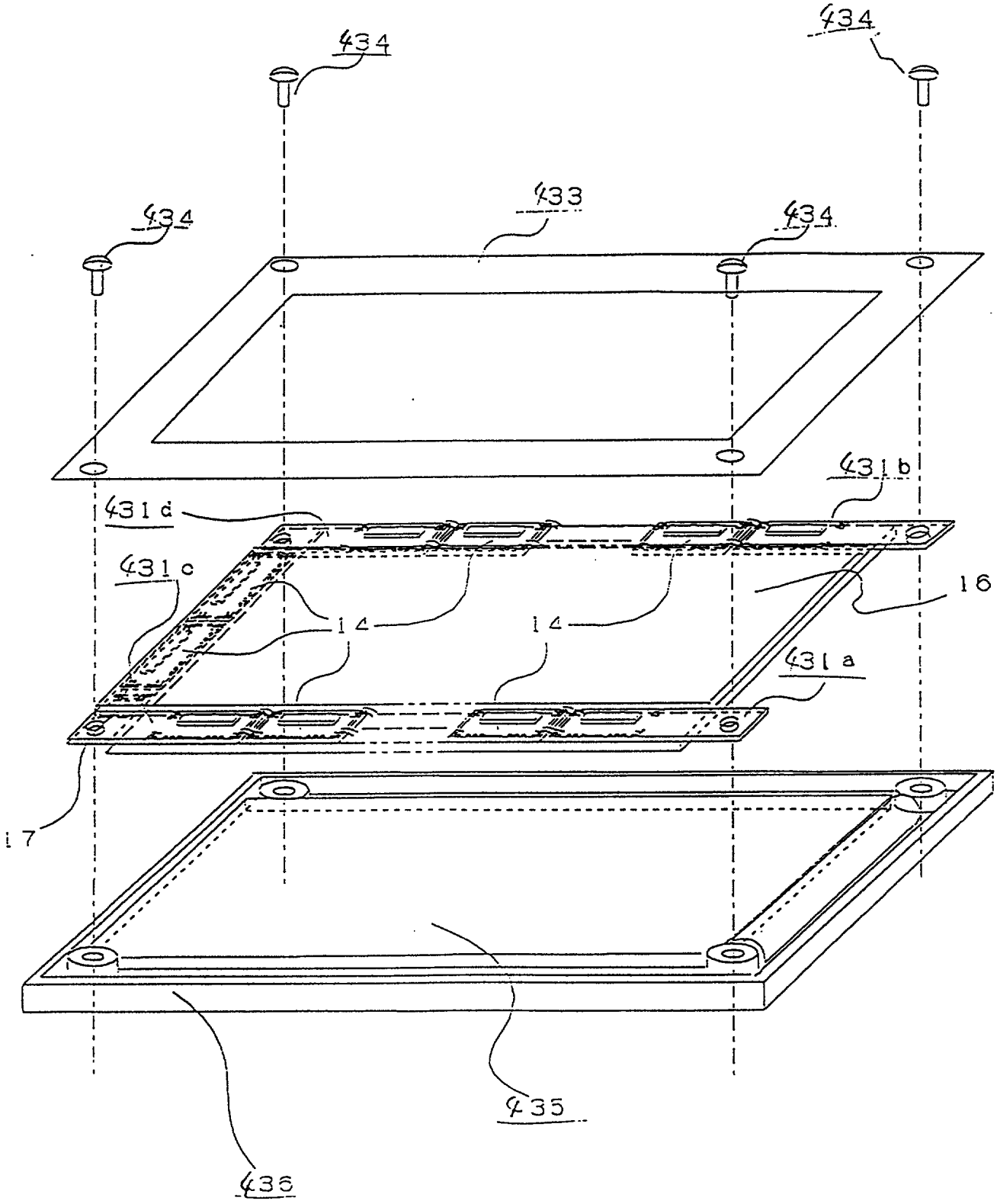


FIG. 80

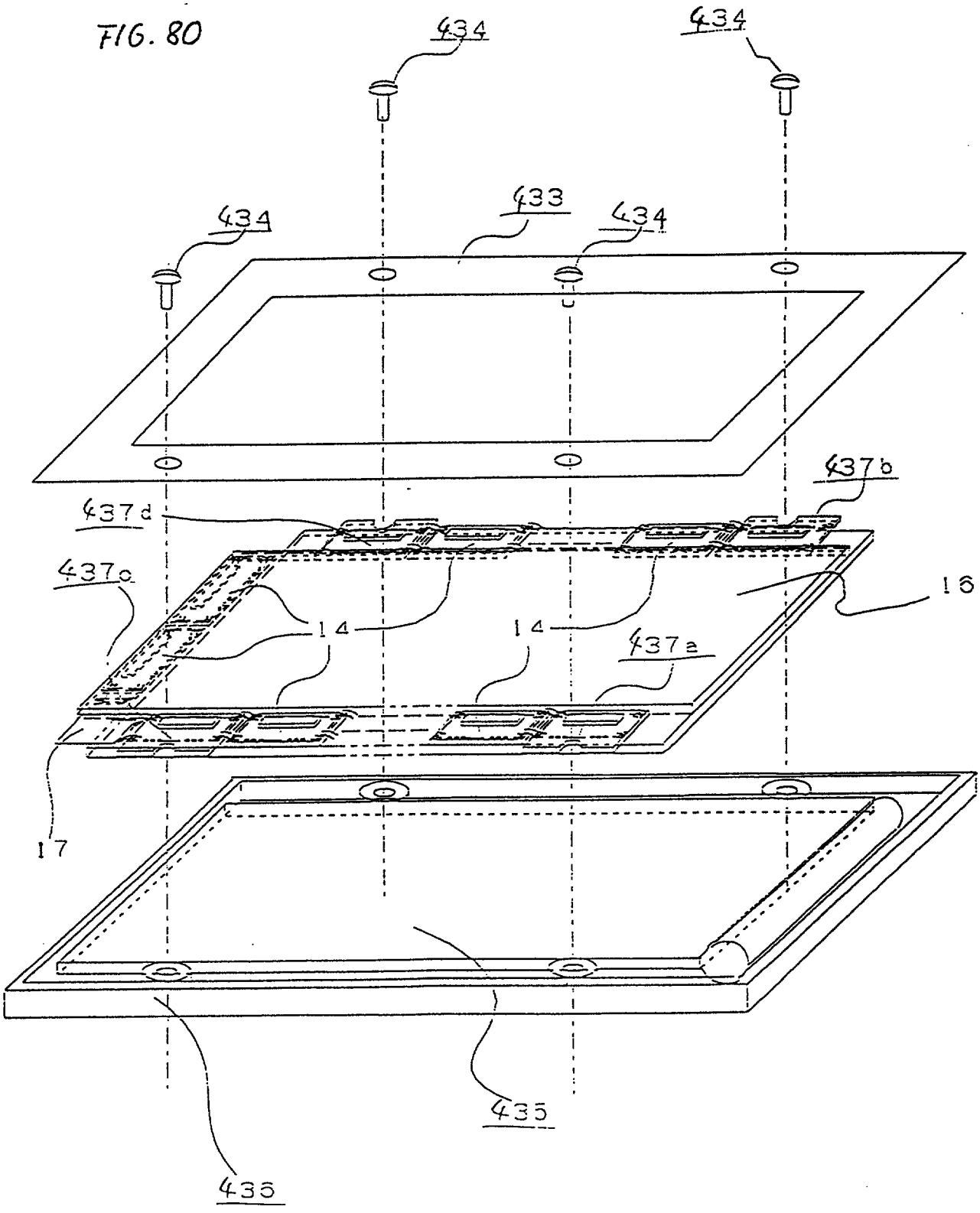


FIG. 81

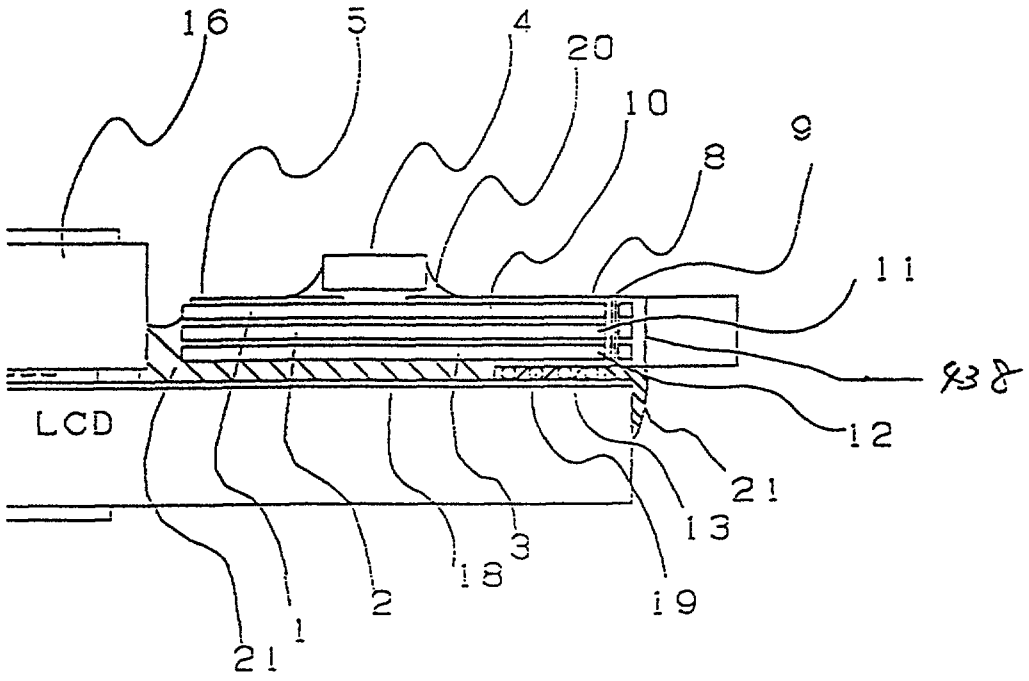


FIG. 82

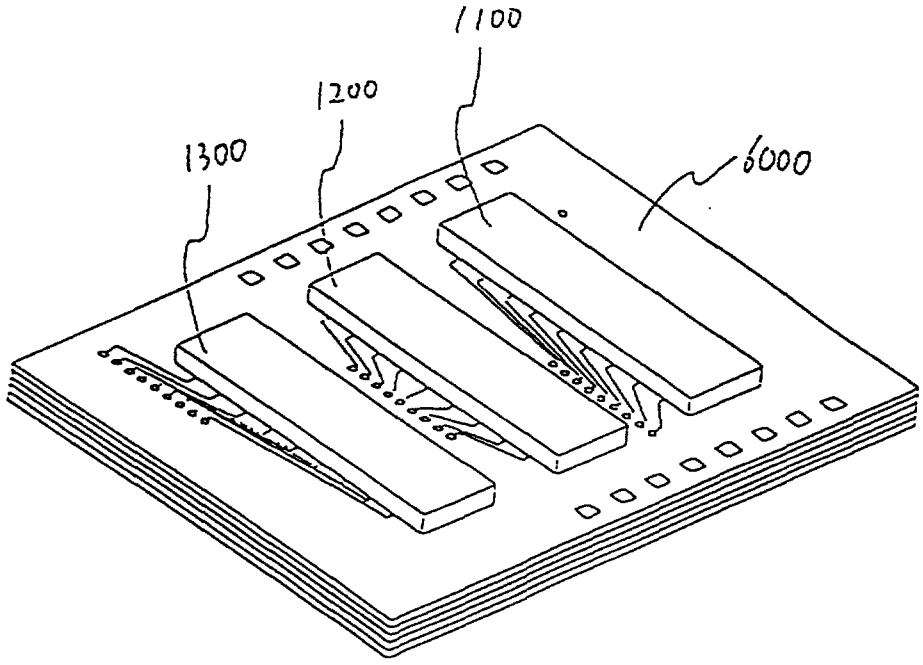


FIG. 83

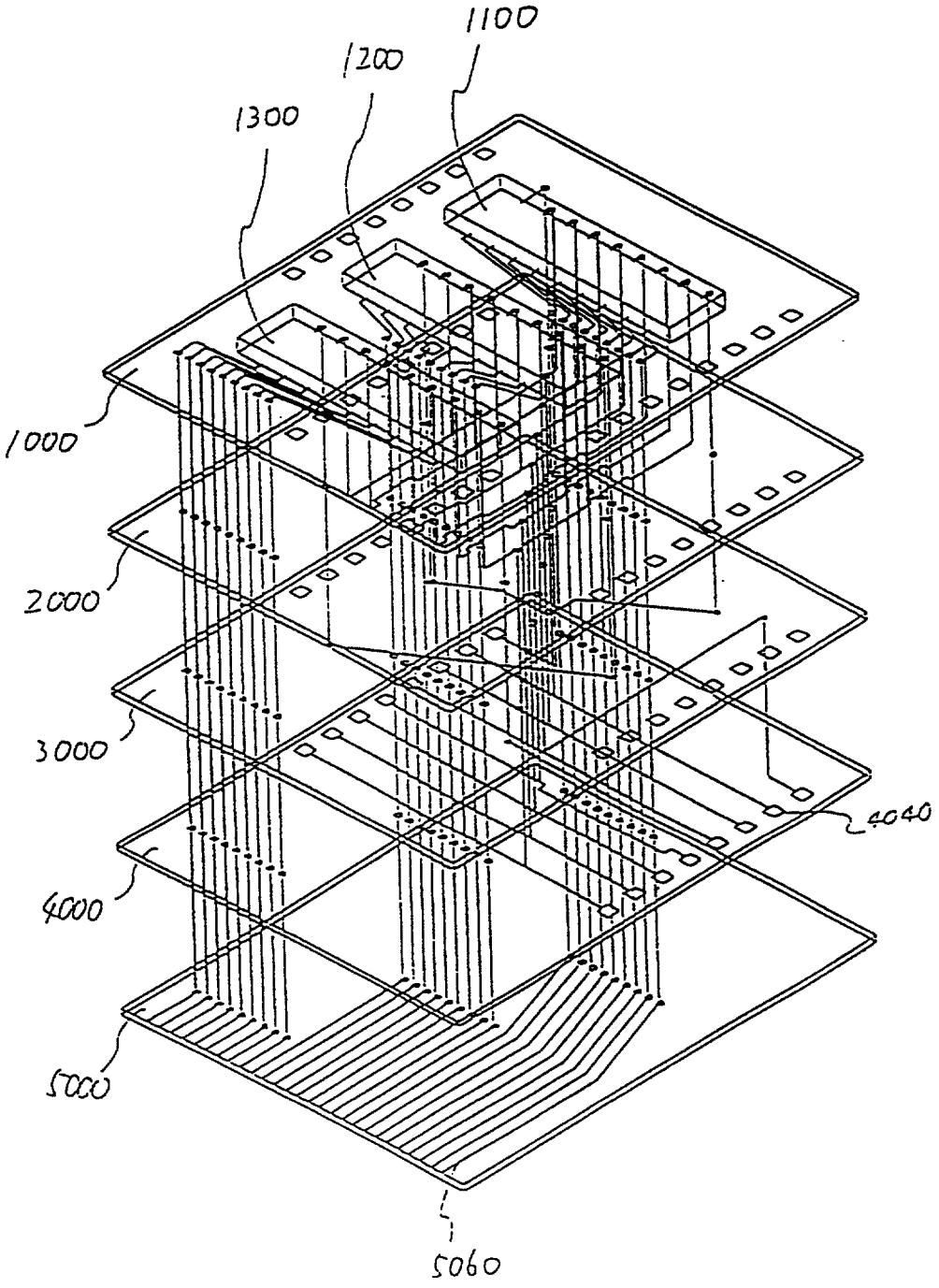


FIG. 8A

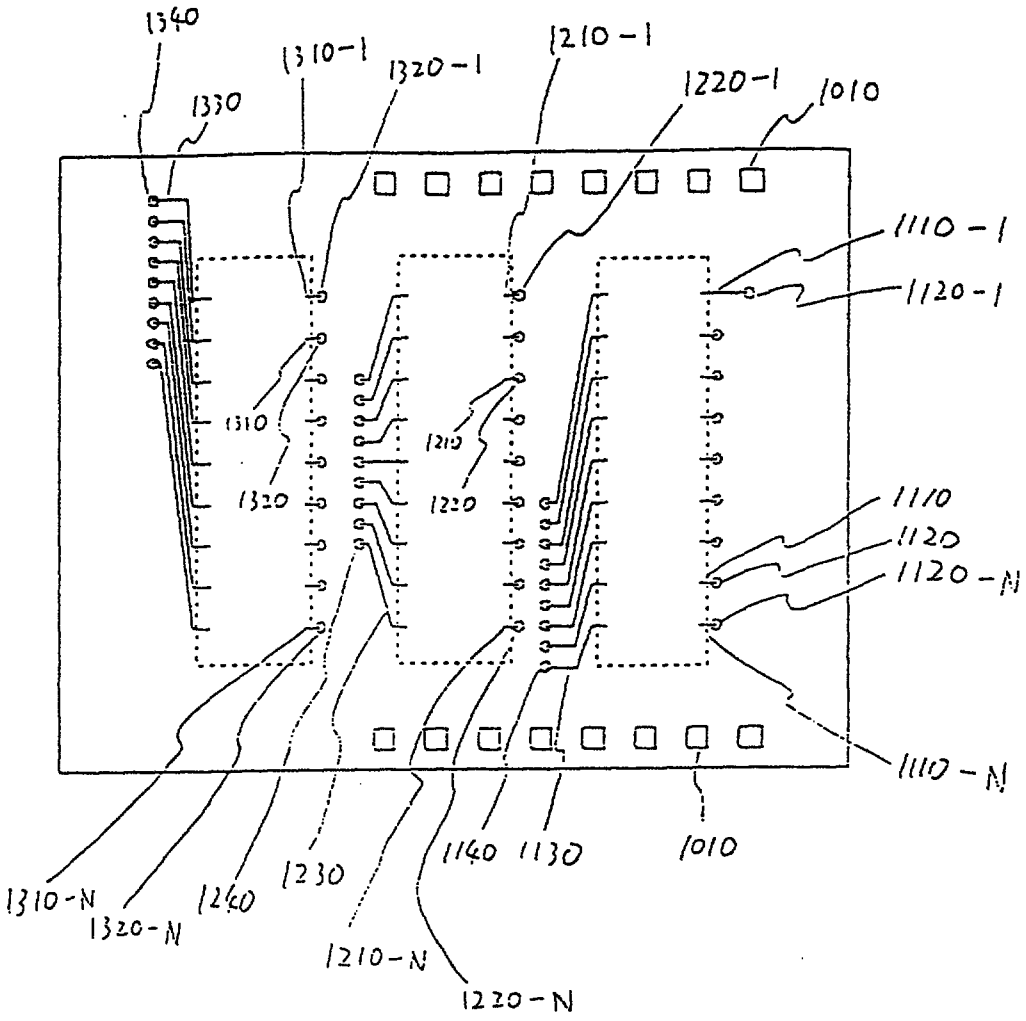

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1330
1310-1
1320-1
1210-1
1220-1
1010
1110-1
1120-1
1310
1320
1210
1220
1110
1120
1120-N
1110-N
1310-N
1320-N
1240
1230
1140
1130
1010
1210-N
1220-N

FIG. 85

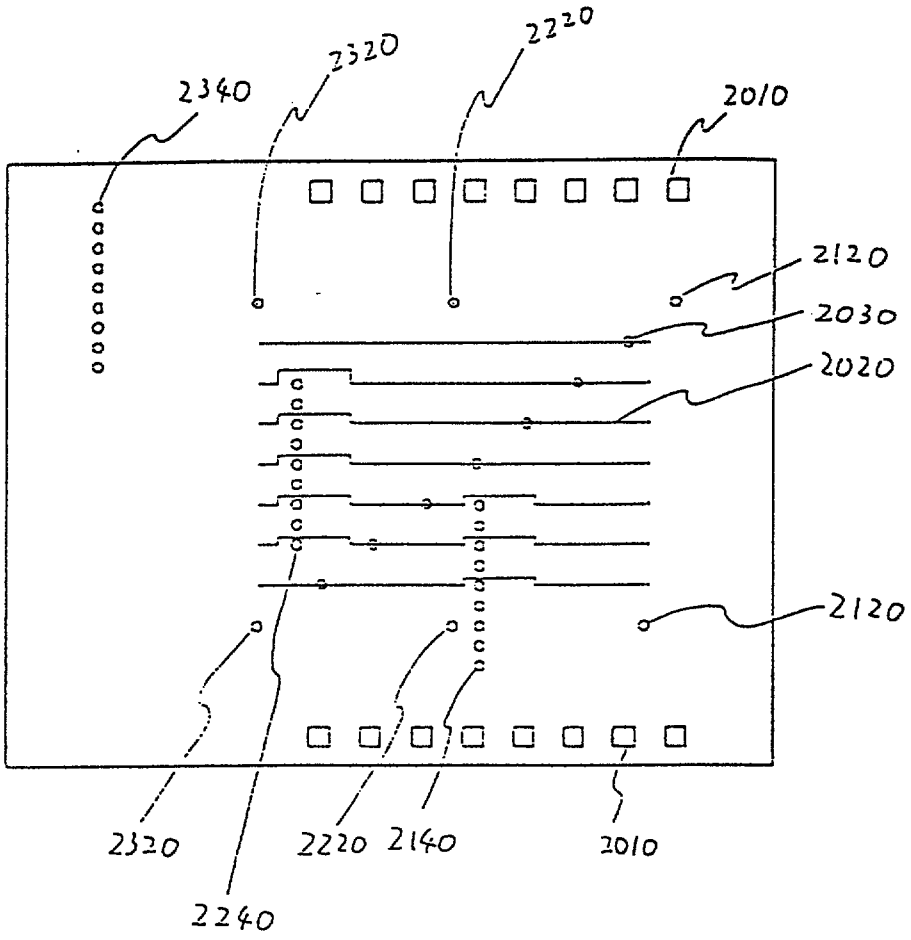

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2320
2220
2010
2120
2030
2020
2120
2320
2220
2140
2010
2240

FIG. 86

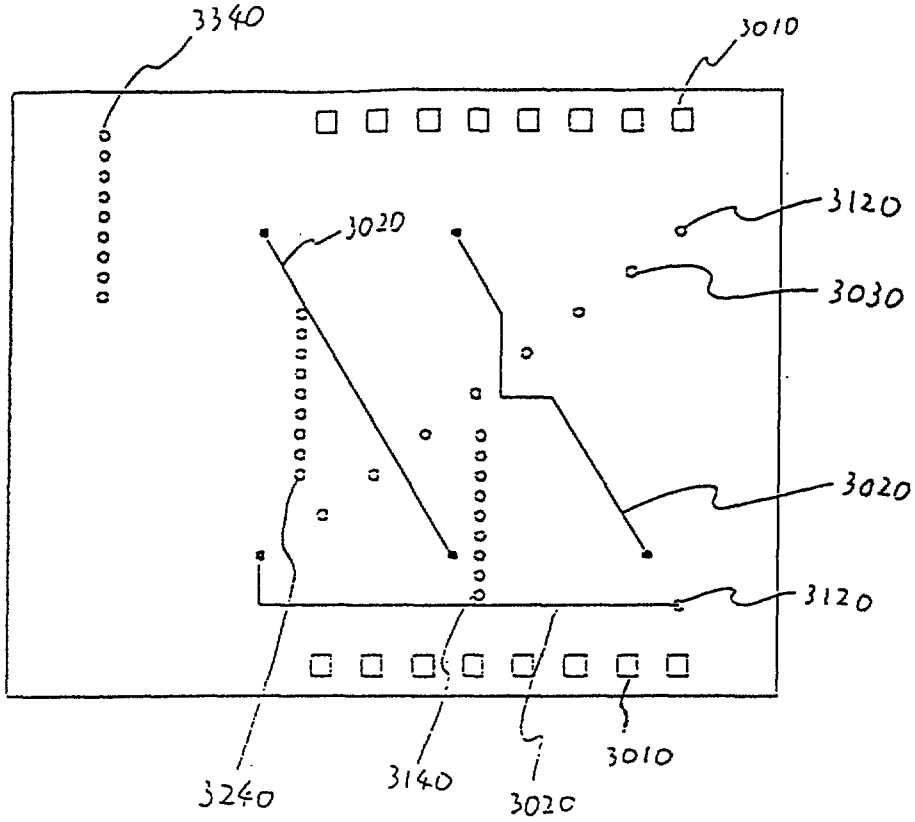

3340
3010
3120
3020
3030
3020
3120
3010
3240
3140
3020

FIG. 87

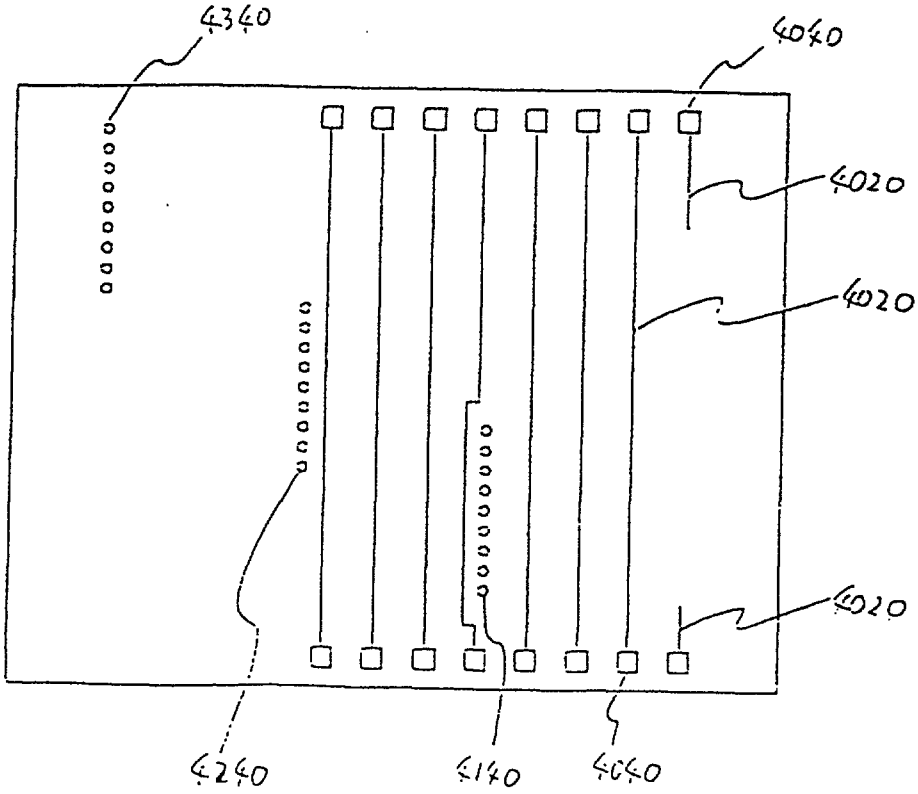

4340
4040
4020
4020
4020
4240
4140
4040

FIG. 88

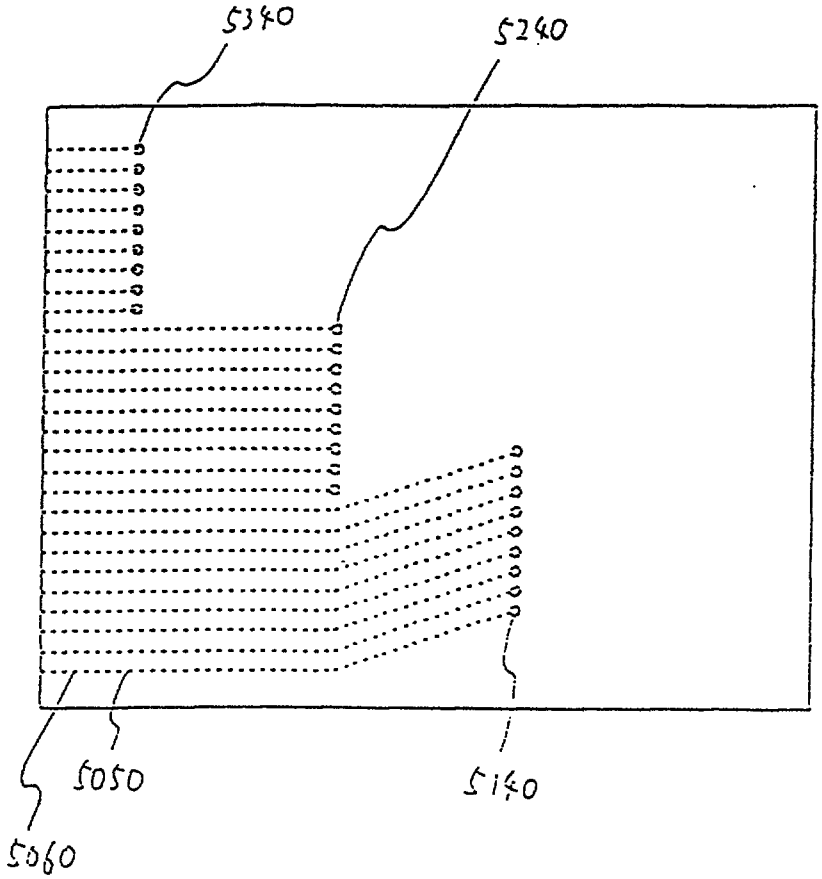


FIG. 89

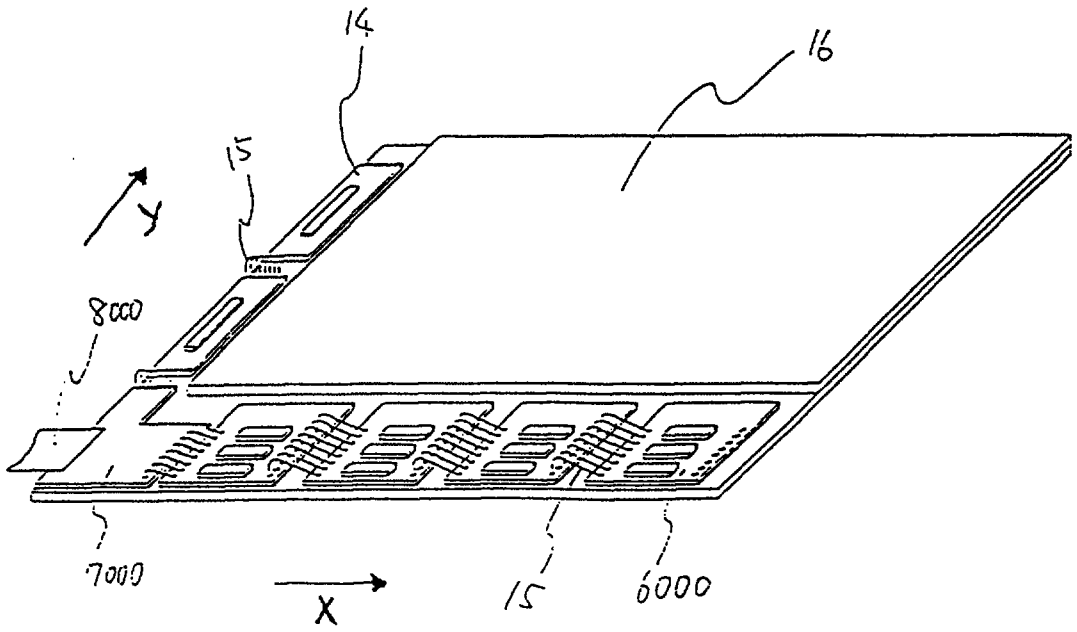


FIG. 90

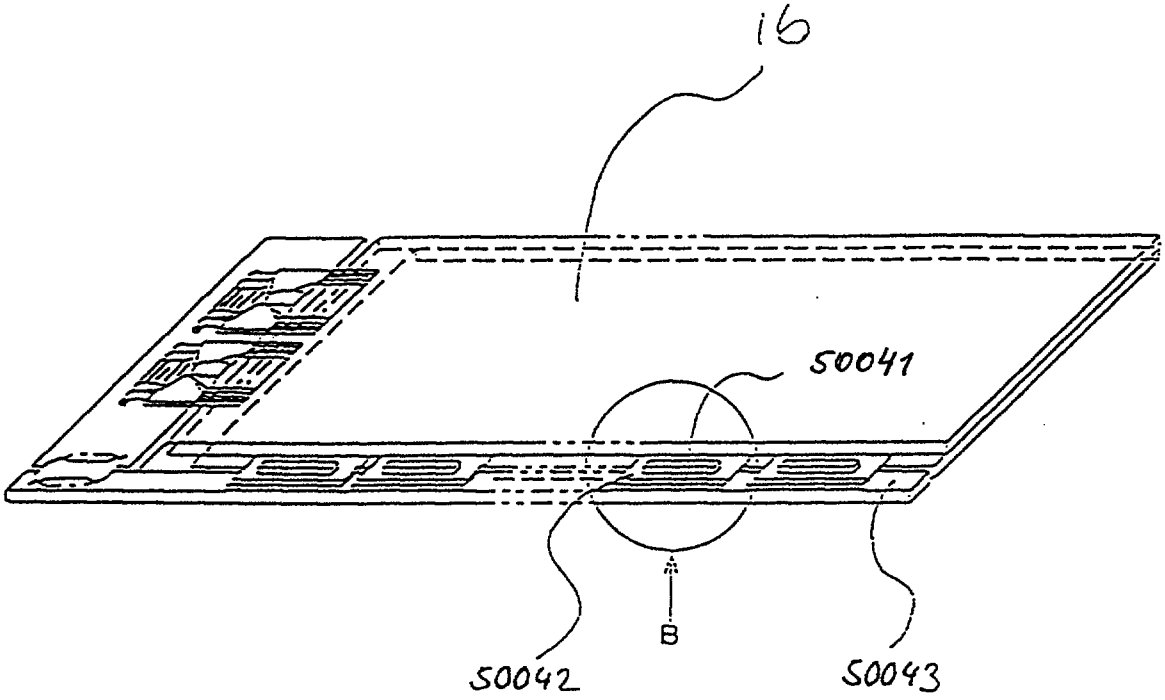

16
50041
B
50042
50043

FIG. 91

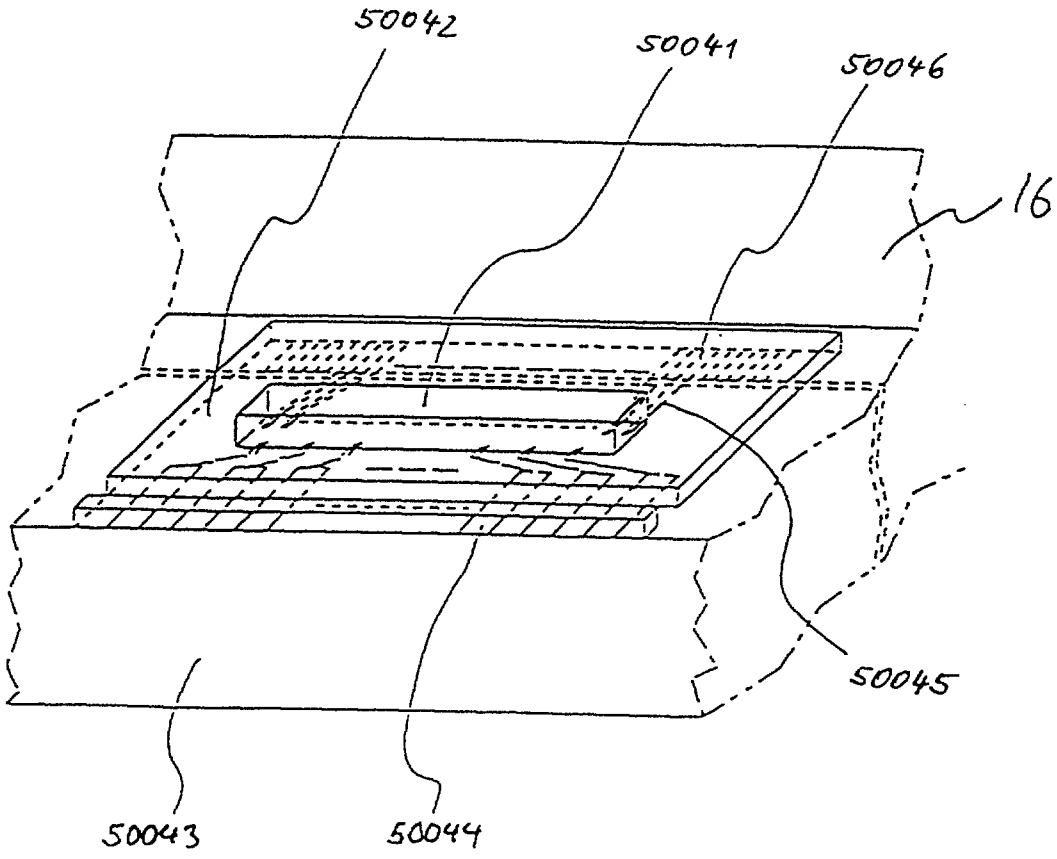

50042
50041
50046
16
50045
50043
50044

FIG. 92

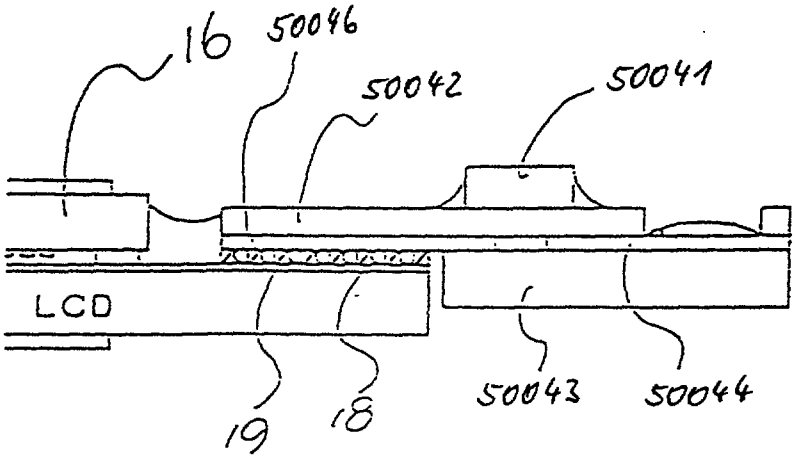

16
50046
50042
50041
LCD
19
18
50043
50044

FIG. 93

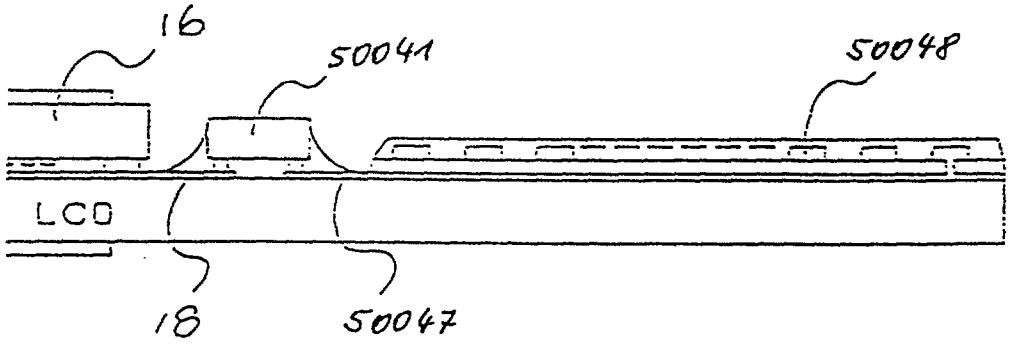

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50041
50048
LCD
18
50047

FIG. 94

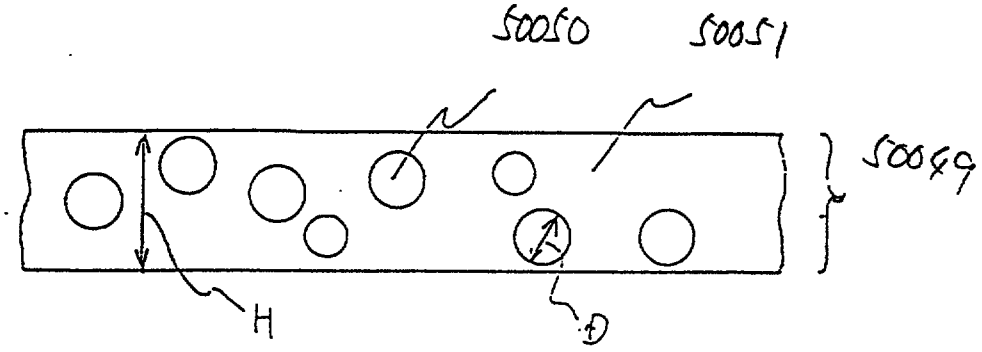


FIG. 95

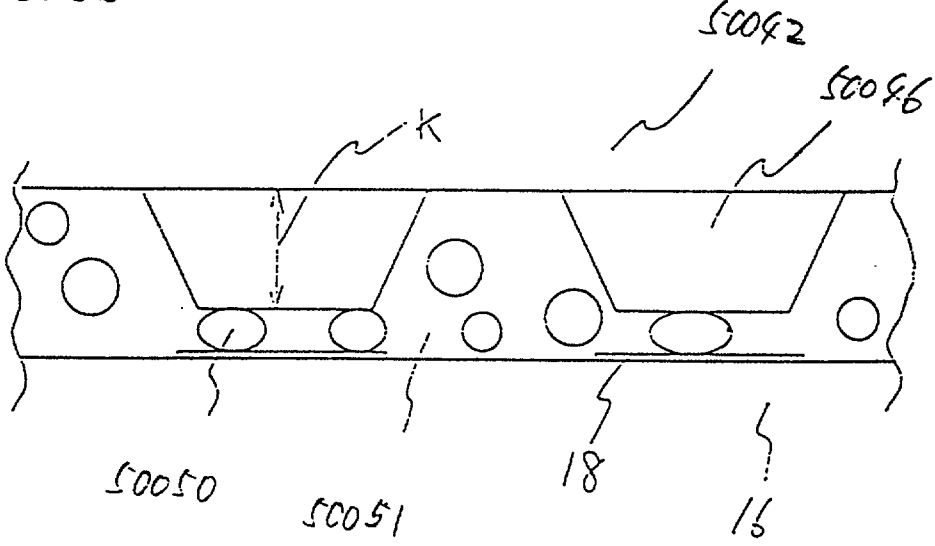


FIG. 96

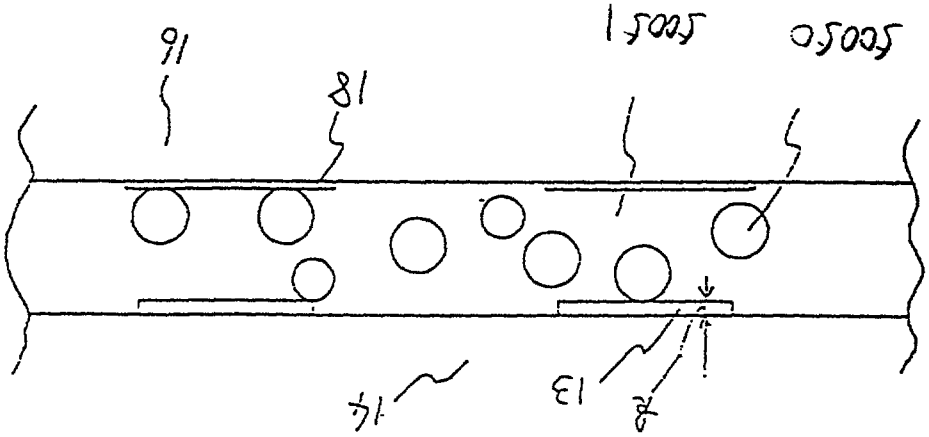

91
81
15005
05005
14
13
12

FIG. 97

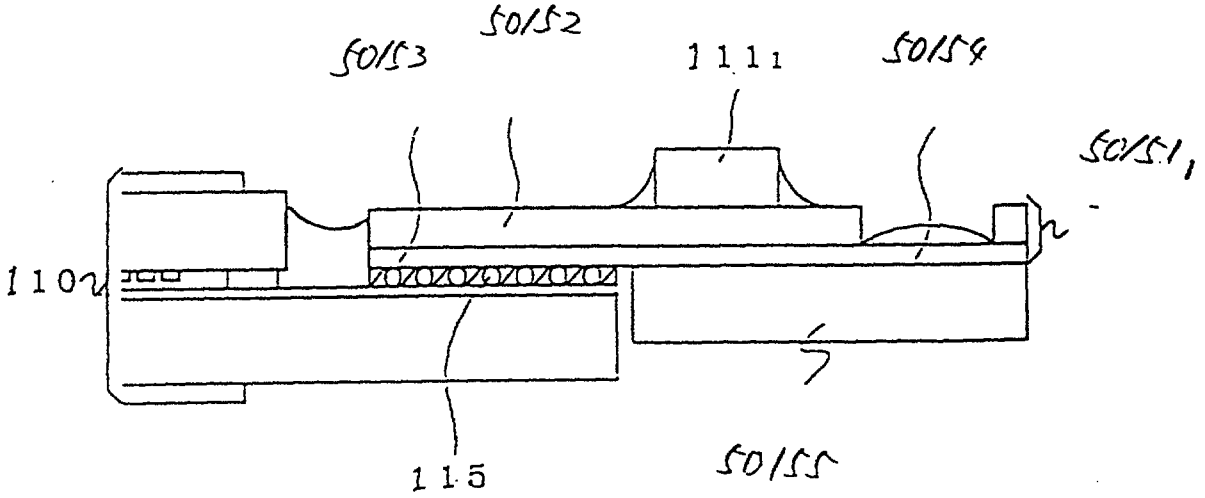

50153
50152
1111
50154
50151
110
115
50155

FIG. 98

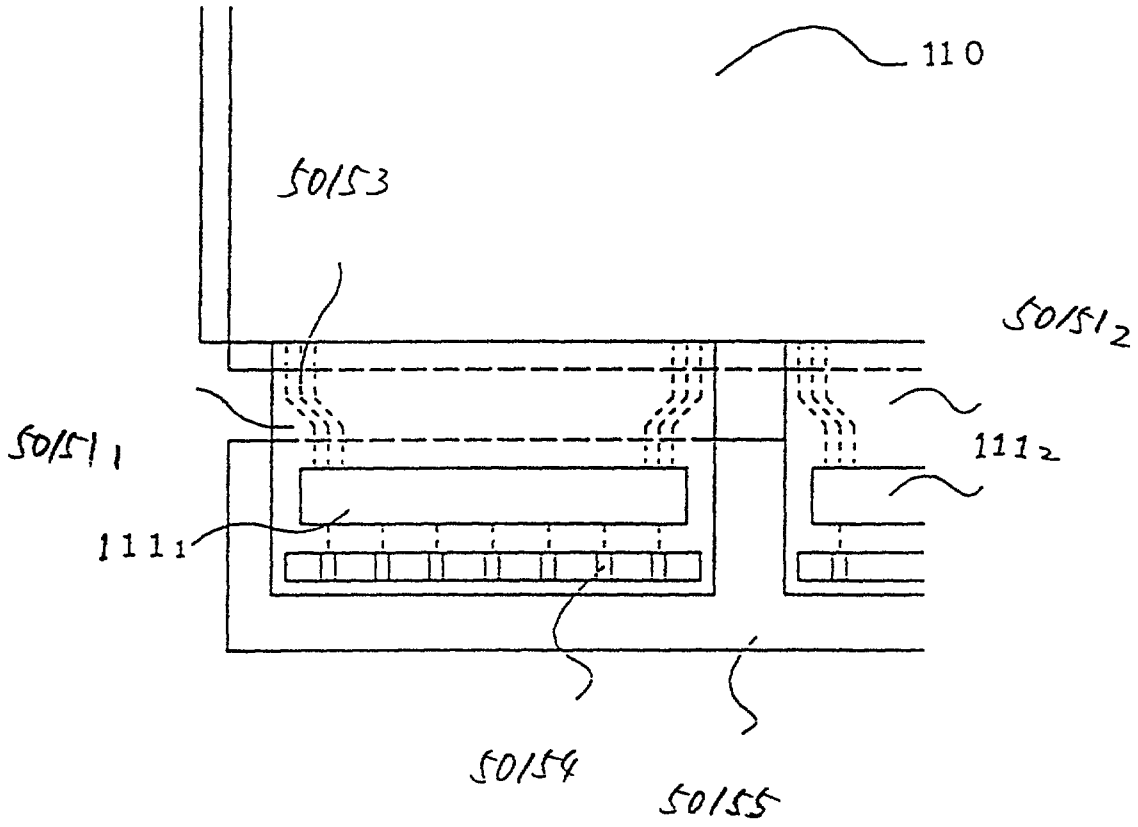
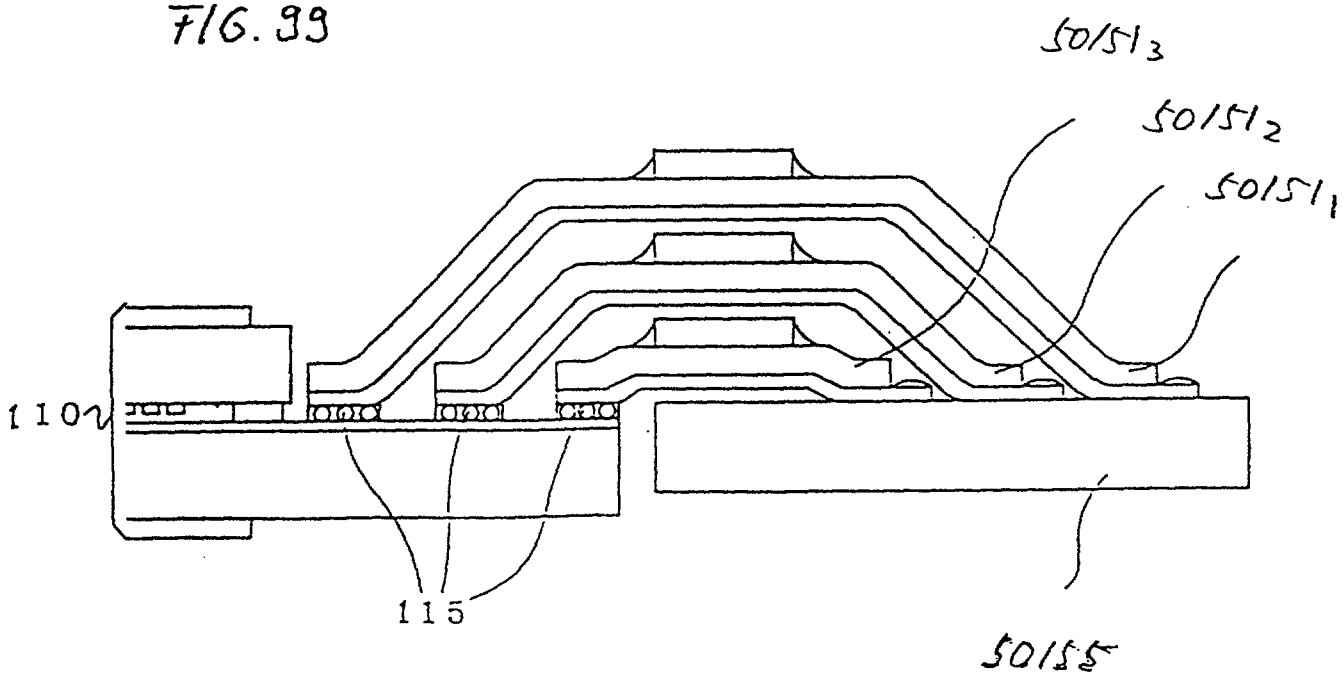

110
50153
50151_2
50151_1
111_2
111_1
50154
50155

FIG. 99


50151_3
50151_2
50151_1
110
115
50155