

**PROGRAMMABLE GAIN AMPLIFIER FOR USE IN DATA NETWORK****TECHNICAL FIELD**

5 The present invention generally relates to network interfacing and, more particularly, to a system for controlling transmission of data between the network stations connected to a network medium and a device and method for adjusting input gain.

BACKGROUND ART

10 There is an ever present demand for transmission of various types of data between computers. A predominate method of transmitting such data includes coding the data into a low frequency base data signal and modulating the base data signal onto a high frequency carrier signal. The high frequency carrier signal is then transmitted across a network cable medium, via RF signal, modulated illumination, or other network
15 medium, to a remote computing station.

At the remote computing station, the high frequency carrier signal must be received and demodulated to recover the original base data signal. In the absence of any distortion of the carrier signal across the network medium, the received carrier would be identical in phase, amplitude, and frequency to the transmitted carrier and could be
20 demodulated using known mixing techniques to recover the base data signal. The base data signal could then be recovered into digital data using known sampling algorithms.

However, the network topology tends to distort the high frequency carrier signal due to numerous branch connections and different lengths of such branches causing numerous reflections of the transmitted carrier. The high frequency carrier is further
25 distorted by spurious noise caused by electrical devices operating in close proximity to the cable medium. Such problems are even more apparent in a network which uses home telephone wiring cables as the network cable medium because the numerous branches and connections are typically designed for transmission of plain old telephone system (POTS) signals in the 0.3 to 3.4 Kiloherztz frequency and are not designed for
30 transmission of high frequency carrier signals on the order of 1 Megahertz or higher. The high frequency carrier signals are further distorted by turn-on transients due to on-hook and off-hook noise pulses of the POTS utilizing the network cables.



Such distortion of frequency, amplitude, and phase of the high frequency carrier signal degrades network performance and tends to impede the design of higher rate networks and challenges designers to continually improve modulation techniques and data recovery techniques to improve data rates. For example, under the home
5 phoneline networking alliance (HPNA) 1.0 standard, a 1 Mbit data rate is achieved using pulse position modulation (PPM) of a carrier, while the more recent HPNA 2.0 standard achieves a 10 Mbit data rate using a complex modulation scheme using a frequency diverse quadrature amplitude modulation (QAM). A problem exists in that a PPM modulated carrier signal and a QAM modulated carrier signal have
10 significantly different power envelopes.

Another problem associated with advancing standards and increasing data rates is that, as in the HPNA example, original base data signal amplitude variations and distortions can cause an incoming analog signal to have an amplitude greater than the dynamic range of an analog to digital converter which converts the incoming
15 analog signal into a digital representation of the incoming analog signal. The incoming analog signal can also have an amplitude which is less than the full dynamic range of the analog to digital converter, resulting in the failure to take advantage of the full dynamic range, or resolution, of the analog to digital converter.

Therefore, based on recognized industry goals for size and cost reductions,
20 what is needed is a device and method for adjusting input gain for an amplifier in a receiver capable of receiving distorted, modulated carrier signals potentially using multiple modulation techniques.

US-A-5,146,155 discloses a measurement circuit that provides a digital value of an analogue signal, the circuit including an amplifier that receives the analogue
25 signal, and an analogue to digital converter that receives the amplified signal. The gain of the amplifier is controlled in discrete steps by a control signal fed back from a control unit that receives the digital output of the analogue to digital converter.

According to one aspect of the present invention there is provided a data networking device, comprising: a variable gain amplifier; an analog to digital
30 converter for converting an analog output signal of the amplifier to a digital signal; and a digital signal monitoring circuit for monitoring the digital signal and supplying

feedback signals to control the gain of the amplifier as a function of the digital signal, characterised in that the amplifier has a first selectable impedance and a second selectable impedance, the impedances being actuated by the feedback signals to adjust the gain of the amplifier, and the digital monitoring circuit monitoring the digital signal to determine the percentage of dynamic range of the analog to digital converter being used to convert the analog output signal of the amplifier.

According to a further aspect of the invention there is provided a method of controlling a variable gain amplifier wherein, an analog output signal of the variable gain amplifier is converted to a digital signal by an analog to digital converter, characterised in that the method comprises: determining a portion of the dynamic range of the analog to digital converter being used to convert the analog output signal of the variable gain amplifier; and providing a first feedback signal to a first selectable impedance and providing a second feedback signal to a second selectable impedance, the first and second feedback signals adjusting the gain of the amplifier to increase the dynamic range used by the analog to digital converter.

In a preferred embodiment of the invention the digital monitoring circuit determines if the digital output signal is consistently near the upper or lower end of the dynamic range of the A/D converter and the feedback signal is correspondingly adjusted to decrease or increase the amplifier gain so that the full dynamic range of the A/D converter is utilised.

These and further preferred features of the present invention will be apparent from the following description with reference to the accompanying drawings wherein, by way of example only:

FIG. 1 is a block diagram of an analog front end circuit having a variable gain amplifier and embodying to the present invention;

FIG. 2 is a representative circuit diagram of the variable gain amplifier shown in Fig.1;

FIG. 3 is a schematic diagram of a first selectable impedance for use with the variable gain amplifier of Fig.2;

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FIG. 4 is a schematic diagram of a second selectable impedance for use with the variable gain amplifier of Fig.2; and

FIG. 5 is a schematic diagram of a selectable capacitive compensation circuit for use with the variable gain amplifier of Fig.2.

5 In the detailed description which follows, identical components have been given the same reference numerals, regardless of whether they are shown in different embodiments of the present invention. In order to clearly and concisely illustrate the

present invention, the drawings may not necessarily be to scale and certain features may be shown in somewhat schematic form.

The present invention relates to a variable gain amplifier which conditions an incoming analog voltage signal to take advantage of the full dynamic range (i.e., resolution) of an analog to digital (A/D) converter in a data networking device.

FIG. 1 illustrates an analog front end circuit 10 of a networking device, such as a 1Mbps, 10Mbps, 100 Mbps or other bandwidth home phoneline networking alliance (HPNA), or other standard, data network operating over a conventional POTS RJ11 telephone line 12. The analog front end circuit 10 receives data signals from the telephone line 12 via a circuit 14 having components to condition the data signals, such as filters, transformers, and surge protection. The received signals, or incoming analog voltage signals 16, are processed by an electronic hybrid circuit 18 to perform functions such as collision detection. Next, the incoming signals 16 are passed through a variable gain amplifier (VGA) 20 and a filter 22 to condition the incoming signals 16. The conditioned, incoming signals are input into another VGA 24 which amplifies the conditioned, received signals for an analog to digital (A/D) converter 26. The input signal to the VGA 24 will be referred herein as V_i and the output of the VGA 24 will be referred to herein as V_o . The operation of the VGA 24 will be described in greater detail below. The A/D converter 26 converts the output of the VGA 24, or V_o , into a digital output, D_{OUT} . D_{OUT} is then sent from the A/D converter 26 to a digital input/output (I/O) circuit 28. The digital I/O circuit 28 acts as an interface between the analog front end circuit 10 and a subsequent network device circuit.

Digital data output signals received from the subsequent network device circuit by the analog front end circuit 10 are received by the digital I/O circuit 28. The digital data output signals are converted into a transmit analog signal by a digital to analog (D/A) converter 30. The transmit analog signal is conditioned by another VGA 32. The VGA 32 acts as an adjustable gain transmit attenuator to allow for flexibility in setting the transmit power of the analog front end circuit 10. The attenuated signal is further conditioned by a filter 34. The filtered, attenuated transmit signal is optionally passed through a transmit switch 36 before being sent to the telephone line 12 through the electronic hybrid circuit 18 and the circuit 14.

One function of the I/O circuit 28 is to provide feedback signals to the VGA 20, the VGA 24 and the VGA 32. The feedback signals are used by VGAs 20, 24 and 32 to vary the gain of those amplifiers.

With additional reference to FIG. 2, a schematic of the VGA 24 is illustrated.

5 The VGA 24 is a programmable amplifier implemented in standards CMOS. The gain of the VGA 24 is adjusted by varying an input attenuator, or first selectable impedance 44, and a second selectable impedance 46 connected to a feedback impedance 48. As illustrated in FIG. 2, the first selectable impedance 44 and the second selectable impedance 46 are continuous potentiometers having total resistance values of R_1 and R_2 respectively. The potentiometers are one illustrative embodiment of the invention and one skilled in the art will appreciate that the selectable impedances 44, 46 can be implemented with discrete uniform or non-uniform tapped resistor ladders actuated with CMOS structures as illustrated in FIGS. 3 and 4 and as discussed in more detail below. Alternatively, the impedances 44, 46 can be implemented with other resistive or
10 switching components giving equivalent results and are considered within the scope of the invention. The feedback impedance 48 has a fixed value, or R_F .

The first selectable impedance 44 and the second selectable impedance 46 are controlled by feedback from the digital I/O circuit 28. More specifically, the digital I/O circuit 28 has a digital monitoring circuit 50 providing feedback to the VGA 24. The
20 digital monitoring circuit 50 monitors the digital output of the A/D converter 26, or D_{OUT} . The digital monitoring circuit 50 collects information and statistics regarding the value of D_{OUT} which are used to adjust the feedback provided to the VGA 24. The statistics and information include signal output levels of the A/D converter 26. If the output of the A/D converter 26 is consistently at or near the upper end of the dynamic range of the
25 A/D converter 26, V_o may be saturating the A/D converter 26 and digital monitoring circuit 50 will provide feedback to the VGA 24 to attenuate V_i or reduce the current gain setting of the VGA 24. On the other hand, if D_{OUT} is consistently less than the full dynamic range of the A/D converter 26, the digital monitoring circuit will provide feedback to the VGA 24 to amplify V_i to take advantage of the full dynamic range of the
30 A/D converter 26. For example, if the digital output of the A/D converter 26 is consistently within the first 60% of the dynamic range of the A/D converter, the digital

monitoring circuit 50 will provide feedback to the VGA 24 so that the gain of the VGA 24 is increased to amplify the signal provided to the A/D converter 26. The foregoing statistics and information about D_{OUT} is collected by monitoring D_{OUT} 's average signal value and determining whether the average signal is within a certain dynamic range for a certain time period, such as 1.0 msec to 1.0 μ sec. One skilled in the art will appreciate that other statistical and/or signal level sampling methods can be used and are considered to be within the scope of the present invention. As a more detailed example, the following table illustrates a sample gain determination look-up table. The factor to increase the gain by is selected conservatively so as not to overly increase the gain of the VGA 24 in a short period of time thereby saturating the A/D converter 26.

TABLE 1

Monitored Dynamic Range of D_{OUT} :	Increase Gain by Factor of:
0-40%	2 to 2.5
40-50%	1.75 to 2
50-60%	1.5 to 1.66
60-70%	1.3 to 1.43
75-80%	1.2 to 1.25
80-85%	1.15 to 1.18
85-90%	1.08 to 1.11
90-95%	1 to 1.05

The feedback signals produced by the digital monitoring circuit 50 can also be used to assist the analog front end circuit 10 recover signals that have been modulated using different standards, such as pulse position modulating (PPM) and frequency diverse quadrature amplitude modulation (QAM). Accordingly, the digital I/O circuit 28 is provided with a modulation detection and feedback circuit, or QAM/PPM R.GAIN select circuit 52 (FIG. 1). The signal modulation type is detected by the QAM/PPM

R_xGAIN select circuit 52 and a corresponding gain feedback signal for the modulation type (R_xGAIN) is produced to adjust the gain of the VGA 24 to coordinate with the power envelope of the modulation type. The gain feed back signal for the modulation type, R_xGAIN, is factored into the feedback signal produced by the digital monitoring circuit 50 used to determine if the full range of the A/D converter 26 is being utilized.

The QAM/PPM R_xGAIN select circuit 52 takes the digital samples from the A/D converter 26, or D_{OUT}, and processes the digital samples with a Hilbert transformer. Using known techniques, the Hilbert transformer separates an I channel signal, or I, and a Q channel signal, or Q, from the digital samples. The I channel signal and the Q channel signal are input to an envelope detector which, utilizing known techniques, calculates the square root of the sum of I²+Q² and generates an envelope signal representative thereof. The I channel signal and the Q channel signal are also coupled to an equalizer and slicer for recovering QAM modulated data, while the envelope signal is coupled to a decoder circuit for recovering PPM modulated data. The envelope signal is also coupled to each of a QAM automatic gain control (AGC) circuit and a PPM AGC circuit. The QAM AGC circuit functions to generate a QAM gain value (QAM RxGain) while the PPM AGC circuit functions to generate a PPM gain value (PPM RxGain). A multiplexer, controlled by a gain select signal, operates to select one of the QAM RxGain and the PPM RxGain signals. The selected gain signal, either QAM RxGain or PPM RxGain, from multiplexer is input to the digital monitoring circuit 50 in either digital or analog form. The envelope signal is also input to a low pass filter for generating a filtered envelope signal which, in turn, is coupled to a carrier sense circuit for detecting the presence of a continuous carrier (e.g. QAM carrier) and generates the above -mentioned gain select signal to control the multiplexer.

With continued reference to FIG. 2, the VGA 24 is a current feedback amplifier having an amplifying component, or operational amplifier 60. The operational amplifier has a first input, or non-inverting input 62, to which V_i is applied through the first selectable impedance 44. The operational amplifier 60 has a second input, or inverting input 64, connected to an output 66 of the operational amplifier 60 through the feedback impedance 48. The non-inverting input is also connected to a first terminal 68 of the second selectable impedance 46. A second terminal 70 of the second selectable

impedance 46 is connected to a ground or other voltage reference. The input voltage to the VGA 24, or V_I , is connected to a first terminal 72 of the first selectable impedance 44. A second terminal 74 of the first selectable impedance 44 is connected to ground or other voltage reference. An output 76 of the first selectable impedance 44 is connected to the non-inverting input 62 of the operational amplifier 60. The output 66 of the operational amplifier 60 is connected to an input of the A/D converter 26.

As mentioned, the first selectable impedance 44 has a total resistance value of R_1 . A first feedback signal, or signals, controls the first selectable impedance 44 such that a portion of R_1 is present between the second terminal 74 and the output 76 of the first selectable impedance 44. This portion of R_1 , or αR_1 , represents a percentage of impedance connected between the second terminal 74 and the output 78. The balance of R_1 , or $(1-\alpha)R_1$, represents the percentage of R_1 connected between the first terminal 72 and the output 76. A second feedback signal, or signals, controls the second selectable impedance 46 such that a portion of R_1 is present between the inverting input 64, or first terminal 68, and the second terminal 70. This portion of R_2 , or βR_2 , is the amount of impedance between the first terminal 68 and the second terminal 70. As one skilled in the art will appreciate, the gain of the VGA 24 can be expressed by the following equation.

$$\frac{V_O}{V_I} = \alpha \left(\frac{R_F}{\beta R_2} + 1 \right)$$

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Referring to FIG. 3, an embodiment of the first selectable impedance 44 is illustrated in greater detail. The first selectable impedance 44 has a resistor ladder 80, or other type of voltage divider, and a multiplexer 82. The resistor ladder 80 has an overall impedance value of R_1 and is made up of a series of individual resistors 84. The multiplexer 82 selects which part of the resistor ladder 80 is connected between the first terminal 72 and the output 76, or $(1-\alpha)R_1$, thereby also determining the portion of the resistor ladder 80 connected between the second terminal 74 and the output 76, or αR_1 . The selection is made by coupling one of a series of taps 85 to the output 76. One skilled in the art will appreciate that the series of individual resistors 84 making up the resistor ladder 80 need not have the same impedance value. The impedance values of the resistors 84 can be the same, linearly related, or non-linearly related, such as

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logarithmically related. The number of individual resistors 84 and their impedance values can be adjusted to result in almost any transfer curve desired. In fact, the actual values of the individual resistors 84 is less important than the percentage of impedance above and below the selected tap 85 of the first selectable impedance 44.

5 The multiplexer 82 is controlled by one or more feedback lines from the digital monitoring circuit 50. The feedback lines are in the form of multiplexer select lines, or α select, used to control or actuate the multiplexer 82. The multiplexer 82 is a potential source of error for the VGA 24. Therefore, it is desirable to avoid creating a voltage drop across the switching mechanism of the multiplexer 82. Therefore, the switching
10 mechanism of the multiplexer 82 is a series of MOS transistors controlled by the α select feedback lines from the digital monitoring circuit 50. The feedback signals, or α select, are digital signals to provide digital control of the VGA 24. NMOS and CMOS implementations of multiplexers which are adapted to receive digital select signals and multiplex, or couple, one of a plurality of taps, or inputs, to a single output are known in
15 the art. Examples of such multiplexers are described in Donald G. Fink and Donald Christiansen, Electronics Engineers Handbook 3d. Ed., 1989, pgs. 16:49-53, incorporated herein by reference.

Referring to FIG. 4, the second selectable impedance is also provided with a resistor ladder 86 made up of a series of individual resistors 88, or other type of voltage
20 divider, and a multiplexer 90 for coupling one of a series of taps 92 to the first terminal 68. Similar to the first selectable impedance 44, the second selectable impedance 46 receives feedback from the digital monitoring circuit 50 in the form of β select lines to determine which portion of the resistor ladder 86 is connected between the first terminal 68 and the second terminal 70 of the second selectable impedance 46, or βR_2 . The
25 impedance values of the individual resistors 88 can be equal, linearly related or non-linearly related. It should be appreciated that the digital monitoring circuit 50 coordinates the α select and β select feedback signals so that the first selectable impedance 44 and the second selectable impedance 46 can be individually or concurrently adjusted to provide the VGA 24 with the desired gain, attenuation or unity
30 gain. The same type of MOS multiplexer used for the first selectable impedance 44 can be used in the second selectable impedance 46.

It is noted that by using a pair of selectable impedances 44, 46 controllable by the digital monitoring circuit 50 adjust the gain of the amplifier, a high degree of gain control is possible with a small number of individual resistors in the resistor ladders 80, 86. The digital monitoring circuit can be implemented with a microprocessor, comparator circuit or the like. The digital monitoring circuit is configured or programmed with predetermined α and β select feedback values to adjust the one or both of the selectable impedances 44, 46 to attain a desired gain of the VGA 24. For example, the digital monitoring circuit 50 can be provided with a memory for storing a look-up table with α and β select feedback values.

To provide stable amplification of the voltage signal V_i at a constant bandwidth, the operational amplifier 60 of the VGA 24 is implemented as a current feedback amplifier to attain the benefits of constant bandwidth with closed loop gain. It is possible that the analog front end circuit will be used to communicate with other devices with more than one bandwidth. With this in mind, the VGA 24 can be adjusted with a selectable compensation capacitor network 94 (FIG. 5) coupled to the amplifier 60. The operational amplifier 60 is provided with a compensation node 96 (FIG. 2) which is connected to one of a plurality of capacitors 98 through a multiplexer 100. Each of the capacitors 98 has a different capacitance value which corresponds to an appropriate compensation for the amplifier 60 to provide closed loop gain at a selectable constant bandwidth. The multiplexer 100 is the same type of multiplexers 82, 90 used in the first and second selectable impedances 44, 46. The multiplexer 100 is controlled by compensation select feedback lines, or comp. select, controlled either by a bandwidth monitor in the digital monitoring circuit 50, the electronic hybrid circuit 18 or a separate bandwidth monitoring circuit connected to the receive side of the analog front end circuit 10. The selectable compensation capacitor network 94 and the variable gain capability of the VGA 24 allows the VGA 24 to provide an analog voltage signal to the A/D converter 26 which maximizes the dynamic range of the A/D converter 26 as the analog signal V_i amplitude varies and as the bandwidth of the received signal varies.

Although particular embodiments of the invention have been described in detail, it is understood that the invention is not limited correspondingly in scope, but includes

all changes, modifications and equivalents coming within the spirit and terms of the claims appended hereto.

CLAIMS:

1. A data networking device, comprising:
a variable gain amplifier (24);
5 an analog to digital converter (26) for converting an analog output signal of the amplifier to a digital signal; and
a digital signal monitoring circuit (50) for monitoring the digital signal and supplying feedback signals to control the gain of the amplifier as a function of the digital signal, characterised in that the amplifier (24) has a first selectable impedance
10 (44) and a second selectable impedance (46), the impedances being actuated by the feedback signals to adjust the gain of the amplifier, and the digital monitoring circuit (50) monitoring the digital signal to determine the percentage of the dynamic range of the analog to digital converter (26) being used to convert the analog output signal of the amplifier.
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2. A data networking device according to claim 1, wherein the first and second selectable impedances (44, 46) each have a resistor ladder (80, 86) and a multiplexer (82, 90), the multiplexer tapping the resistor ladder based on the feedback signals.
- 20 3. A data networking device according to claim 2, wherein the multiplexer is implemented with MOS transistors and the feedback signals are digital select lines for actuating the multiplexers.
4. A data networking device according to claim 1, wherein the variable gain
25 amplifier is provided with a capacitive compensation circuit (94) for adjusting the bandwidth of the amplifier.
5. A data networking device according to claim 4, wherein the capacitive
30 compensation circuit has a plurality of capacitors (98) one of which is coupled to a compensation node (96) of the variable gain amplifier with a multiplexer (100).

6. A data networking device according to claim 1, wherein the percentage of the dynamic range is a function of the average signal value of the digital signal for a predetermined period of time.

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7. A data networking device according to claim 1, wherein a signal modulation type is determined by a modulation detection and feedback circuit (52), the modulation detection and feedback circuit producing a modulation type gain feedback signal which is factored into the feedback signals to actuate the first and second selectable impedances.

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8. A data networking device according to claim 1, wherein the variable gain amplifier (24) is a current feedback operational amplifier.

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9. A data network device according to claim 1, wherein the first selectable impedance (44) has a resistor ladder (80) having a first terminal (72) connected to receive an analog voltage signal and a second terminal (74) connected to a voltage reference, and a multiplexer (82) for coupling an output (76) of the first selectable impedance to a selected point on the resistor ladder, the output connected to a first input (62) of an amplifier component (60), the feedback signals actuating the multiplexer to select a portion of the resistor ladder to be connected between the first terminal (72) and the first amplifier input (62).

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10. A data network device according to claim 1, wherein the second selectable impedance (46) has a resistor ladder (86) having a first terminal (68) connected to an input of an amplifier component (60) and a second terminal (70) connected to a voltage reference, and a multiplexer (90) for coupling the first terminal (68) to a selected point on the resistor ladder, the feedback signals actuating the multiplexer to select a portion of the resistor ladder to be connected between the input of the amplifier component and the voltage reference.

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11. A data network device according to claim 10, wherein the amplifier component (60) has a feedback impedance (48) connected between an output of the amplifier component and the input of the amplifier component.

5 12. A data network device according to claim 9, wherein the second selectable impedance has a resistor ladder having a first terminal connected to a second input of an amplifier component and a second terminal connected to a voltage reference, and a multiplexer for coupling the first terminal to a selected point on the resistor ladder, the feedback signal actuating the multiplexer to select a portion of the resistor ladder to be
10 connected between the second input of the amplifier component and the voltage reference.

13. A data network device according to claim 12, wherein the amplifier component has a feedback impedance connected between an output of the amplifier component and the second input of the amplifier component.
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14. A method of controlling a variable gain amplifier (24) wherein, an analog output signal of the variable gain amplifier is converted to a digital signal by an analog-to-digital converter (26), characterised in that the method comprises:
20 determining a portion of the dynamic range of the analog to digital converter being used to convert the analog output signal of the variable gain amplifier; and
providing a first feedback signal to a first selectable impedance (44) and providing a second feedback signal to a second selectable impedance (46), the first and second feedback signals adjusting the gain of the amplifier to increase the
25 dynamic range used by the analog to digital converter.

15. A method according to claim 14, wherein the portion of dynamic range used by the analog-to-digital converter is a function of the average signal value of the digital signal for a predetermined period of time.
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16. A method according to claim 14, further comprising the step of selectively coupling a first input of an amplifier component of the variable gain amplifier to an input voltage signal through a portion of a resistor ladder in accordance with the first feedback signal.
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17. A method according to claim 14, further comprising the step of selectively coupling a second input of an amplifier component of the variable gain amplifier to a voltage reference through a portion of a resistor ladder in accordance with the second feedback signal.
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18. A method according to claim 16, further comprising the step of selectively coupling a second input of an amplifier component of the variable gain amplifier to a voltage reference through a portion of a resistor ladder in accordance with the second feedback signal.
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19. A method according to claim 14, further comprising the steps of determining a modulation type of a receive signal, producing a modulation type gain feedback signal and factoring the modulation type gain feedback signal into the first and second feedback signals.
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20. A method according to claim 14, wherein the first and second feedback signals are digital select signals for controlling multiplexers in the first and second selectable impedances.
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21. A method according to claim 14, further comprising the steps of determining a bandwidth of a receive signal and providing a feedback signal to couple one of a series of compensation capacitors to a compensation node of the variable gain amplifier.