

CLAIMS

1. A memory cell comprising:
 - an active electrode consisting of an active electrode material;
 - a first noble electrode in contact with the active electrode, the first noble electrode being a patterned electrode comprising a noble electrode material;
 - a resistive switching layer in contact with the active electrode and the first noble electrode; and
 - a second noble electrode comprising a noble electrode material, the second noble electrode in contact with the resistive switching layer;wherein the first noble electrode comprises a grid comprising a plurality of openings;
wherein the first noble electrode is configured to block current from flowing through;
wherein portions of the resistive switching layer in contact with the active electrode, and extending within the plurality of openings of the grid form conduction channels such that one or more conduction paths are formed in the conduction channels when a potential difference is applied along one direction across the resistive switching layer;
wherein the active electrode material is selected from a group consisting of titanium (Ti), nickel (Ni), tantalum (Ta), hafnium (Hf), and aluminum (Al) such that the active electrode and the resistive switching layer form a Schottky barrier of 1.1 eV or below; and
wherein the first noble electrode and the resistive switching layer form a Schottky barrier of 1.2 eV or above.
2. The memory cell according to claim 1,
 - wherein the noble electrode material of the first noble electrode is same as the noble electrode material of the second noble electrode.
3. The memory cell according to claim 1,

wherein the noble electrode material of the first noble electrode is different from the noble electrode material of the second noble electrode.

4. The memory cell according to claim 1,
wherein the noble electrode material of the first noble electrode and the noble material electrode material of the second noble electrode are electrically conductive materials, and are selected from a group consisting of noble metals, conductive oxides, and conductive nitrides.
5. The memory cell according to claim 1,
wherein the active electrode material is an electrically conductive material, and is an active metal or an active metal alloy.
6. The memory cell according to claim 1,
wherein the resistive switching layer comprises an oxide material.
7. The memory cell according to claim 10,
wherein the oxide material is a transition metal oxide or a perovskite oxide.
8. A method of forming a memory cell, the method comprising:
forming an active electrode consisting of an active electrode material;
forming a first noble electrode in contact with the active electrode, the first noble electrode being a patterned electrode comprising a noble electrode material;
forming a resistive switching layer in contact with the active electrode and the first noble electrode; and
forming a second noble electrode comprising a noble electrode material, the second noble electrode in contact with the resistive switching layer;
wherein the first noble electrode comprises a grid comprising a plurality of openings;
wherein the first noble electrode is configured to block current from flowing through;

wherein portions of the resistive switching layer in contact with the active electrode, and extending within the plurality of openings of the grid form conduction channels such that one or more conduction paths are formed in the conduction channels when a potential difference is applied along one direction across the resistive switching layer;

wherein the active electrode material is selected from a group consisting of titanium (Ti), nickel (Ni), tantalum (Ta), hafnium (Hf), and aluminum (Al) such that the active electrode and the resistive switching layer form a Schottky barrier of 1.1 eV or below; and

wherein the first noble electrode and the resistive switching layer form a Schottky barrier of 1.2 eV or above .

9. The method according to claim 12,

wherein the active electrode is formed before the first noble electrode is formed on the active electrode;

wherein the resistive switching layer is formed in contact with the active electrode and the first noble electrode after forming the active electrode and the first noble electrode; and

wherein the second noble electrode is formed on the resistive switching layer after the resistive switching layer is formed.

10. The method according to claim 12,

wherein the second noble electrode is formed by any one deposition process selected from a group consisting of atomic layer deposition (ALD), chemical vapor deposition (CVD), pulsed laser deposition (PLD), and sputtering.