IPW COPY
9702894-A

NON-VOLATILE MEMORY WITH EMBEDDED PROGRAMMABLE CONTROLLER

STATEMENT OF RELATED APPLICATIONS

This application claims priority from U.S. Provisional Application No. 60/024,355, filed August 19, 1996, the disclosure of which is herein incorporated by reference.

BACKGROUND OF THE INVENTION

The present invention relates to non-volatile memory systems and more particularly to a system that integrates hierarchically organized non-volatile memory with a programmable controller for performing operations on the non-volatile memory.

New multimedia applications for computers make great demands on system performance both in terms of processing power and memory capacity. For example, 1-D and 2-D Discrete Cosine Transforms and Inverse Discrete Cosine Transforms are necessary to implement JPEG and MPEG compression and decompression. Wavelet compression requires various digital filtering operations. Fractal compression potentially requires both filtering and extensive search operations. Image enhancement also requires digital filtering. All of these operations require extensive computations and/or comparisons to be performed on large amounts of data.

One solution is to simply assign these tasks to the CPU of a computer system. Multimedia performance will then be limited by the CPU speed as well as the speed of access to memory. If the computer system is running other tasks concurrently, these other tasks will also be performed slowly.

Another solution is to provide supplemental hardware. For example, a computer system may be equipped with an additional board including a digital signal processing circuit and memory, both dedicated to multimedia tasks. This approach, however, adds considerable expense and furthermore, the added memory duplicates resources already available within the computer system.

Similar problems are posed by system security. Controlling access to the computer and/or protecting the confidentially of data stored and/or transmitted by the

computer requires that encryption and decryption be implemented. Encryption and decryption represent yet another potential drain on the computer's processing power. Furthermore, encryption and decryption key information are typically stored on the hard drive of the computer where they are difficult to protect.

SUMMARY OF THE INVENTION

The present invention provides computer systems with additional performance for demanding applications while adding little additional hardware. In one embodiment, a slave device for a host computer system combines an embedded programmable controller with non-volatile memory, local RAM, and interface logic. The host computer system treats the slave device as if it would be a hierarchical memory system such as a conventional disk drive on which it may store and retrieve files. Additionally, the host computer system may program the controller to perform operations on stored information, including image processing and/or data compression. The non-volatile memory may include a disk drive, optical disk, writable CD-ROM, and/or non-volatile solid state memory.

In accordance with a first aspect of the invention, apparatus for providing non-volatile data storage and additional processing to a host computer system includes a non-volatile memory system including at least one non-volatile memory device. The non-volatile memory system includes a hierarchical memory structure and responds to hierarchical memory structure control commands received from the host computer system by storing and retrieving information from the host computer system. The apparatus further includes a programmable controller. The programmable controller operates according to a control program received from the host computer system. The programmable controller responds to one or more commands command from host computer system to invoke the control program. The commands cause the programmable controller to operate on information stored in the non-volatile memory system.

In accordance with a second aspect of the invention, apparatus for non-volatile data storage and high-speed data processing in a host computer system includes a plurality of units. Each such unit includes a non-volatile memory system that includes at least one non-volatile memory device. The non-volatile memory system implements a hierarchical memory structure and responds to hierarchical memory structure control commands by storing and retrieving information. Each such unit further includes a

programmable controller. The programmable controller operates an externally configurable control program and responding to a command from the host computer system to invoke the control program. The control program operates on the information stored in the non-volatile memory system. Each such unit further includes an interface system for exchanging information with others of the plurality of units. The plurality of units is programmable by the host computer system to operate concurrently on stored information.

A further understanding of the nature and advantages of the inventions herein may be realized by reference to the remaining portions of the specification and the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 depicts a computer system suitable for incorporating the present invention.

Fig. 2A depicts a storage system combining hierarchical storage and supplemental processing for installation within the computer system of Fig. 1 in accordance with one embodiment of the present invention.

Fig. 2B depicts the storage system of Fig. 2A augmented with computer accessible memory which may be accessed as a part of system memory of the host system of Fig. 1 in accordance with one embodiment of the present invention.

Fig. 3 depicts a network of storage systems similar to the one in Fig. 2 in accordance with one embodiment of the present invention.

Fig. 4 depicts how subunits of storage systems similar to the one in Fig. 2 are functionally interconnected in an MPEG compression application of the multiple storage system configuration of Fig. 3 in accordance with one embodiment of the present invention.

Fig. 5 depicts functional elements of a digital portable telephone which acts as a host computer system to the storage system of Fig. 2 in accordance with one embodiment of the present invention.

Fig. 6 depicts a digital motion camera unit that acts as a host computer system to the storage system of Fig. 2 in accordance with one embodiment of the present invention.

Fig. 7 depicts a personal digital assistant that acts as a host computer system to the storage system of Fig. 2 in accordance with one embodiment of the present invention.

DESCRIPTION OF SPECIFIC EMBODIMENTS

Fig. 1 depicts a host computer system 10 suitable for incorporating the present invention. Host computer system 10 includes a bus 12 which interconnects major subsystems such as a central processor 14, a system memory 16 (typically RAM), an input/output (I/O) controller 18, an external device such as a display screen 24 via a display adapter 26, serial ports 28 and 30, a keyboard 32, a floppy disk drive 36 operative to receive a floppy disk 38, and a CD-ROM player 40 operative to receive a CD-ROM 42. Many other devices can be connected such as a mouse 46 connected via serial port 28 and a network interface 48 connected via serial port 30. Bus 12 may include signal components which may or may not operate together. Bus 12 may be divided into constituent buses for particular purposes such as memory access, I/O access, etc.

In accordance with one embodiment of the present invention, host computer system 10 incorporates a special storage system 50 that incorporates both non-volatile memory and programmable processing for performing operation on the contents of its memory. One function of storage system 50 is to take the place of a combination of a disk controller, such as an IDE controller or SCSI controller, and a hard disk drive. To host computer system 10, storage system 50 appears as a hierarchical memory system able to receive and respond to hierarchical memory control commands to store and retrieve files within a stored directory structure. In accordance with the present invention, storage system 50 is programmable to respond to other commands to perform data processing operations on stored information.

Fig. 2A depicts a particular configuration of storage system 50 in accordance with one embodiment of the present invention. Storage system 50 includes a host interface 202, an embedded programmable controller 204, an internal RAM 206, an internal ROM 208, one or more internal DSP circuits 210, one or more internal coder circuits 212, and one or more content addressable memory (CAM) units 214. Storage system 50 further includes an error correction coding unit 216, a non-volatile memory interface 218, and a plurality of non-volatile memory devices 220. Host interface 202 is

connected to embedded programmable controller 204, internal RAM 206, internal ROM 208, DSP circuit 210, coder circuit 212, CAM 214 by an internal bus structure 222. Of course, many of these components may be omitted in accordance with the present invention.

Storage system 50 may be physically implemented as a printed circuit board, a multi-chip module, or a single integrated circuit. The individual circuits of Fig. 2 may be independent integrated circuits. With a greater level of integration, multiple components may be combined into a single integrated circuit.

Host interface 202 interacts with bus 12 of computer system 10. For example, bus 12 may be a PCI bus. Host interface 202 will then be equipped to interact with the PCI bus. In part, host system 10 interacts with storage system 50 as if it were a hierarchical memory structure operating under the direction of an SCSI or IDE controller. Host system 10 uses storage system 50 to save and retrieve files. The interaction between host system 10 and host interface 202 for the purpose of data storage and retrieval is explained in Messmer, The Indispensable PC Hardware Book, (Addison Wesley, 2nd Ed. 1995), pp. 731-838, the contents of which are herein incorporated by reference for all purposes.

Embedded programmable controller 204 interprets the storage and retrieval commands received from host system 10 and directs the flow of stored and retrieved data between host interface 202 an non-volatile memory interface 218. Embedded programmable controller 204 is preferably an ARM-7 TDMI available from ARM Limited of Cambridge, England. Error correction coding unit 216 is interposed in the data path between host interface 202 and non-volatile memory interface 218. Error correction coding unit 216 applies an error correcting code to data be stored on non-volatile memory devices 220. For retrieved data, error correction coding unit 216 checks for errors, corrects errors, and removes the code. Error correction coding unit 216 may be programmable via host interface 202.

Non-volatile memory devices 220 are preferably 4MB or larger flash memory devices internally optimized to support MS-DOS sectors. In an alternative embodiment, a hard disk drive, or writable optical drive serves as non-volatile memory. Non-volatile memory interface 220 is particularized to generate whatever data, address, and control signals are needed to interact with non-volatile memory devices 220.

Embedded programmable controller 214 operates in accordance with a control program. A portion of this control program resides in ROM 208 and cannot be easily modified. Another portion is modifiable by host system 10 and resides within non-volatile memory devices 220 and within internal memory of controller 214. The portion within ROM 208 handles basic controller operation and file storage and retrieval. File storage and retrieval is preferably handled as specified by the ATA disk control specification, ANSI-X3-221-1994, as available from the American National Standards Institute of New York, New York, the contents of which are herein incorporated by reference.

Preferably, a minimal set of extensions to the ATA interface command set includes a "write to internal memory of embedded controller," "execute embedded controller memory," "reset embedded controller write memory pointer." When host system 10 is to configure embedded controller 204, it first invokes the command, "reset embedded controller write memory pointer." It then invokes "write to internal memory of embedded controller," as many times as necessary to load the controller's internal memory with the control program. After the program is loaded, the host system may invoke the control program by issuing an "execute embedded controller memory" command. The internal memory of the controller may be either volatile or non-volatile.

Further extensions to the ATA interface command set may include but are not limited to "open new internal file," "write internal sector," "read internal sector," "close internal file," "execute internal file," "terminate internal execution," and "hide internal file." The referenced files file sectors are stored in non-volatile memory system 220. The modifiable portion of the control program performs operations on information stored within non-volatile memory devices 220.

By modifying this control program, host computer system 10 may configure storage system 50 to perform various functions independently of CPU 14. For example, storage system 50 may perform JPEG or MPEG image compression on image data to be written within non-volatile memory devices 220. Storage system 50 may also implement image enhancement algorithms to improve resolution to, e.g., correct CCD array flaws or suppress noise in captured NTSC frames. RAM 206 may be used for storage of intermediate results.

In accordance with one embodiment of the present invention, other circuitry may cooperate with embedded programmable controller 204. For example, if

included, digital signal processing circuit(s) 210 may assist in digital signal processing operations. Such operations may include calculation of 1-D and 2-D linear transformations such as Discrete Cosine Transforms and Inverse Discrete Cosine Transforms (IDCT) as used in JPEG and MPEG. Other 1-D and 2-D filters may programmed to support other compression schemes such as wavelet-based compression. Digital signal processing circuit(s) 210 may also perform quantization operations to coarsen the data from the 1-D and 2-D filters. Digital signal processing circuit(s) 210 may be one or more components such as the Motorola 56000 series available from Motorola of Schaumburg, Illinois, or the Oak DSP core developed by DSP Group, Inc. of Santa Clara, California. The control program for digital signal processing circuit(s) 210 is also modifiable by host computer system 10 and stored in non-volatile memory devices 220.

If coder(s) 212 are included, they may assist in other operations needed for image compression and decompression. For example, coder(s) 212 may perform run-length encoding of the results of the outputs of the 2-D DCT or 2-D filters implemented by digital signal processing circuit(s) 210. Coder(s) 212 may also perform bit packing operations to support compression or run-length decoding and unpacking to support decompression. Coder(s) 212 may also perform Huffman encoding and decoding to support the JPEG and MPEG schemes. Coder(s) 212 may also perform bit scrambling to support decryption and/or encryption.

Wavelet and fractal compression/decompression may be supported by DSP circuit(s) 210, coder (s) 212, and CAM(s) 214. Fractal image compression and decompression uses CAM(s) 214 to search for recurring patterns. Further details of fractal image compression and decompression are explained in D.R. McGregor, et al., "Faster Fractal Compression", Dr. Dobb's Journal, (January 1996), Y. Fisher, "Fractal Image Compression", SIGGRAPH '92 Course Notes, Y. Fischer, et al., "Fractal (Self-VQ) Encoding of Video Sequences", Proceedings of the SPIE, Visual Communications and Image Processing, (September 1994), Barnsley, et al., Fractal Image Compression, (A.K. Peters Ltd. 1993), and U.S. Patent No. 5,065,447 issued to Barnsley et al. on November 12, 1991. The contents of all five references are herein incorporated by reference.

Storage system 50 may also enhance the security of encryption and decryption. Password data to control access by host computer system 10 or for

encrypting and decrypting data on storage system 50 may be maintained in non-volatile memory system 220. The password data may include one-way key data for decrypting passwords entered by a user. Embedded programmable controller 204 operates to preclude external retrieval to the one-way key data, enhancing security. When the user initially selects the password using application software running on host computer system 10, embedded programmable controller 204 translates the password into the key data that will be used to decrypt the password and stores it in a private memory area of non-volatile memory system 220. This private area is accessible only by embedded programmable controller 204 for password decryption and is not accessible via the ATA hierarchical memory control commands. Such a password may be used to allow access by certain applications on host computer system 10, to control access to otherwise hidden files on non-volatile memory system 220, or to access a key to decrypt or encrypt data stored on non-volatile memory system 220. Encryption and decryption may be supported by coder(s) 212.

To accommodate highly processing-intensive tasks, multiple storage systems as in Fig. 2 may be combined in an array for high speed processing. Such an arrangement is highly suitable for MPEG, wavelet, and fractal compression or decompression. To accommodate this configuration. storage system 50 may include one or more other interfaces 224 for this purpose. Information to be stored or retrieved and control program information may be passed through one of N, preferably 4 or more ports: COM1, COM2, COM3, COM4, etc. Host interface 202 may also be used for interfacing with other storage systems instead of with host bus 12.

Fig. 2B depicts an extension to storage system 50 wherein a computer accessible memory 226 is physically integrated with storage system 50. Although only a portion of the components depicted in Fig. 2A are replicated in Fig. 2B, it is to be understood that any of the components of Fig. 2A may be included with a storage system 50 that is physically integrated with computer accessible memory 226. Computer accessible memory 226 connects to a host system memory bus 228 which may form a portion of bus 12. Computer accessible memory 226 operates within system memory 16 and may include one or both of volatile and non-volatile memory circuitry. Host bus 12 may include signals which are independent and concurrently active relative to the computer memory access signals whereby data processing elements in storage system 50 may independently and concurrently operate upon or transmit to these signals to support

data compression (including image compression), decompression, encryption, decryption or other high speed data processing requirements.

Furthermore, a cache 230 and a further error correction coding unit 232 are interposed between computer accessible memory 226 and host system memory bus 228. Cache 230 optimizes system memory access performance for host system 10 and is particularly valuable in non-volatile memory applications. Error correction coding unit 232 improves the reliability and life expectancy (known as mean time between failure) of computer accessible memory 226.

Fig. 3 depicts such an array configuration 300 including multiple storage systems 50 and a global bus controller 302. Global bus controller 302, known to those of skill in the art, serves as the direct interface to host bus 12. Global bus controller 302 directs information to be stored, control program information, storage and retrieval commands, and processing commands to a particular storage system 50. Global bus controller 302 receives retrieved information from storage systems 50 and sends it onto host bus 12. For storage and retrieval purposes, the host system interacts with global bus controller 302 with conventional storage and retrieval commands as would be used by a SCSI or IDE hard disk controller. These commands are augmented with additional commands for requesting special processing operations.

To distribute commands, control program information, and information to be stored and retrieved, a 2-D binary tree communication network interconnects multiple storage systems 50. Fig. 3 shows a particular configuration with 16 storage systems 50. The various COM ports and host interface are used to interconnect the storage systems 50. A part of the control program for each storage system 50 concerns providing the necessary connectivity within the context of the overall network. In many image compression schemes, each storage system 50 performs the processing associated with a strip of an image or a group of strips. The network also incorporates a 2-dimensional nearest-neighbor-with-edge-units-wrapping-around-to-corresponding-edge-units communications scheme often known as a torus communications grid.

Fig. 4 depicts how subunits of storage system 50 are functionally interconnected in an MPEG compression application of the multiple storage system configuration of Fig. 3. The various subunits perform the functions necessary to MPEG compression. Global bus input pixel data 402 comes from global bus controller 302 either directly or via one or more other storage systems 50. A scan line block input

input buffer 404 is implemented with RAM 206. A 2-D Discrete Cosine Transform Engine and Quantizer 406 transforms the pixel data and quantizes the results in accordance with quantization control information delivered via a compensation feedback input 408 and other quantization control information received from global bus controller 302. The result is quantized block DCT coefficient data which is stored in a block DCT coefficient buffer 410, also implemented by RAM 206.

The MPEG compression schemes take advantage of similarities between successive frames of pixels and the fact that differences between successive frames often consist of motion of one or more objects against a fixed background. Accordingly, it is useful to store a last block of DCT coefficients in a last block DCT coefficient buffer 412, also implemented by RAM 206. Furthermore, because motion may involve importing an object from an adjacent pixel area handled by a different storage system, an input line 414 connects to one or more of the COM ports or host interface 202. Similarly, a neighborhood DCT block buffer 416 also implemented by RAM 206 receives DCT coefficients from one or more other storage systems 50. A motion detection circuit 418 can then generate motion data based on the difference between the current DCT coefficients and previous ones. Motion detection circuit 418 may be implemented by DSP circuit(s) 210 and/or CAM unit(s) 214. Motion detection circuit 418 generates data for special difference frames for characterizing a difference from a previous frame.

A logic circuit 419 switches between the DCT coefficient data of the current frame and the difference data and also generates data for controlling the final grouping of MPEG data into I-frames, B-frames, and P-frames as known to those of skill in the art. Logic circuit 419 also generates a portion of the quantization control data for compensation feedback input 408. A bit packing circuit 420 composes the frames, and writes them to a non-volatile write and/or output buffer implemented by RAM 206. From there, the packet data are written to non-volatile memory system 220.

Storage system 50 implements a non-volatile memory circuit with user configurable encryption capabilities. For example, storage system 50 may store a phone number directory in encrypted form which may be decrypted only upon entering a password. The key for verifying the password is stored in non-volatile memory system 220 and may not be retrieved or altered. Instead of a password, a voice sample or thumb print may be analyzed to provide access. Again the key for verifying the voice

sample or thumb print is not accessible outside of storage system 50. The processing for verification, encryption, and/or decryption may be performed by the various processing components within storage system 50, especially coder(s) 212.

A host computer system as depicted in Fig. 1 is but one application of storage system 50. Other devices may also take advantages of the features of storage system 50. Fig. 5 depicts functional elements of a digital portable telephone 500 which acts as a kind of host computer system. A microphone 502 converts the user's speech to an input analog audio signal. An A/D converter 504 converts this input analog audio signal to an input digital audio signal. Similarly, a D/A converter 506 converts an output digital audio signal to an output analog audio signal to be fed to a speaker 508. A spread spectrum encoder/decoder and control/interface 510 performs the control functions for the telephone, controlling interaction with a public wireless telephone network, decoding received spread spectrum signals and generating encoded spread spectrum signals. An LCD display 512 displays user interface information. A keypad 514 allows the user to control the operation of telephone 500.

An IF modulator/demodulator 516 performs the modulation and demodulation functions at an intermediate frequency (IF). An RF transceiver 518 converts the IF signal to an allocated frequency for transmission by an antenna 520 to the public wireless network. Furthermore, RF transceiver 518 receives a signal from antenna 520 and converts it to IF for demodulation by IF modulator/demodulator 516.

Further inaccessible encryption and decryption keys stored in non-volatile memory system 220 may be used for encrypting and decrypting voice signals to enhance the security of wireless communications. Invoking secure voice transmission also typically requires entry of a password or analysis of a thumbprint or voice sample. Encryption and decryption of the voice signal is performed by the various processing components within storage system 50. For added security, storage system 50 may be detachable from portable telephone 500.

Fig. 6 depicts a digital motion camera unit 600 that acts as a host computer system to storage system 50. Digital motion camera unit 600 includes a CCD array 602 for detecting an image and converting the image to an electrical signal. An LCD display 604 displays a user interface. A user controls digital motion camera unit 600 via a keypad 606. Internal control and interface circuitry 608 incorporates a CCD interface 610, an LCD interface 612, a human input interface 614, and global bus

controller 302. In accordance with one embodiment of the present invention, a removable card incorporates 618 the array of storage systems 50 shown in Fig. 3 and an interface 620 to connect to global bus controller 302. Removable card 618 stores moving image data captured by CCD array 602 and performs MPEG compression, as discussed with reference to Fig. 4, on the moving image data to increase storage capacity. Removable card 618 may plug into a player (not shown) to replay the captured moving image data. At that time, the processing components of removable card 618 may perform MPEG decompression.

Fig. 7 depicts a personal digital assistant 700 that acts as a host computer system to one or more storage systems 50. An LCD screen 702 displays a user interface. A user may enter data or control the operation of personal digital assistant 700 by using a keypad 704 or other assorted peripherals 706 such as a stylus. Intermediate results and control information are stored in a RAM 708. A personal digital assistant control/interface 710 serves as the principle processor of personal digital assistant 700. For long term storage of data and software, personal digital assistant 700 uses one or more storage systems 50. Fig. 7 shows one of the storage systems 50 as being removable. For user security, one or more of storage systems 50 may store encrypted data accessible via a user password. As was discussed above, the key for verifying the password is not accessible outside storage system 50. Without the password, even the presence of encrypted files may not be visible.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereunto without departing from the broader spirit and scope of the invention as set forth in the appended claims. Many such changes or modifications will be readily apparent to one of ordinary skill in the art. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense, the invention being limited only by the provided claims and their full scope of equivalents.

WHAT IS CLAIMED IS:

1. Apparatus for providing non-volatile data storage and additional processing to a host computer system, said apparatus comprising:

a non-volatile memory system including at least one non-volatile memory device, said non-volatile memory system responding to hierarchical memory structure control commands received from said host computer system by storing and retrieving information from said host computer system; and

a programmable controller, said programmable controller receiving a first control program from said host computer system, and responding to a first command from said host computer system to invoke said first control program, said first control program operating on said information stored in said non-volatile memory system, wherein said non-volatile memory system and said programmable controller together implement a hierarchical memory structure.

2. The apparatus of claim 1 further comprising a RAM device for storing intermediate results of said first control program.

3. The apparatus of claim 1 wherein said non-volatile memory system stores said first control program.

4. The apparatus of claim 1 further comprising a host interface that couples said non-volatile memory system and said programmable controller to said host computer system.

5. The apparatus of claim 1 further comprising a ROM device for storing a non-modifiable second control program of said programmable controller.

6. The apparatus of claim 1 further comprising an error correction coding system coupled to said non-volatile memory system that applies an error correcting code to information stored in said non-volatile memory system and that removes said error correcting code from information retrieved from said non-volatile memory system, whereby errors are detected and corrected.

* C L M S *

7. The apparatus of claim 6 wherein said error correction coding system is programmable from said host computer system.

8. The apparatus of claim 1 further comprising a digital signal processor operating in conjunction with said programmable controller.

9. The apparatus of claim 8 wherein said digital signal processor is programmable from said host computer system.

10. The apparatus of claim 1 further comprising a programmable component independent of said programmable controller and operating in conjunction with said programmable controller.

11. The apparatus of claim 10 wherein said programmable component is optimized for performing bit packing and unpacking to support compression and decompression.

12. The apparatus of claim 10 wherein said programmable component supports encryption and decryption.

13. The apparatus of claim 1 further comprising an additional interface component for exchanging information with a system external to said apparatus.

14. A plurality of apparatus as in claim 13 interconnected for data processing under control of said host computer system.

15. The apparatus of claim 1 further comprising a content addressable memory component accessible to said programmable controller.

16. The apparatus of claim 1 wherein said non-volatile memory system comprises a hard disk drive.

17. The apparatus of claim 1 wherein said non-volatile memory system comprises a non-volatile solid state memory device.

18. The apparatus of claim 1 wherein said non-volatile memory system comprises an optical disk drive.

19. The apparatus of claim 1 wherein said non-volatile memory system comprises a writable CD-ROM.

20. The apparatus of claim 1 wherein said programmable controller performs encryption using a key stored in said non-volatile memory system.

21. The apparatus of claim 1 wherein said programmable controller performs password verification using a key stored in said non-volatile memory system.

22. The apparatus of claim 1 wherein said programmable controller performs decryption using a key stored in said non-volatile memory system.

23. The apparatus of claim 1 wherein certain information stored in said non-volatile memory system is inaccessible to said host computer system.

24. The apparatus of claim 23 wherein said certain information comprises a key for one of password verification, encryption, and decryption.

25. The apparatus of claim 1 wherein said host computer issues a second command to said programmable controller to receive data to be part of said first control program.

26. The apparatus of claim 25 wherein said host computer issues a third command to start reception of data for said first control program.

27. The apparatus of claim 1 further comprising:

a supplemental memory system physically integrated with said programmable controller and non-volatile memory system and accessible as a part of system memory to said host computer system.

28. The apparatus of claim 27 wherein said supplemental memory system comprises non-volatile memory.

29. The apparatus of claim 28 further comprising error control coding circuitry to apply error coding to data stored in said memory system accessible as a part of system memory.

30. The apparatus of claim 28 further comprising:

a cache interposed between said memory system and said host computer system optimizing memory access performance of said host computer system.

31. Apparatus for non-volatile data storage and high-speed data processing in a host computer system, said apparatus comprising:

a plurality of units, each said unit comprising:

a non-volatile memory system including at least one non-volatile memory device, said non-volatile memory system responding to hierarchical memory structure control commands by storing and retrieving information;

a programmable controller, said programmable controller operating an externally configurable control program, and responding to a command from said host computer system to invoke said control program, said control program operating on said information stored in said non-volatile memory system, wherein said programmable controller and said non-volatile memory system together implement a hierarchical memory structure; and

an interface system for exchanging information with others of said plurality of units; and wherein

said plurality of units being programmable by said host computer system to operate concurrently on stored information.

32. The apparatus of claim 31 wherein each said unit further comprises a programmable component independent of said programmable controller and operating in conjunction with said programmable controller.

33. The apparatus of claim 32 wherein said programmable component is optimized for performing bit packing and unpacking to support compression and decompression.

34. The apparatus of claim 32 wherein said programmable component supports encryption.

35. The apparatus of claim 32 wherein said programmable component comprises a digital signal processing circuit.

36. The apparatus of claim 31 wherein each of said plurality of units further comprises a content-addressable memory.

37. A host computer system comprising:

a host CPU;

a host bus; and

apparatus for providing non-volatile data storage and additional processing to said host computer system, said apparatus comprising:

a non-volatile memory system including at least one non-volatile memory device, said non-volatile memory system and responding to hierarchical memory structure control commands received from said host computer system by storing and retrieving information from said host computer system; and

a programmable controller, said programmable controller operating a first control program received from said host computer system via said host bus, and responding to a command from said host CPU to invoke said first control program, said first control program operating on said information stored in said non-volatile memory system, wherein said non-volatile memory system and said programmable controller together implement a hierarchical memory system.

* C L M S *

38. The host computer system of claim 37 wherein said host computer system is a personal digital assistant.

39. The host computer system of claim 37 wherein said non-volatile memory system stores a key for at least one of encrypting data, decrypting data, and password verification.

40. The wireless telephone unit of claim 37 wherein said key is inaccessible to said host bus.

41. A wireless telephone unit comprising:

an RF transceiver for transmitting and receiving data via a wireless network;

a microphone for capturing input audio signals;

a speaker for outputting audio responsive to an output audio signal;

wireless telephone control circuitry that receives said input audio signals and provides said output audio signals and provides a modulated output signal to said RF transceiver and receives a modulated input signal from said RF transceiver to implement telephone operation via said microphone and said speaker;

a non-volatile memory system including at least one non-volatile memory device, said non-volatile memory system responding to hierarchical memory structure control commands received from said wireless telephone control circuitry by storing and retrieving information from said wireless telephone control circuitry; and

a programmable controller, said programmable controller operating a first control program received from said wireless telephone control circuitry, and responding to a command from said wireless telephone control circuitry to invoke said first control program, said first control program operating on said information stored in said non-volatile memory system, wherein said non-volatile memory system and said programmable controller together implement a hierarchical memory system.

42. The wireless telephone unit of claim 41 wherein said non-volatile memory system stores a key for at least one of encrypting telephone number data,

decrypting telephone number data, encrypting voice data, decrypting voice data, and password verification.

43. The wireless telephone unit of claim 42 wherein said key is inaccessible to said wireless telephone control circuitry.

44. A digital motion camera unit comprising:

a CCD array for capturing moving image data;

a camera control circuit that accepts said moving image data and relays said moving image data to a bus interface;

a storage system coupled to said camera control circuit via said bus interface and comprising a plurality of units, each said unit comprising:

a non-volatile memory system including at least one non-volatile memory device, said non-volatile memory system responding to hierarchical memory structure control commands by storing and retrieving information;

a programmable component, said programmable component operating an externally configurable control program, and responding to a command from said camera control circuit to invoke said control program, said control program operating on said information stored in said non-volatile memory system, wherein said programmable controller and said non-volatile memory system together implement a hierarchical memory structure; and

an interface system for exchanging information with others of said plurality of units; and

said plurality of units operating concurrently on stored information.

45. The digital motion camera unit of claim 44 wherein said storage system is removable.

46. The digital motion camera unit of claim 44 wherein said non-volatile memory stores said moving image data and said programmable component operates to compress said moving image data.

47. The digital motion camera unit of claim 46 wherein said programmable component operates to compress said moving image data in accordance with an MPEG compression scheme.

48. The digital motion camera unit of claim 46 wherein said programmable component comprises a programmable controller.

49. The digital motion camera unit of claim 46 wherein said programmable component comprises a digital signal processing circuit.

NON-VOLATILE MEMORY WITH EMBEDDED PROGRAMMABLE CONTROLLER

ABSTRACT OF THE DISCLOSURE

Computer systems may be provided with additional performance for demanding applications while adding little additional hardware. For example, a slave device for a host computer system combines an embedded programmable controller with non-volatile memory, local RAM, and interface logic. The host computer system treats the slave device as if it would be a hierarchical memory system such as a conventional disk drive on which it may store and retrieve files. Additionally, the host computer system may program the controller to perform operations on stored information, including image processing and/or data compression. The non-volatile memory may include a disk drive, writable CD-ROM, optical drive, or non-volatile solid state memory.

Fig.2A

This Sheet Has Been Replaced

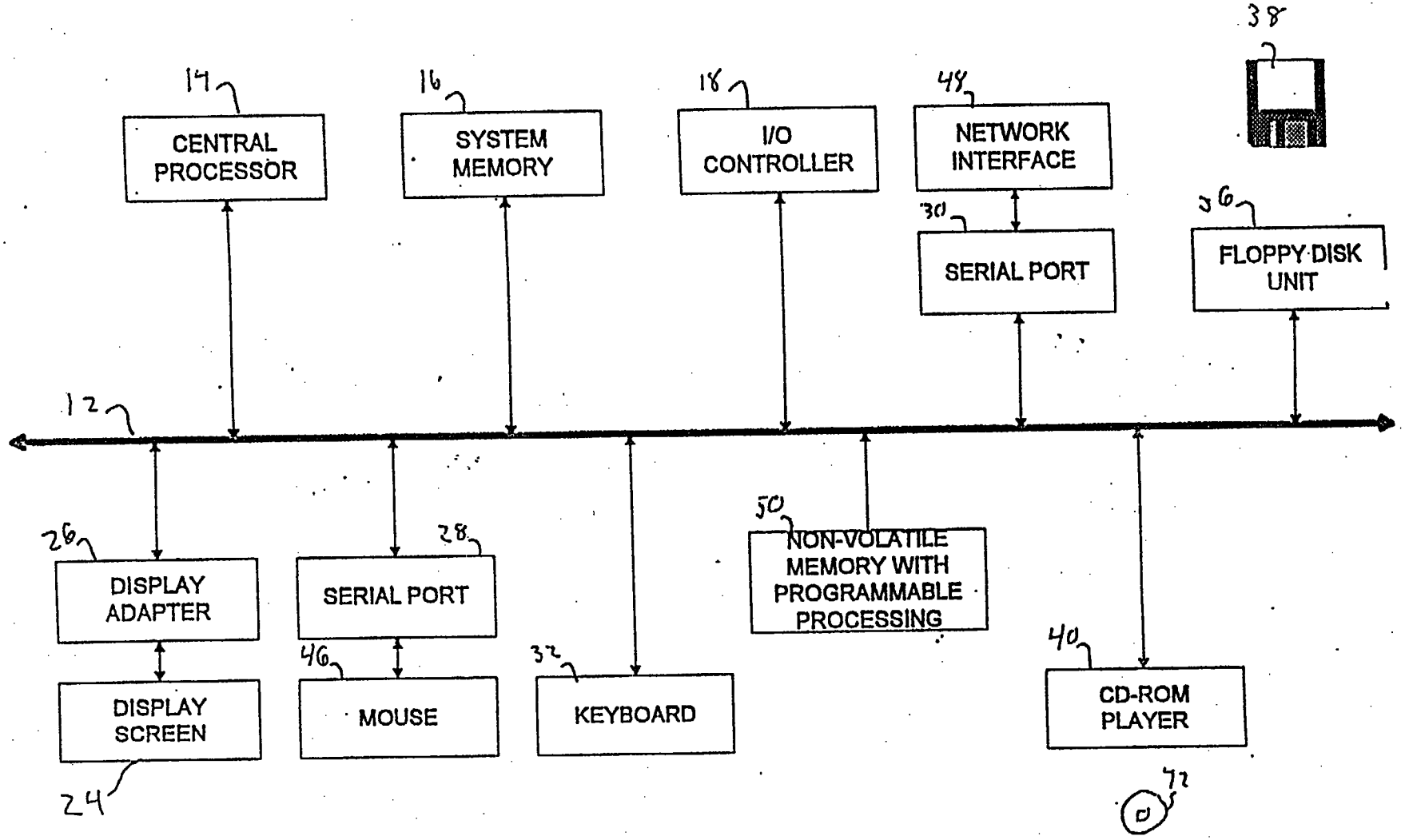


Fig. 1

THIS SHEET HAS BEEN REPLACED

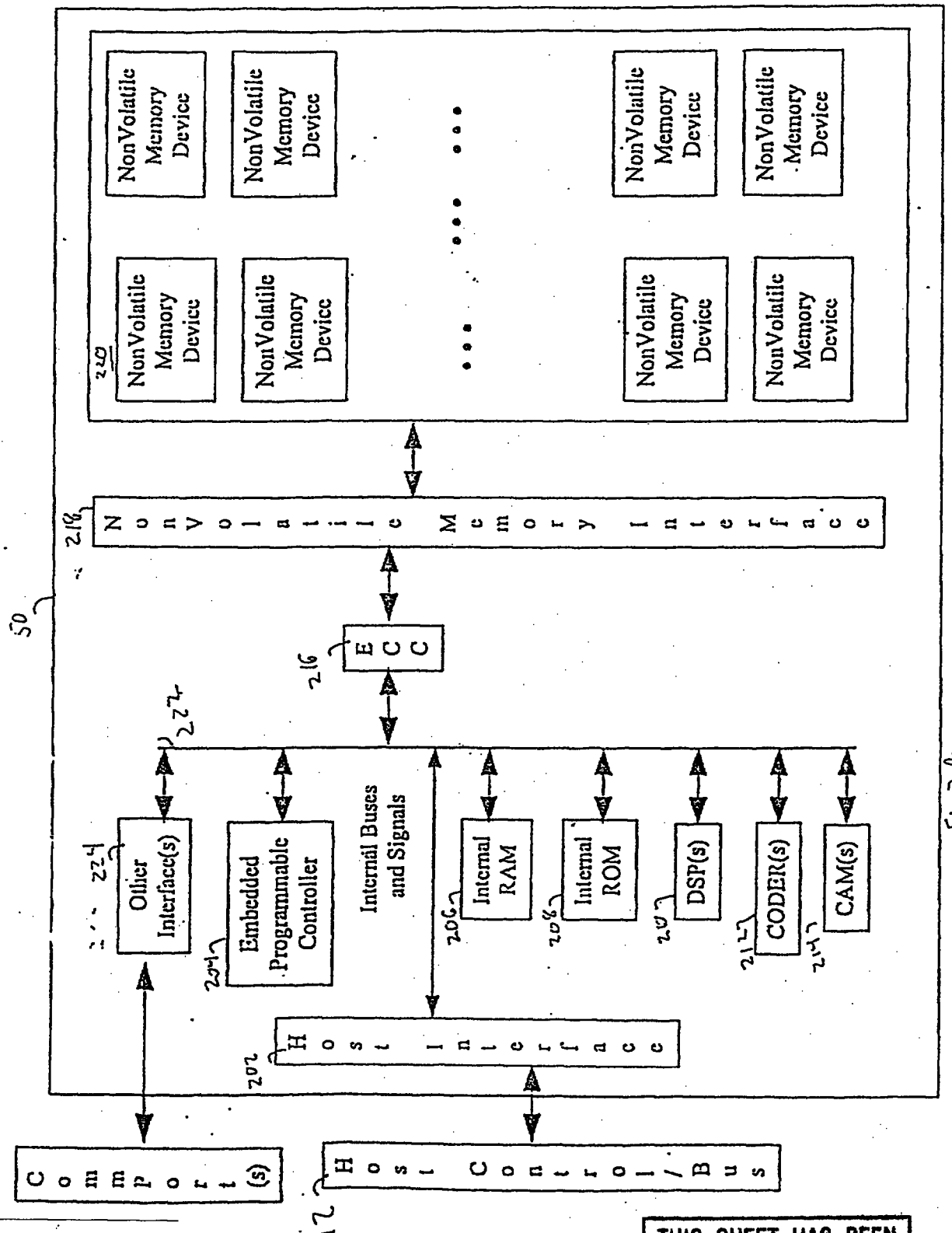


Fig 2A

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

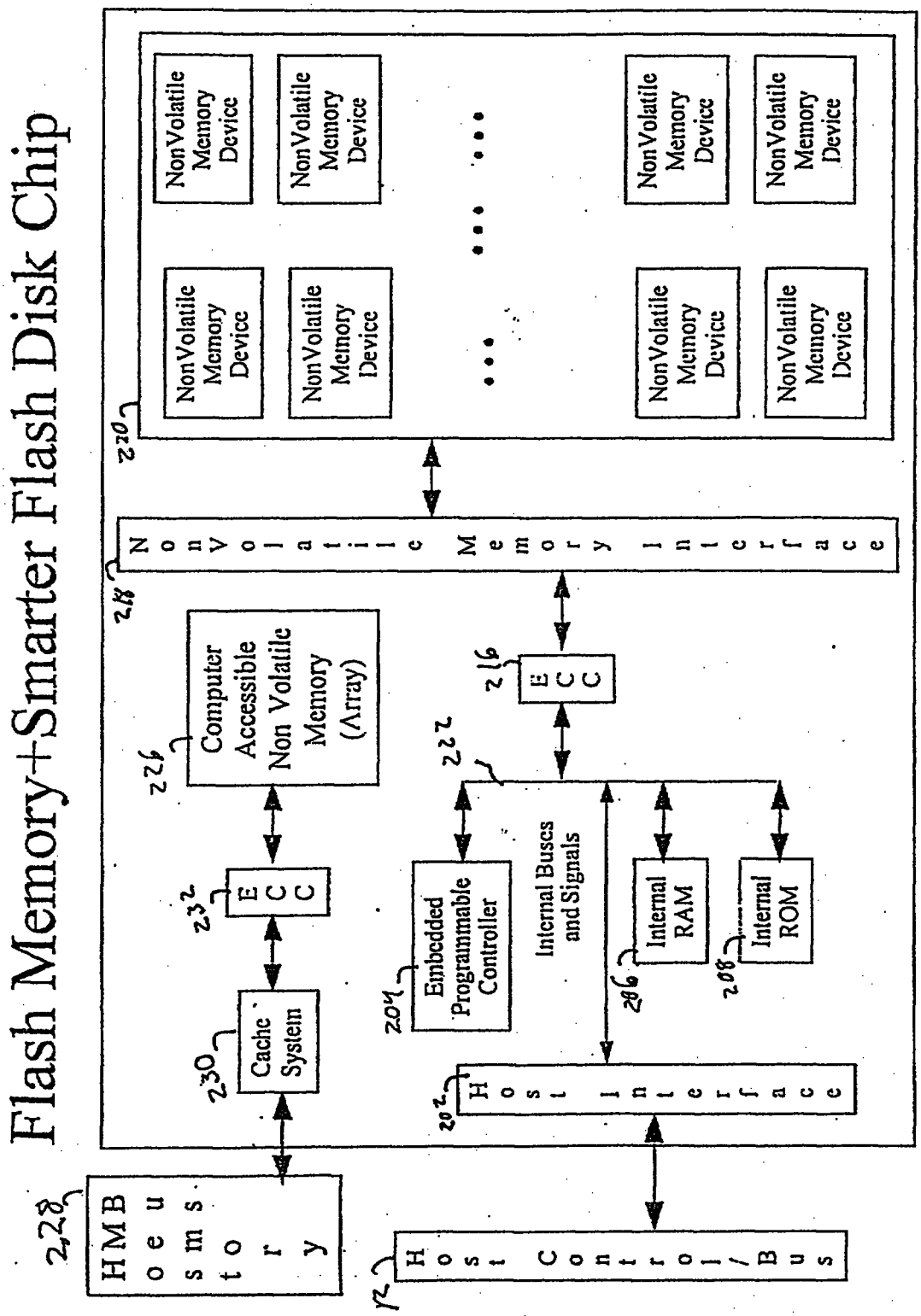


Fig. 2B

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

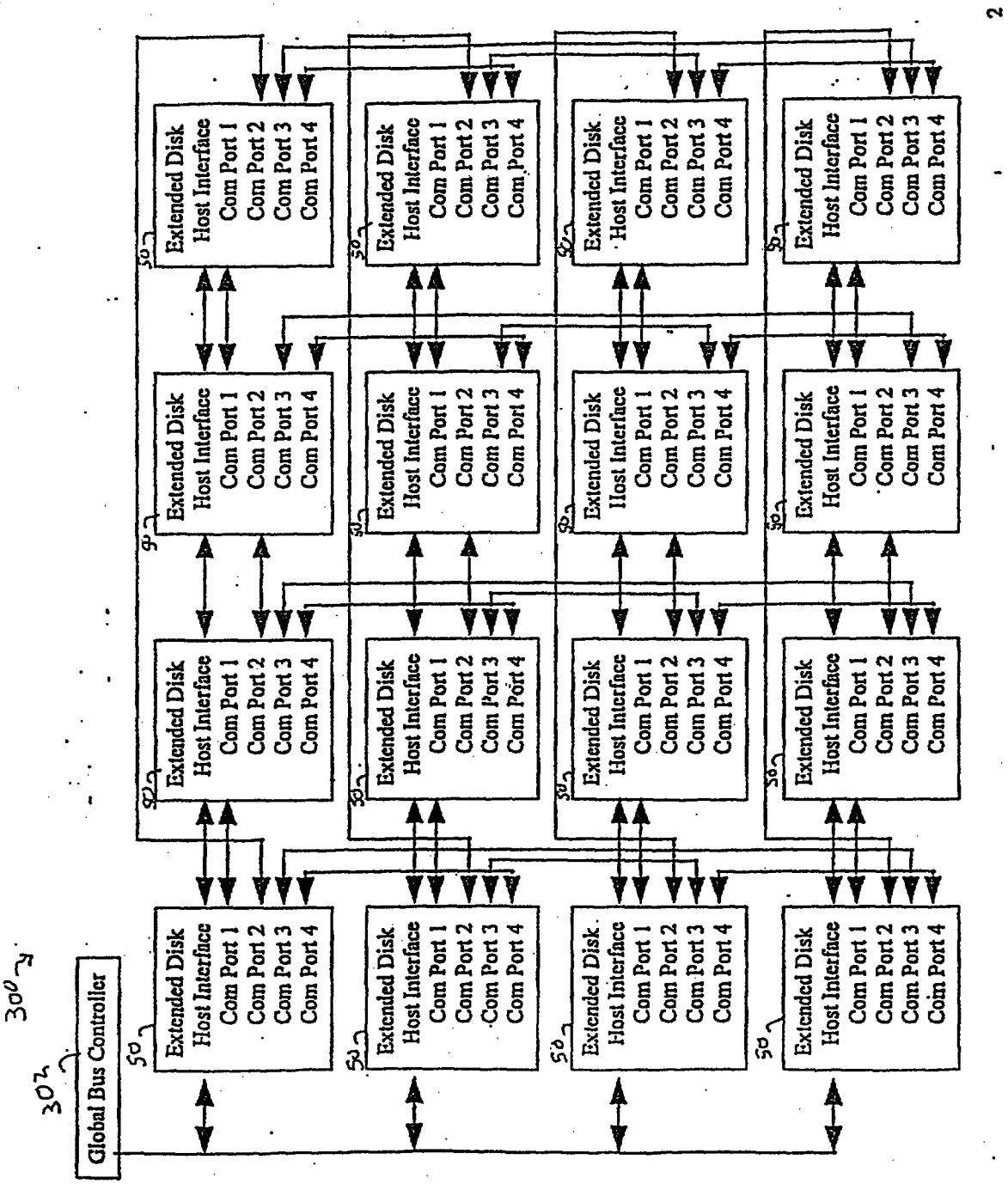


Fig. 3

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

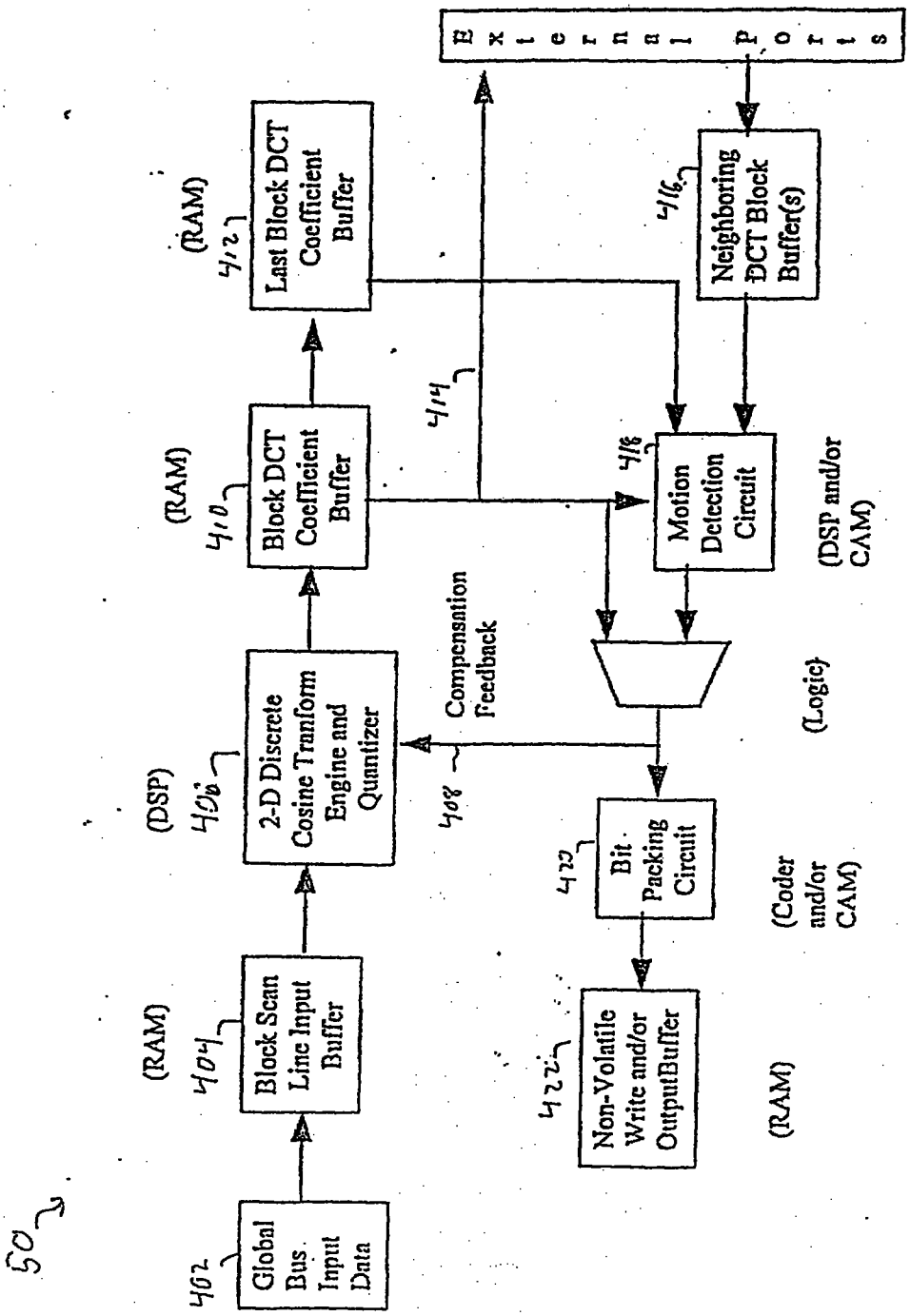


Fig. 4

THIS SHEET HAS BEEN REPLACED

This Sheet Has Been Replaced

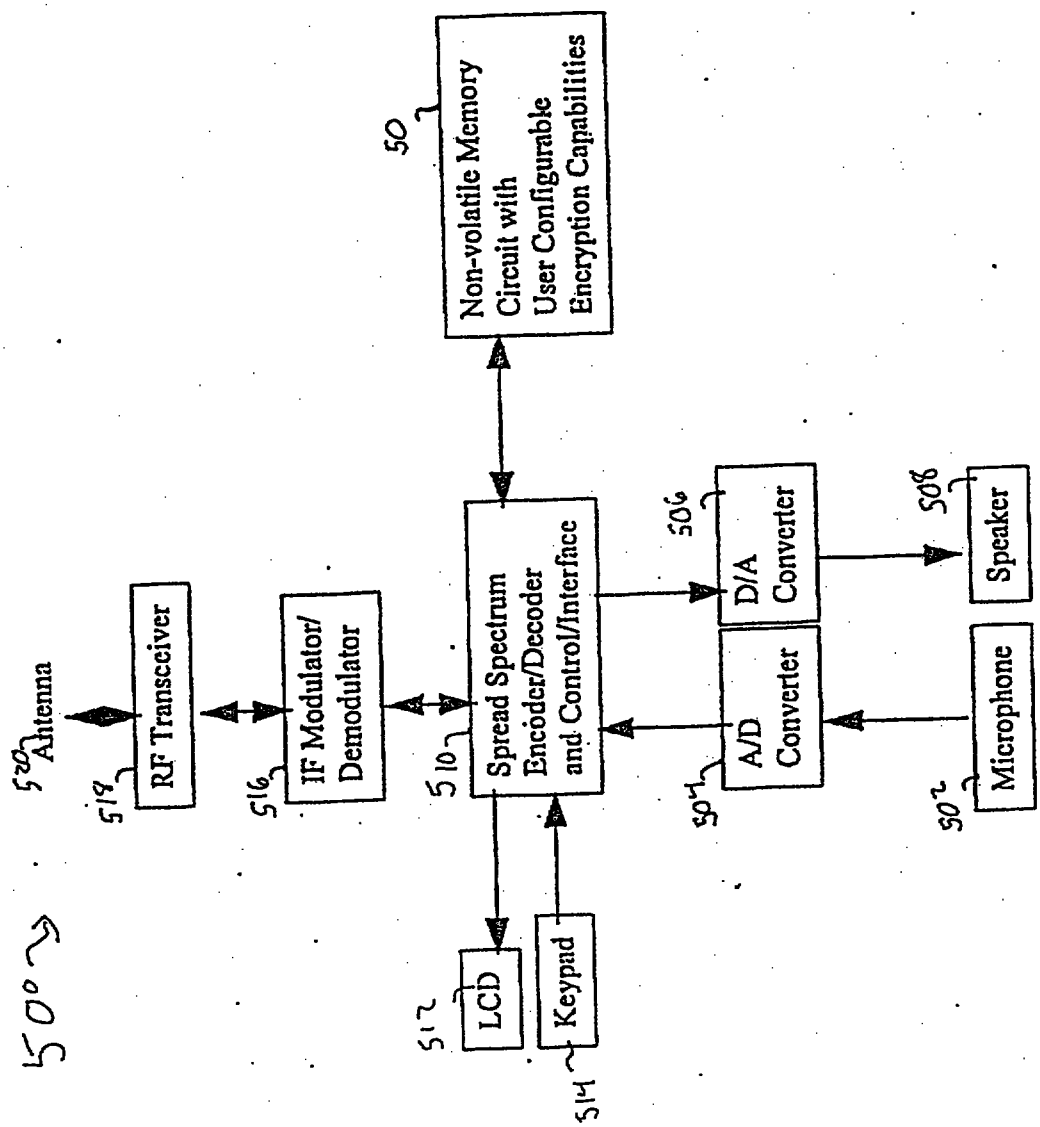


Fig. 5

THIS SHEET HAS BEEN REPLACED

This Sheet Has Been Replaced

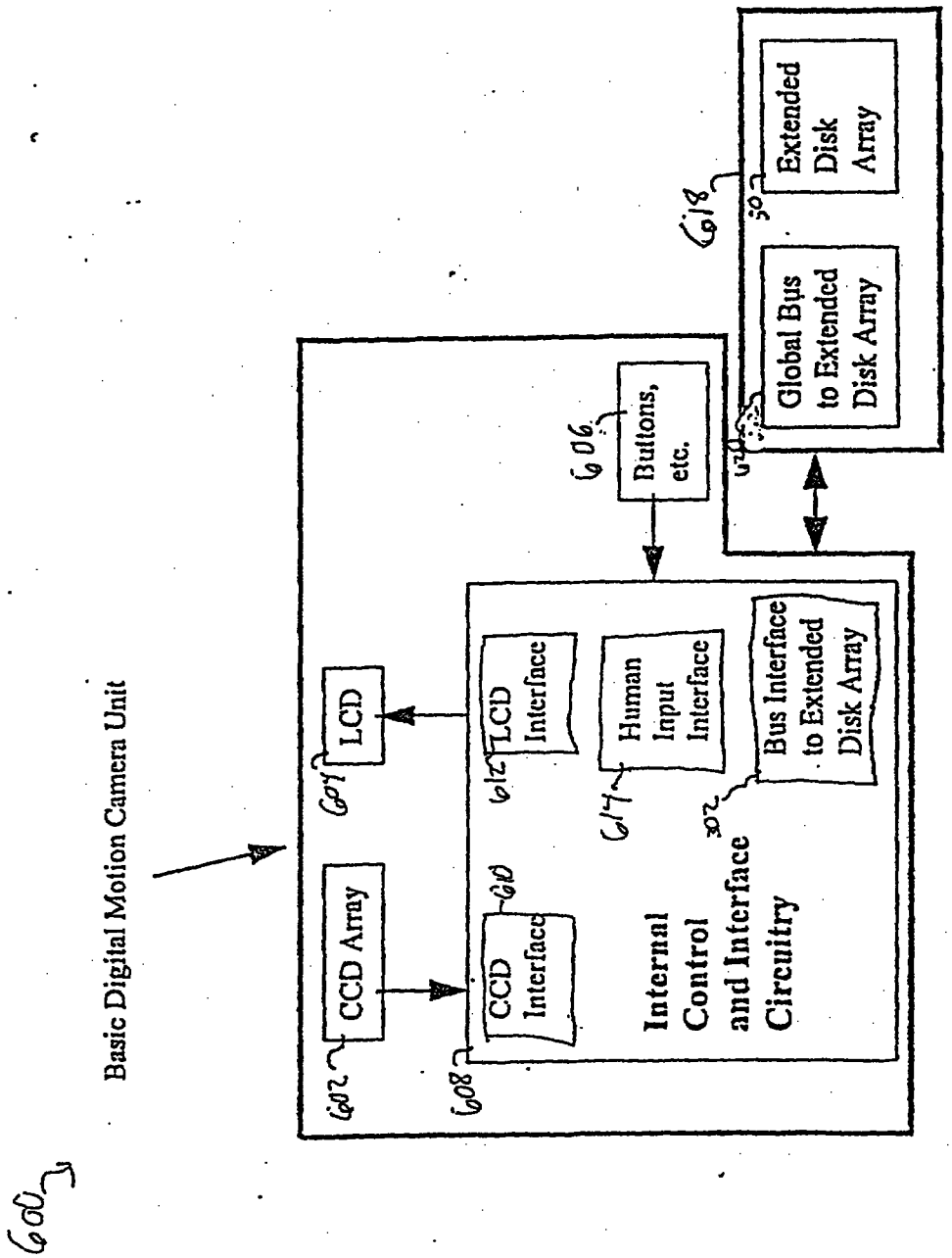


Fig. 6

This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED

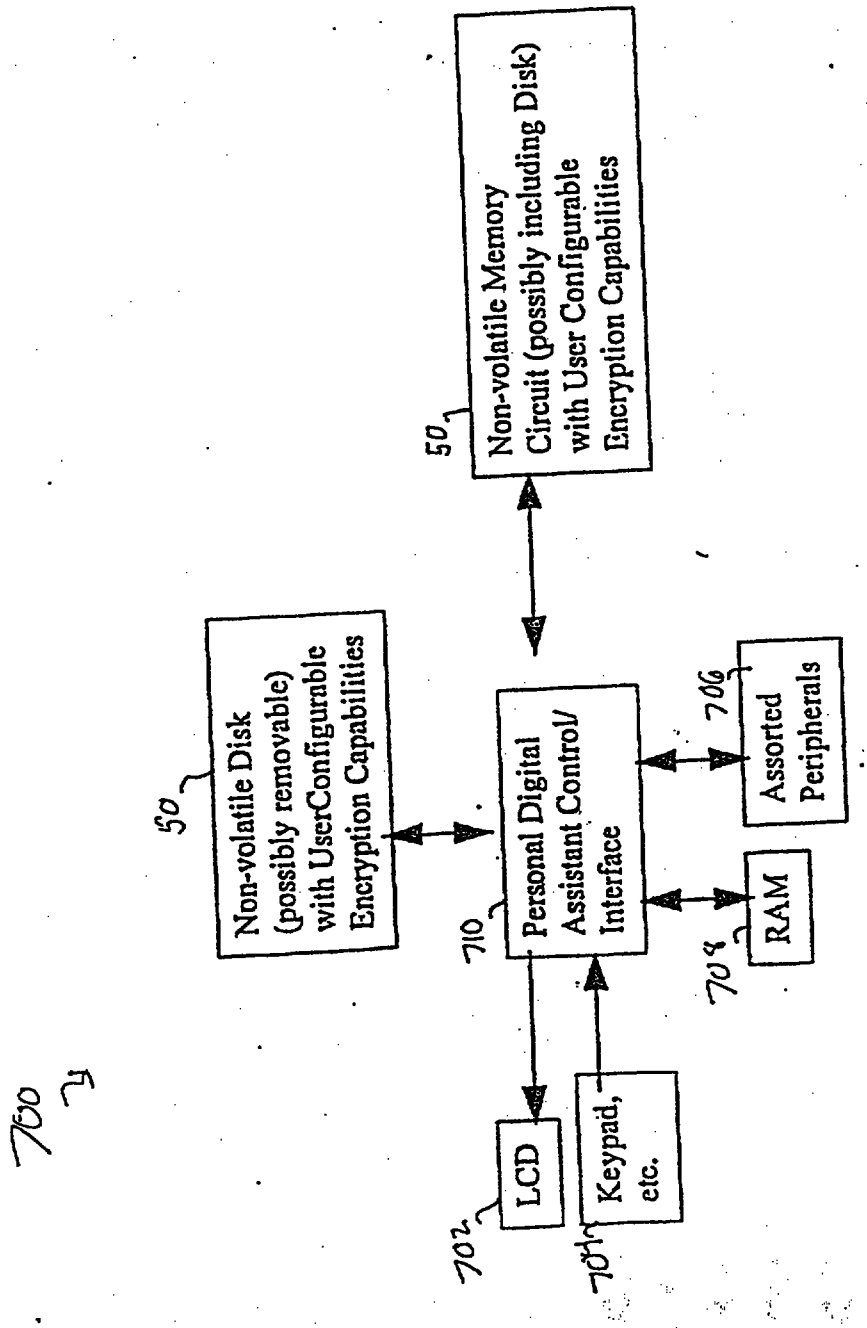


Fig. 7

THIS SHEET HAS BEEN REPLACED

This Sheet Has Been Replaced

REPLACEMENT SHEETS SG
☐ Description : paged ..... to paged .....
☐ Claim(s) : paged ..... to paged .....
☑ Drawing(s) : paged 1 to paged 8
☐ Abstract : paged ..... to paged .....

DATE OF RECEIPT .....

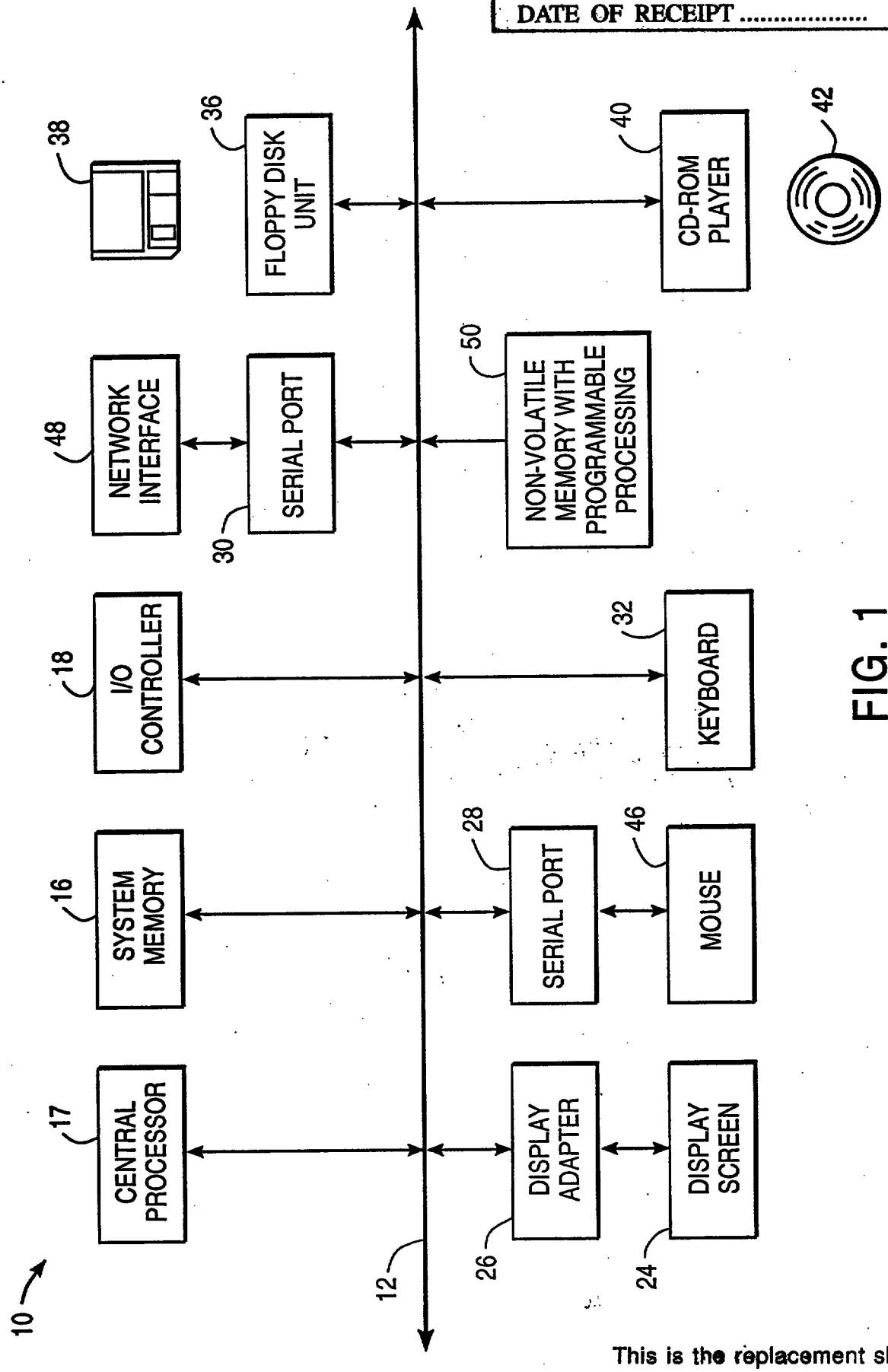


FIG. 1

This is the replacement sheet

Date: 08 SEP 1997

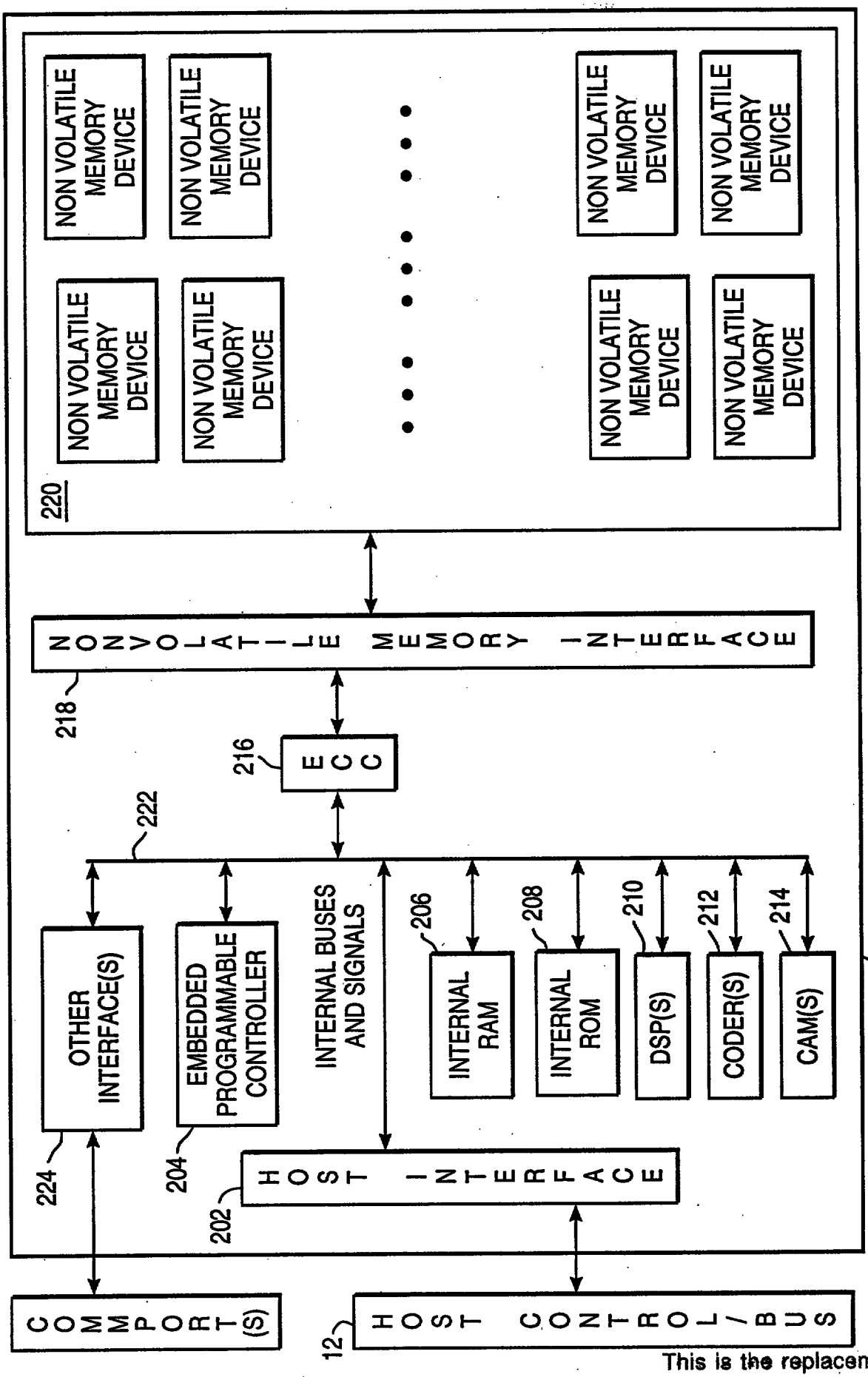


FIG. 2A

This is the replacement sheet

Date: 08 SEP 1997

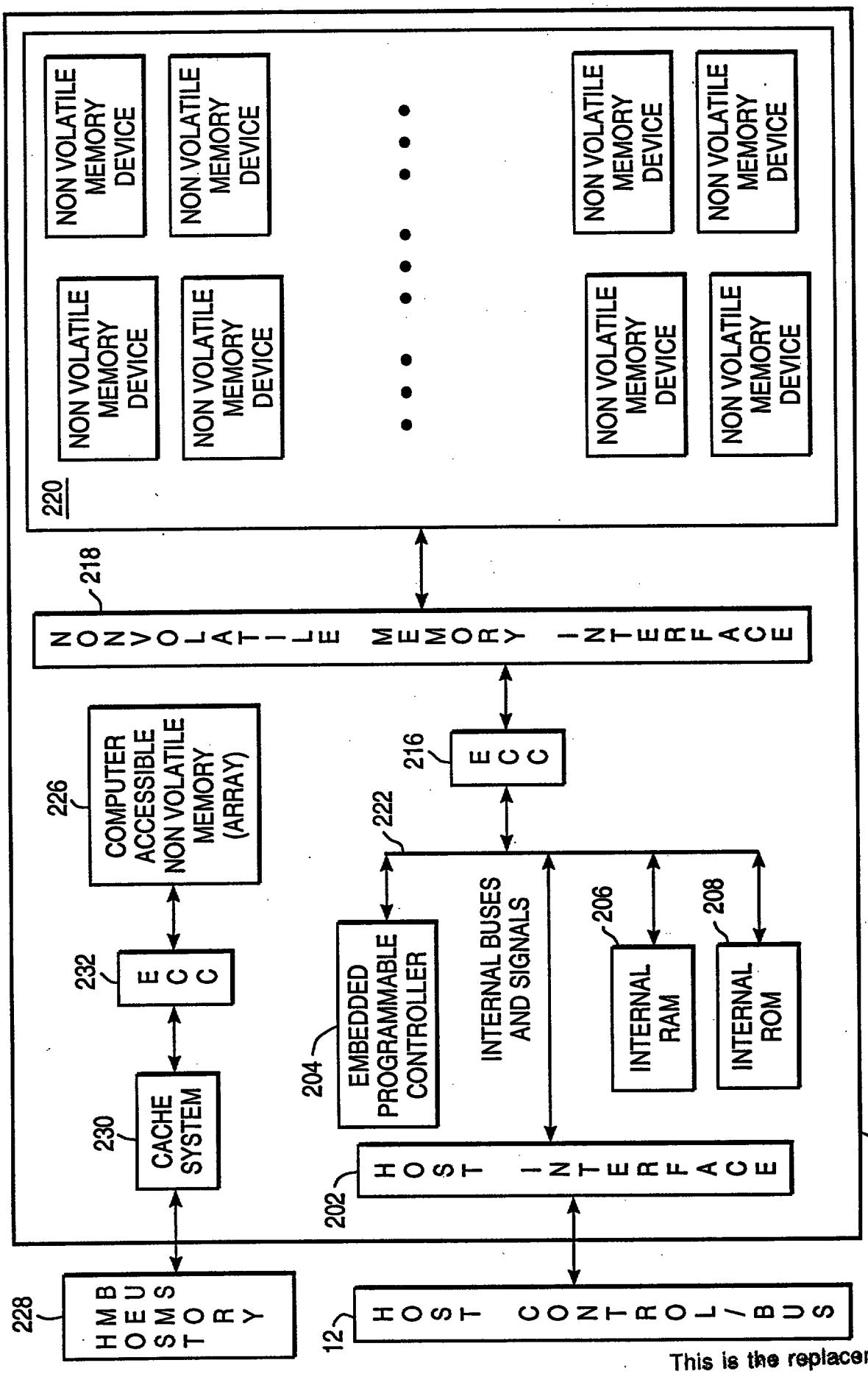


FIG. 2B FLASH MEMORY + SMARTER FLASH DISK CHIP

This is the replacement sheet

Date: 08 SEP 1997

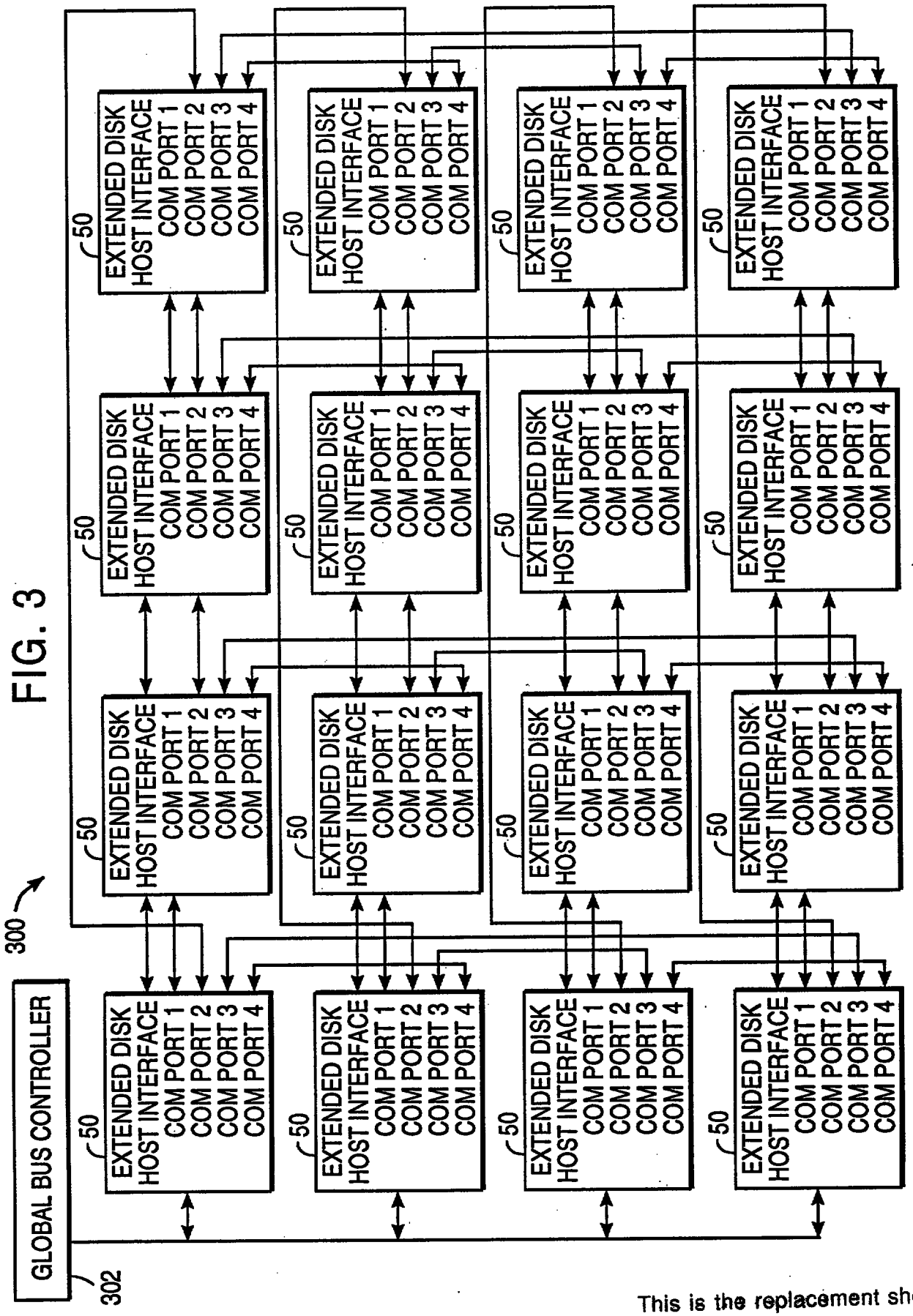


FIG. 3

This is the replacement sheet

Date: 08 SEP 1997

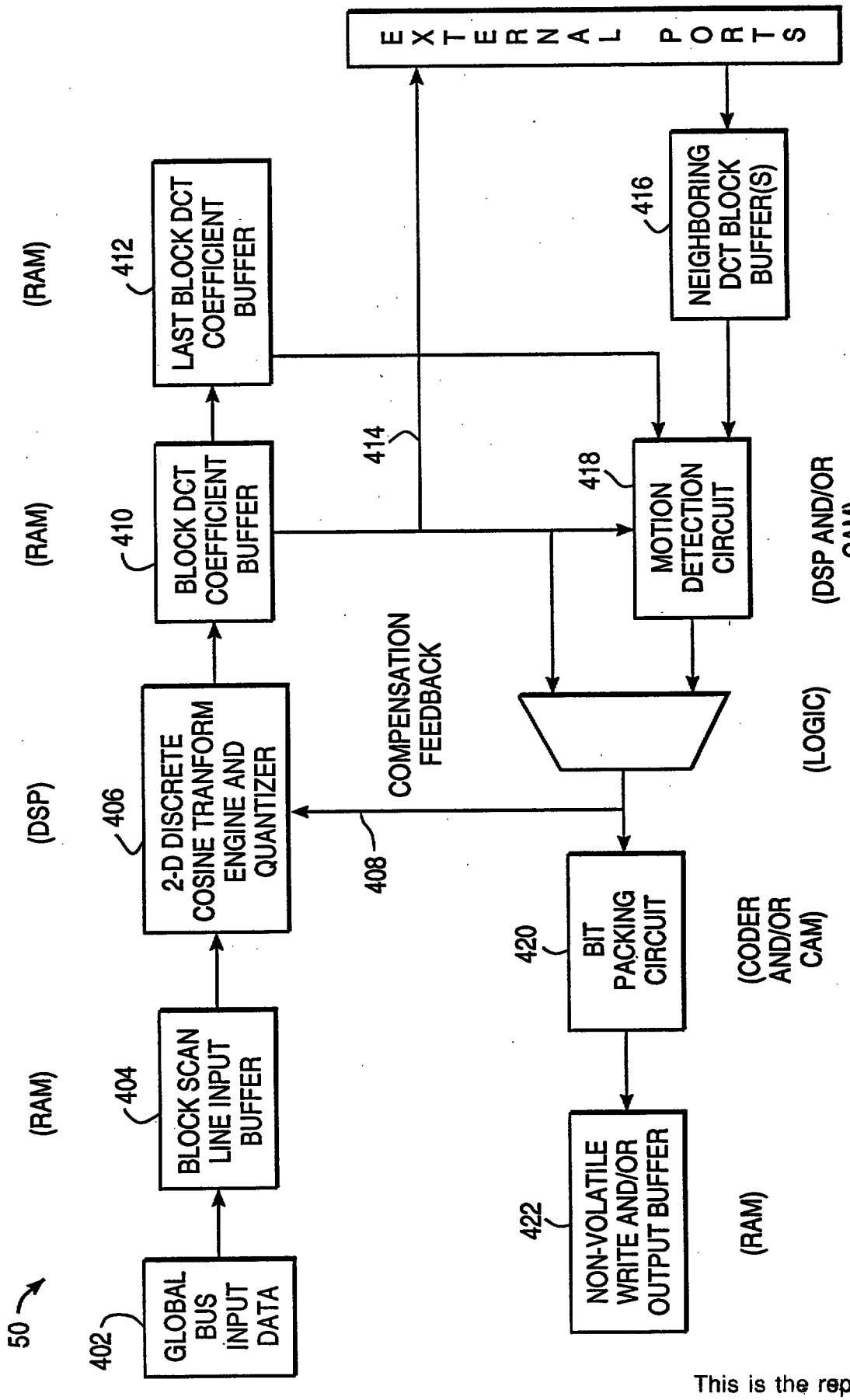


FIG. 4

This is the replacement sheet

Date: 08 SEP 1997

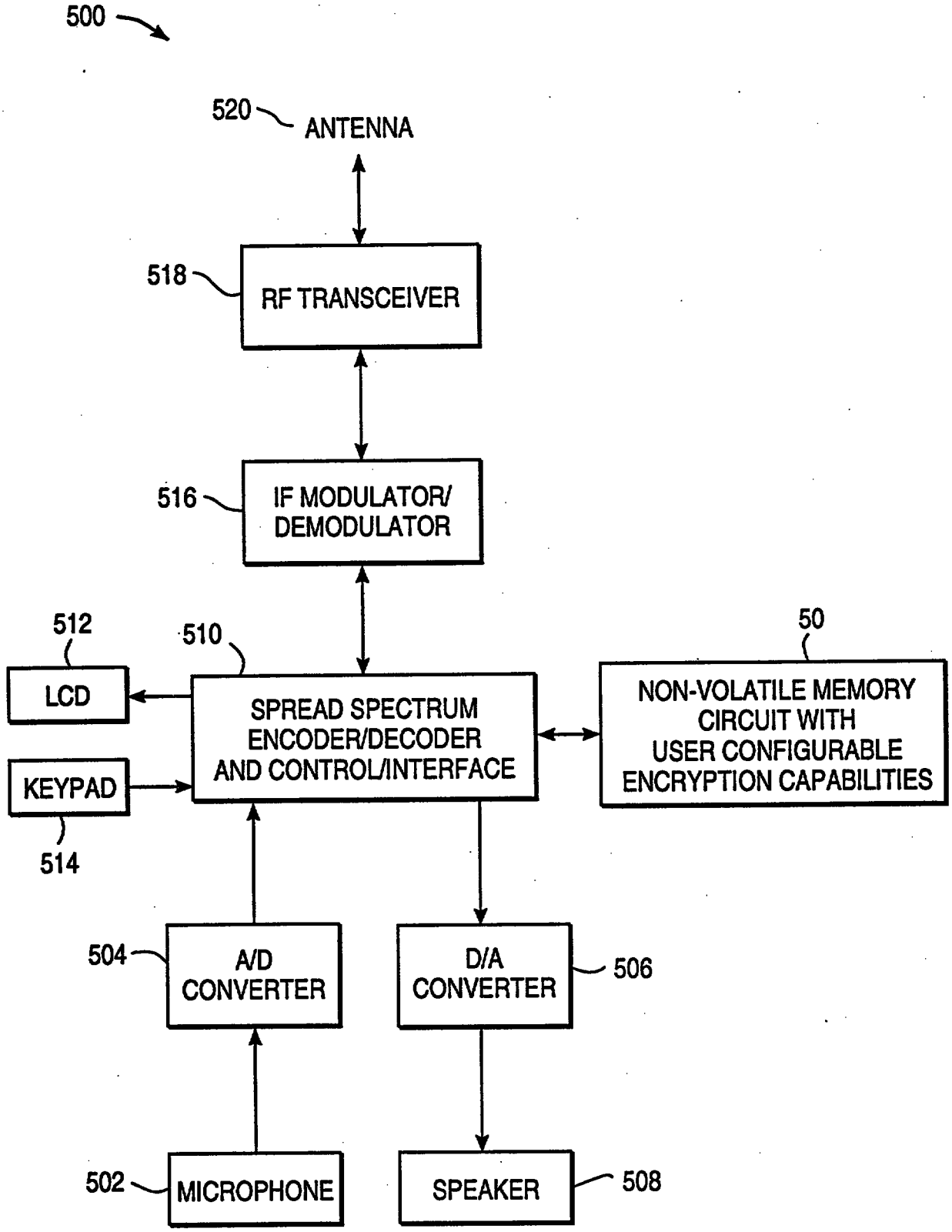


FIG. 5

This is the replacement sheet

08 SEP 1997

Date:

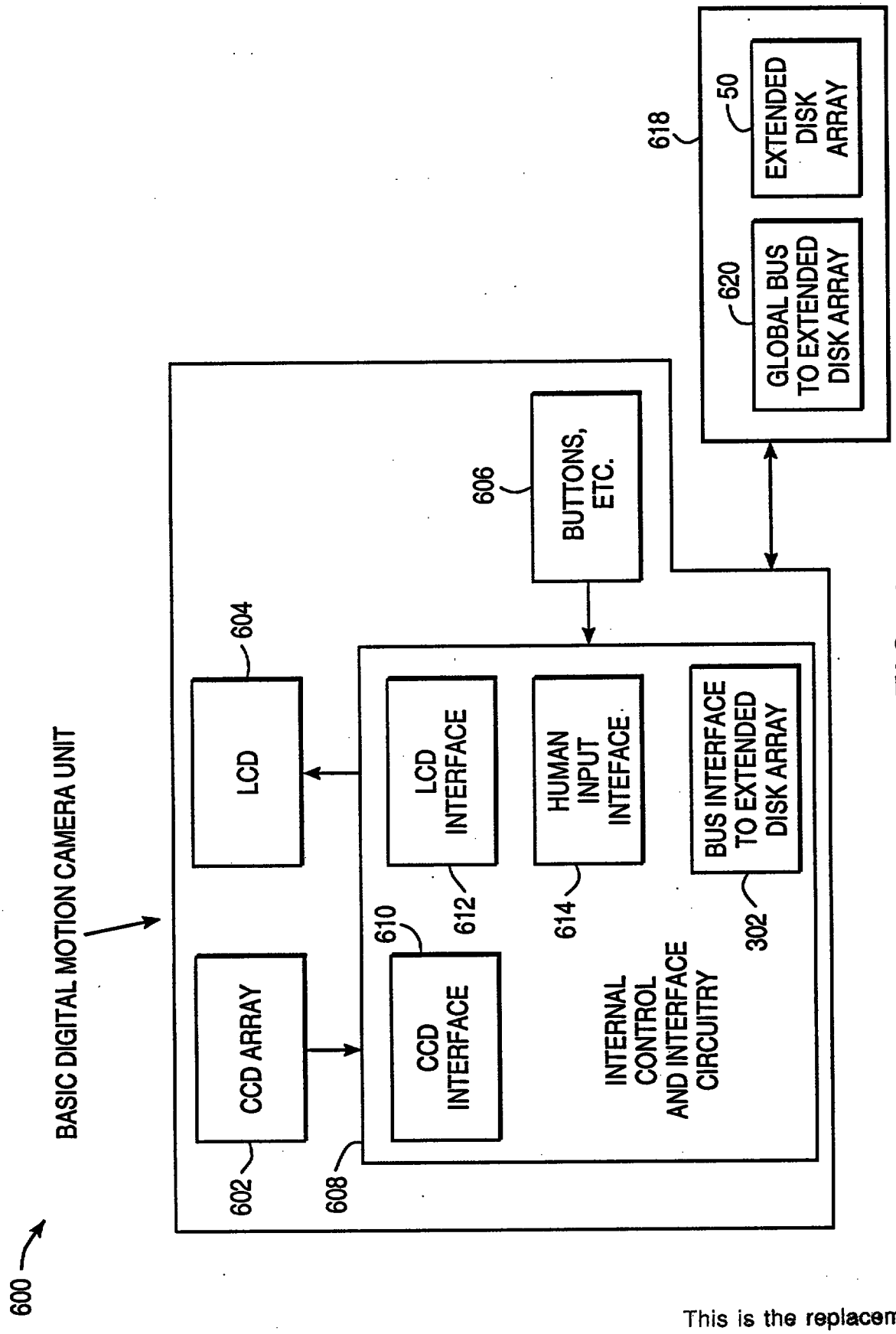


FIG. 6

This is the replacement sheet

Date: 08 SEP 1997

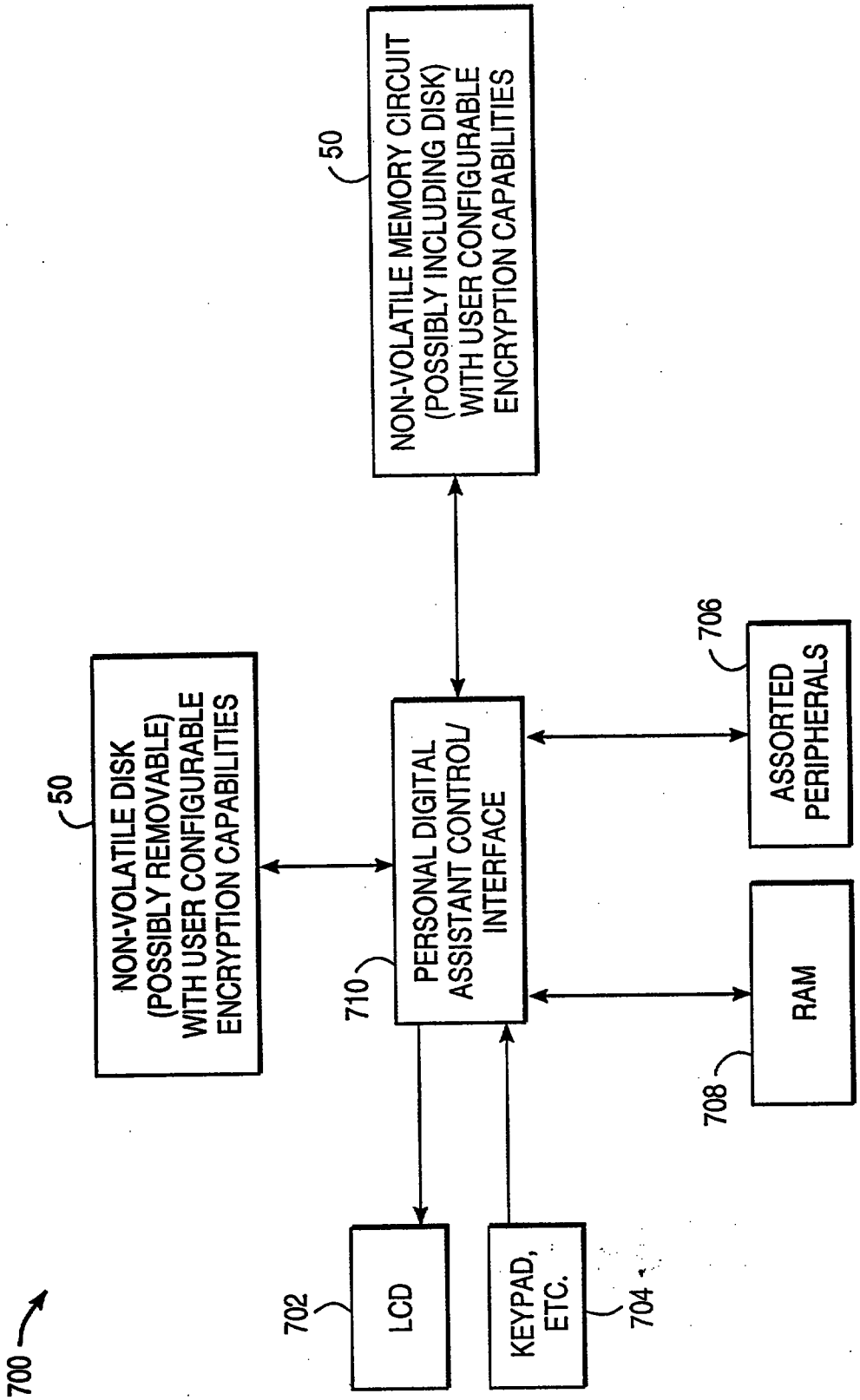


FIG. 7

This is the replacement sheet

Date: 08 SEP 1997