

Description

Background of the Invention

This invention relates in general to voltage controlled oscillators and relates in particular to a voltage controlled ring oscillator that can operate at high frequencies and that can be implemented in a small number of elements formed on a single chip. Voltage controlled oscillators are widely used in communication systems. In Figure 1 is illustrated a conventional ring oscillator. This oscillator consists of an odd number N of inverters, each having a gate delay of T_d . If a rising logic edge propagates around the ring it will, after one round trip, become a falling edge. After two such trips, it will again be a rising edge. Since the time of propagation around the loop is $N \cdot T_d$, the period of this signal will be $2N \cdot T_d$. Equivalently, this circuit oscillates at a frequency of $1/2N \cdot T_d$.

Three conditions are required to ensure that this circuit will function as an oscillator. First, the small signal gain of each inverter must be such that the net gain around the loop is greater than 1. When the net gain is greater than 1, the signal on the loop will grow with each pass around the loop until the inverters saturate to a point such that the total gain of the loop drops to 1. Second, there must be an odd number of inversions around the loop. If there were an even number, then the circuit operation could peg at the maximum positive or negative signal achievable at saturation of all inverters and the circuit would not oscillate. Thus, by requiring a net inversion around the ring, it is assured that such saturation at a constant circuit value will not occur. An alternate means of preventing latchup is to provide for an AC coupling in the ring. This method is usually avoided in monolithic implementations due to the difficulty in fabricating the required coupling capacitors. Third, N is chosen to be greater than two. According to Nyquist's Stability Criterion, the existence of more than two dominant poles in the circuit transfer function guarantees that the circuit will be unstable. Therefore, N is chosen to be greater than two.

In conventional voltage controlled ring oscillators, the frequency is varied by varying the gate delay T_d of each stage. In one such oscillator, an FET is introduced before each inverter. The control voltage is applied to the gate of each of the FETs to vary the delay of each FET, thereby varying the frequency of the oscillator. In another voltage controlled ring oscillator, voltage controlled bias currents are used for each inverter to modify the rise and fall times of the inverters, thereby varying the gate delay T_d of each inverter. Unfortunately, both of these schemes introduce elements that limit the maximum frequency that can be produced by the

oscillator.

For cost reasons, it is always desirable to minimize both the chip count and the number of external parts needed to build a given system. Thus, it would be advantageous to have an oscillator design that utilizes a small number of elements that are compatible so that they can be integrated onto a single chip with other circuits with which the oscillator is to interact without need for external frequency determining elements.

JP-A-56 47125 shows a digitally controllable delay element that is switchable to any of a plurality of discrete delay times.

Electronic Design, Vol. 20, September 26, 1968 page 71 shows a ring oscillator.

Electronics Letters, Vol. 22, June 5, 1986, pages 677 to 679 discloses a plurality of delay elements arranged in a loop and a pair of field effect transistors that receive a control signal from a potentiometer (the potentiometer is discussed in the accompanying text but not shown in the drawing). The FETs' apply varying amounts of feedback from two different points in the loop to control the frequency of oscillation.

US-B-3 996 481 discloses, (in Fig. 3) a plurality of delay elements arranged in series and suggests that the series of delay elements is "looped back" on itself to form a ring oscillator.

US-A-4 434 438 discloses a variable delay circuit comprising delay elements for providing a delayed signal; adjustment amplifiers, the gain of which is controlled by control circuitry; and a summing amplifier for adding together the output signals of said adjustment amplifiers to provide a delayed output signal. The disclosure substantially relates to the delaying of analogue signals, especially video signals.

U-S-A 3 293 552 also discloses a variable delay circuit in which delayed signals are provided by delay elements. The delayed signals are provided for a plurality of different frequency ranges. The circuit comprises adjustment means for each of said plurality of frequency ranges, the gain of which adjustment means is controlled by control circuitry; and a summing amplifier for adding together the output signals of said adjustment means to provide a delayed output signal.

IBM Technical Disclosure Bulletin, Vol. 25, No. 69, February 1983, pages 4493 to 4495 discloses a voltage-controlled ring oscillator comprising a plurality of inverters and delay elements and a combination element including a linear combiner for combining two input signals, the combination element and a first plurality of the inverters and delay elements configured in a first feedback loop having an odd number of signal inversions and a first loop oscillation frequency, said combination element and a second plurality of the inverters and delay

elements configured in a second feedback loop also having an odd number of signal inversions and a second loop oscillation frequency, the linear combiner being responsive to a control signal.

The switching is digital and therefore is discrete.

Accordingly, the present invention provides a voltage-controlled ring oscillator comprising a plurality of inverters and delay elements and a combination element including a linear combiner for combining two input signals, the combination element and a first plurality of the inverters and delay elements operatively configured in a first feedback loop having an odd number of signal inversions and a first loop oscillation frequency, said combination element and a second plurality of the inverters and delay elements operatively configured in a second feedback loop also having an odd number of signal inversions and a second loop oscillation frequency, the linear combiner being responsive to a control signal, characterised in that the control signal continuously varies the gains of the feedback loops such that any increase in the gain of the one loop is accompanied by a corresponding decrease in the gain of the other, so as to continuously tune the oscillator to any desired frequency between the first and second loop frequencies.

The delay circuit is continuously variable by an analogue control voltage.

In the Figures, the first digit of a 1,2 or 3 digit reference numeral and the first two digits of a 4 digit reference numeral will indicate the first figure in which that element appear.

In accordance with the illustrated preferred embodiment of the invention, a ring oscillator is presented that utilizes an inverter/combination circuit to introduce a voltage controllable delay into the ring. This inverter/combination circuit produces from an input signal a second signal which is delayed by a fixed amount of delay. A linear combination of this delayed signal and the input signal is produced, the amount of each of the two signals being determined by an applied control voltage. For an input sine wave, the resulting output signal from this inverter/combination circuit is shifted in phase by 180 degrees and is delayed by an amount that is determined by the applied control voltage. This variable controllable delay plus a fixed delay from other elements in the loop determine the period of oscillation of the oscillator. This enables the frequency of oscillation of the oscillator to be varied by an applied control voltage.

When this circuit is inserted into a ring, there results a configuration consisting of two loops. In one limit of operation, the signal in the ring travels around only a first of these loops, referred to as the low frequency loop, and the resulting oscillator frequency is the minimum producible by this os-

cillator. In the other limit of operation, the signal in the ring travels around only the other of these loops, referred to as the high frequency loop, and the resulting oscillator frequency is the maximum producible by this oscillator. The oscillator frequency varies monotonically between these two frequency extremes as a function of the applied control voltage.

In order to have stable operation of this inverter/combination circuit, the maximum allowable delay produced by this inverter/combination circuit is limited to $1/2f$. In order to achieve an increased range of frequency tunability, a plurality of these delay elements are utilized in the oscillator. In one embodiment, a plurality of these inverter/combination elements are coupled in series in a ring. In another embodiment having a larger maximum oscillator frequency, these inverter/combination circuits are combined in a cascade type of arrangement.

Description of the Figures

Figure 1 illustrates a conventional ring oscillator.

Figure 2 illustrates the general form of the inverter/combination circuit in a voltage controlled ring oscillator.

Figure 3 illustrates the amount of variable delay produced in the output signal of the inverter/combination as a function of a control parameter C that is determined by an applied control voltage.

Figure 4 is a simplified block diagram of the circuit of figure 2 with the elements within dashed lines 25 in Figure 2 represented as inverting variable delay element 25 in Figure 4.

Figure 5 is a block diagram of a ring oscillator having three inverters in its high frequency loop and 5 inverters in its low frequency loop.

Figure 6 illustrates a ring oscillator in which the high frequency loop utilizes an even number of differential inverters.

Figure 7 illustrates the reduction in the amplitude of the output signal V_z of the inverter/combination circuit that can result if the relative phase between V_x and V_y is allowed to approach π .

Figure 8 illustrates the responsiveness of the inverter/combination circuit to changes in control parameter C when the phase between V_x and V_y is π .

Figure 9 is a block diagram of a ring oscillator utilizing a plurality of inverter/combination circuits connected in series in a loop to achieve a stable oscillator having an extended frequency tuning range.

Figure 10 is a block diagram of a ring oscillator utilizing a plurality of inverter/combination circuits connected in a cascade arrangement that not only achieves stable oscillation over an extended range of frequency, but also maintains a high maximum frequency of operation.

Figure 11 presents a particular embodiment of the circuit of Figure 10 to illustrate how the inverter/combination circuits function at values of $C = 0$, $1/2$ and 1 to determine the oscillator frequency.

Figure 12 is an embodiment of the inverter/combination cell and the inverter in bipolar circuitry.

Figure 13 is an embodiment of a ring oscillator utilizing FETs.

Description of the Preferred Embodiment

In Figure 2 is shown a block diagram illustrating the operation of this new oscillator. This circuit contains an inverter/combination circuit 21 and three delay elements 22, 23 and 24 which introduce delays of d_1 , d_2 , and d_3 , respectively. Delay element 23 produces a signal V_y at a first input of inverter/combination circuit 21 and delay element 24 produces a signal V_x at a second input of inverter/combination circuit 21. The output signal V_z of inverter/combination circuit 21 is equal to the linear combination $-[C(V_C)V_x + D(V_C)V_y]$ where C and D are functions of an applied control voltage V_C . In order to achieve monotonic tuning of this oscillator with applied control voltage V_C , the functions C and D should be monotonic in V_C . In order for the amplitude of V_z to be substantially constant, it is advantageous for $C + D$ to be fairly constant. For the embodiments shown in Figures 13 and 14, $C + D$ is substantially constant at a value of 1 . Thus, D can be replaced by $(1-C)$ so that this linear combination becomes $-[C^*V_x + (1-C)^*V_y]$ where C is in the range $0 \leq C \leq 1$. The value of C is determined by a control voltage V_C applied to a control input of inverter/combination circuit 21 and is used to vary the frequency of oscillation of this oscillator.

The relative delay $d_3 - d_2$ produces a relative phase shift $P = 2\pi f^*D = w^*(d_3 - d_2)$ of signal V_x relative to signal V_y , where f is the frequency of the oscillator and w is the angular frequency of the oscillator. The relationship between the output signal V_z of inverter/combination circuit 21 and its input signals V_x and V_y can be seen by reference to the phasor diagram in Figure 3. Phase shift P shows up in this phasor diagram as the angle P between V_x and V_y and angle Q shows up as the angle Q between V_z and V_y . As C varies from 0 to 1 , phase shift Q varies from 0 to P .

This phase shift Q is equivalent to an effective delay of $Q/2\pi f$ of V_z relative to V_y . Therefore, the

circuit within dashed line 25 is an inverting variable delay (IVD) element which introduces a phase shift of π and a delay D which varies from d_2 for $C = 0$ to d_3 for $C = 1$. Thus, the circuit in Figure 3 is equivalent to the circuit shown in Figure 4. Therefore, the frequency of this oscillator is $1/2(d_1 + D)$ and is tunable over the range from $1/(d_1 + d_2)$ to $1/(d_1 + d_3)$. In particular embodiments, any one of the delay elements can be eliminated. Likewise, inverter/combination circuit 21 can be replaced by a combination circuit, that produces a linear combination $V_z = C^*V_x + (1-C)^*V_y$, plus either an inverter somewhere in path ABC or an inverter in each of paths CDE and CFG.

In Figure 5 is illustrated an embodiment of the oscillator utilizing a combination circuit 51 and 5 inverters 52-56. Loop ABCGA contains 5 inverters and loop ABCEA contains 3 inverters. Thus, both of these loops contain the required odd number of inversions to serve as a ring oscillator. Inverters 52, 53 and 54 produce the delay d_1 . Inverters 54 and 55 produce the delay d_3 . The delay d_2 is substantially zero in this embodiment.

When the control voltage sets combination parameter C equal to 0 , all of the signal circulates in loop ABCEA. This loop is referred to as the high frequency loop because it contains only 3 inverters and therefore for $C = 1$ the period of the signal is equal to three times the gate delay of each of these inverters. Thus, for $C = 0$, the frequency is equal to $1/6T_d$.

When the control voltage sets combination parameter C equal to 1 , all of the signal circulates in loop ABCGA. This loop is referred to as the low frequency loop because it contains 5 inverters and therefore, for $C = 1$, the frequency is equal to $1/10T_d$. Because the phase delay between points C and A varies monotonically from 0 to $2T_d$ as C varies from 0 to 1 , the frequency varies monotonically from $1/6T_d$ to $1/10T_d$ as C varies from 0 to 1 . Thus, this embodiment has a $5:3$ ratio in the maximum and minimum frequencies generated by this oscillator. This oscillator is referred to as a $3/5$ oscillator.

As discussed above, in order to avoid the oscillator failing to oscillate because its signal pegs at the positive or negative extremes of amplifier operation, both the low frequency and high frequency loops must have a net inversion. However, such inversion does not necessarily require an odd number of inverters in both loops. In Figure 6 is illustrated an embodiment utilizing differential inverters in which an even number of inverters is utilized in both loops. To achieve the net inversion, the wires are crossed over as shown between inverters 62 and 63 but are not crossed over between the other elements. However, in other embodiments, the crossover could occur between combination circuit

61 and inverter 62 or between inverter 63 and node C. Similarly, it is not necessary that a pair of inverters be used in path CG. This pair of inverters can be replaced by an amplifier that provides the amplification and delay otherwise produced by inverters 64 and 65 or, in Figure 5, produced by inverters 55 and 56.

The output signal can be tapped from this circuit at any point in the connections between elements 21-24. In the embodiment illustrated in Figure 2, the signal V_z is selected to be the output signal. However, the choice of output point can assist in increasing the maximum frequency attainable by this oscillator. In order to make this maximum frequency as large as possible for a given arrangement of inverters, the amount of loading of the high speed loop ABCEA should be minimized. Thus, in the embodiment in Figure 5, the output voltage is tapped from the output of inverter 56. As a result of this, the signal at point C is amplified by passing through inverters 55 and 56 before it is tapped at point G. This results in less loading of the high speed loop ABCEA than if the output signal were tapped at point A as in Figure 2. An amplifier 57 is included in the output path to boost the amplitude of the output signal V_{out} . This choice also loads the low frequency loop more heavily so that the low frequency end is reduced, thereby somewhat increasing the tuning range.

It should be noted that, in Figure 3, the angle P between V_y and V_x varies with C . This variation occurs because P equals $2\pi f^*(d_3-d_2)$ and f varies with C . As illustrated in Figure 6, as C decreases toward zero, the frequency increases toward the maximum frequency of the oscillator. In Figure 7 is illustrated the situation that will result if P approaches π for some value of C near $1/2$. In this situation, the amplitude of V_z becomes small enough that there may not be sufficient gain in other elements in the ring oscillator to achieve a net gain of at least 1, as is required to achieve and maintain oscillation. In this situation, when the amplitude of V_z becomes too small, the circuit oscillation will cease.

If p approaches π when C is nearer to 0 or 1 than it is to $1/2$, then this significant decrease in amplitude of V_z may not occur. However, even in this case oscillator stability problems will arise. As is illustrated in Figure 8, when there is a phase difference of π between V_x and V_y , then these two vectors will be collinear so that they no longer form a basis for the complex phasor plane. Once this point is reached, as C is further varied, V_z will tend to stay collinear with vector V_y . Therefore, as C is varied further, the amplitude of V_z will change, but the phase difference Q between V_z and V_y will not change. However, as C is varied through $C = 1/2$, the amplitude of V_z is forced to be zero so that the

oscillator will cease to oscillate. Thus, in general, the inverter/combination circuit should be selected so that P is less than π throughout the operating range of the oscillator. This requires that the number of inverters in the low frequency loop be less than twice the number of inverters in the high frequency loop. Unfortunately, this limits the range of tuning to less than an octave.

A ring oscillator that is turnable over more than one octave without becoming unstable can be produced by utilizing a plurality of inverter/combination circuits. In Figure 9 is illustrated one embodiment in which three inverting variable delay (IVD) elements of Figure 2 are connected in series in a ring to form a ring oscillator having a frequency range greater than one octave without being unstable. For the particular case in which element 23 is omitted from the inverting variable delay element 25, in which delay element 24 is a pair of inverters, and in which inverter/combination element consists of a combination element in series with an inverter, this inverting variable delay element introduces a delay that can vary from T_d to $3T_d$. When $C = 0$, the signal passes through three inverters so that the high frequency loop has a delay of $3T_d$. When $C = 1$, the signal passes through nine inverters so that the low frequency loop has a delay of $9T_d$. Thus, this circuit exhibits a tuning range of 3:1, which compares to the tuning range of 5:3 of the oscillator of Figure 5.

In Figure 10 is shown an oscillator in which two inverter/combination elements are cascaded in a combination with some inverters to achieve an increased tuning range. This oscillator is achieved by replacing the constant delay produced by elements 55 and 56 in Figure 5 with a noninverting variable delay block of elements identical to elements 52, 54, 55, 56 and 51 of Figure 5. This circuit consists of a pair of combination circuits 1001 and 1002 plus a set of seven inverters 1003 - 1009.

That this circuit provides an extended frequency tuning range can be seen as follows. When $C = 1$, combination circuits 1001 and 1002 are unresponsive to their x inputs. Therefore, the oscillator signal travels only around the loop consisting of elements 1001 and 1003 - 1005. This is the high frequency loop and contains three inverters so that the maximum frequency is $1/6T_d$. When $C = 0$, combination circuits 1001 and 1002 are unresponsive to their y inputs so that the oscillator signal travels around the low frequency loop consisting of elements 1001, 1003-1008, 1002, and 1009 in series. This low frequency loop contains all seven inverters so that the minimum frequency of this oscillator is $1/14T_d$. Therefore, there is a 7:3 tuning range of this oscillator. In order to illustrate that for intermediate values of C that intermediate frequencies will be produced, the following simple analysis

will show that for $C = 1/2$ that the loop delay is $4.5 T_d$ so that the frequency is $1/9T_d$ which is in the middle of the tuning range. When $C = 1/2$, both inverters produce an equal mix of their input signals so that each has an output signal having a phase midway between the phases of its input signals. Starting at the upper right corner of this circuit as zero reference phase, to reach the output of each of inverters 1004-1008, the signal must pass through each of the preceding inverters in that path. Therefore, the phase delay at the output of each of these 5 inverters is 1, 2, 3, 4, and 5 times T_d respectively. Since combination circuits 1001 and 1002 each produces at its output an equal mix of its two inputs, its output phase is the average of the phases of its two input signals. Therefore the delay at the output of combination element 1002 is 4, which means that the delay at the x input of combination circuit 1001 is 5. This delay on its x input and the delay of $2T_d$ on its y input means that the delay at the output of combination circuit 1001 is equal to 3.5. Therefore, the total delay is $4.5 T_d$.

The general structure of this extended tuning range oscillator is shown in Figure 11. This circuit has N cascaded stages. The first stage contains a combination circuit 1111, an inverter 1112 and a gain delay element 1113 that provides both gain and delay of the signal through it. In the kth stage, for $k = 2, \dots, N$ for some integer N, there is a combination circuit 11k1, and a pair of gain/delay elements 11k2 and 11k3. There is also an additional gain/delay element 11N4. In the embodiment shown in Figure 10, each of the gain delay elements is an inverter. In general, for $k = 2 - N-1$, elements 11k2 and 11k3 are required to be either both inverting or are both noninverting. Element 11N4 is always noninverting. The delay for each of elements 11k3 can be freely chosen by the designer, but in general it will be advantageous to have increasing delay with increasing k. The gain and delay from elements 11k2 for $k = 2, \dots, N-1$ will in general be caused by the gain and delay that arise from real nonidealized combination circuits 11k1.

Actual embodiments of ring oscillators in accordance with this invention are shown in Figures 12 and 13. In Figure 12, the inverter/combination cell and the inverter are implemented with bipolar elements. In Figure 13, the oscillator is implemented using field effect transistors.

Claims

1. A voltage-controlled ring oscillator comprising a plurality of inverters and delay elements (52-56) and a combination element (51) including a linear combiner (1201) for combining two input

signals, the combination element and a first plurality of the inverters and delay elements (52-54) operatively configured in a first feedback loop having an odd number of signal inversions and a first loop oscillation frequency, said combination element and a second plurality of the inverters and delay elements (52-56) operatively configured in a second feedback loop also having an odd number of signal inversions and a second loop oscillation frequency, the linear combiner being responsive to a control signal (V_c), characterised in that the control signal continuously varies the gains of the feedback loops such that any increase in the gain of the one loop is accompanied by a corresponding decrease in the gain of the other, so as to continuously tune the oscillator to any desired frequency between the first and second loop frequencies.

2. An oscillator as in claim 1, wherein the combination element comprises a first controllable-gain amplifier (1202) responsive to the linear combiner (1201) to amplify a signal in the first feedback loop according to the control signal and a second controllable-gain amplifier (1203) responsive to the linear combiner to amplify a signal in the second feedback loop according to the control signal, any change in the second control signal that increases the gain of one of the controllable-gain amplifiers being effective to correspondingly reduce the gain of the other.
3. An oscillator as in claim 2, wherein the linear combiner (1201) comprises first and second resistive elements (1204, 1205) and first and second current controllers (1206, 1207) responsive to the control signal to provide operating current to the first and second controllable-gain amplifiers (1202, 1203) through the first and second resistive elements, respectively.
4. An oscillator as in any preceding claim wherein the combination element comprises an inverter/combination unit (21) and the delay elements comprise a first delay unit (23) in a separate section of the first feedback loop, a second delay unit (24) in a separate section of the second feedback loop, and a common delay unit (22) in a common section of both feedback loops, the first delay unit having a time delay of zero or more and the second delay unit having a time delay greater than that of the first, the inverter/combination unit and the first and second delay units together defining an inverting variable delay element (25).



will show that for $C = 1/2$ that the loop delay is $4.5 T_d$ so that the frequency is $1/9T_d$ which is in the middle of the tuning range. When $C = 1/2$, both inverters produce an equal mix of their input signals so that each has an output signal having a phase midway between the phases of its input signals. Starting at the upper right corner of this circuit as zero reference phase, to reach the output of each of inverters 1004-1008, the signal must pass through each of the preceding inverters in that path. Therefore, the phase delay at the output of each of these 5 inverters is 1, 2, 3, 4, and 5 times T_d respectively. Since combination circuits 1001 and 1002 each produces at its output an equal mix of its two inputs, its output phase is the average of the phases of its two input signals. Therefore the delay at the output of combination element 1002 is 4, which means that the delay at the x input of combination circuit 1001 is 5. This delay on its x input and the delay of $2T_d$ on its y input means that the delay at the output of combination circuit 1001 is equal to $3.5 T_d$. Therefore, the total delay is $4.5 T_d$.

The general structure of this extended tuning range oscillator is shown in Figure 11. This circuit has N cascaded stages. The first stage contains a combination circuit 1111, an inverter 1112 and a gain delay element 1113 that provides both gain and delay of the signal through it. In the kth stage, for $k = 2, \dots, N$ for some integer N, there is a combination circuit 11k1, and a pair of gain/delay elements 11k2 and 11k3. There is also an additional gain/delay element 11N4. In the embodiment shown in Figure 10, each of the gain delay elements is an inverter. In general, for $k = 2 - N-1$, elements 11k2 and 11k3 are required to be either both inverting or are both noninverting. Element 11N4 is always noninverting. The delay for each of elements 11k3 can be freely chosen by the designer, but in general it will be advantageous to have increasing delay with increasing k. The gain and delay from elements 11k2 for $k = 2, \dots, N-1$ will in general be caused by the gain and delay that arise from real nonidealized combination circuits 11k1.

Actual embodiments of ring oscillators in accordance with this invention are shown in Figures 12 and 13. In Figure 12, the inverter/combination cell and the inverter are implemented with bipolar elements. In Figure 13, the oscillator is implemented using field effect transistors.

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signals, the combination element and a first plurality of the inverters and delay elements (52-54) operatively configured in a first feedback loop having an odd number of signal inversions and a first loop oscillation frequency, said combination element and a second plurality of the inverters and delay elements (52-56) operatively configured in a second feedback loop also having an odd number of signal inversions and a second loop oscillation frequency, the linear combiner being responsive to a control signal (V_c), characterised in that the control signal continuously varies the gains of the feedback loops such that any increase in the gain of the one loop is accompanied by a corresponding decrease in the gain of the other, so as to continuously tune the oscillator to any desired frequency between the first and second loop frequencies.

2. An oscillator as in claim 1, wherein the combination element comprises a first controllable-gain amplifier (1202) responsive to the linear combiner (1201) to amplify a signal in the first feedback loop according to the control signal and a second controllable-gain amplifier (1203) responsive to the linear combiner to amplify a signal in the second feedback loop according to the control signal, any change in the second control signal that increases the gain of one of the controllable-gain amplifiers being effective to correspondingly reduce the gain of the other.
3. An oscillator as in claim 2, wherein the linear combiner (1201) comprises first and second resistive elements (1204, 1205) and first and second current controllers (1206, 1207) responsive to the control signal to provide operating current to the first and second controllable-gain amplifiers (1202, 1203) through the first and second resistive elements, respectively.
4. An oscillator as in any preceding claim wherein the combination element comprises an inverter/combination unit (21) and the delay elements comprise a first delay unit (23) in a separate section of the first feedback loop, a second delay unit (24) in a separate section of the second feedback loop, and a common delay unit (22) in a common section of both feedback loops, the first delay unit having a time delay of zero or more and the second delay unit having a time delay greater than that of the first, the inverter/combination unit and the first and second delay units together defining an inverting variable delay element (25).



5. A voltage-controlled ring oscillator according to claim 4 comprising a plurality of said inverting variable delay elements (91, 92, 93) configured in a serial cascade, the oscillator being tunable through a frequency range of more than 2:1.

6. A voltage-controlled ring oscillator according to any of claims 1 to 3 comprising a plurality of said combination elements (1001, 1002; 11k1) and a plurality of delay elements (1003-1008; 11k2, 11k3) configured in parallel cascade, the oscillator being tunable through a frequency range of more than 2:1.

Patentansprüche

1. Spannungsgesteuerter Ringoszillator mit mehreren Invertern und Verzögerungselementen (52 - 56) und einem Kombinationselement (51), das einen linearen Kombinator (1201) zum Kombinieren von zwei Eingangssignalen aufweist, wobei das Kombinationselement und eine erste Mehrzahl der Inverter und Verzögerungselemente (52 - 54) in einer ersten Rückführungsschleife funktionsmäßig zusammengestellt sind, die eine ungerade Anzahl von Signalinversionen aufweist und eine erste Schleifen-Schwingungsfrequenz hat, wobei das Kombinationselement und eine zweite Mehrzahl der Inverter und Verzögerungselemente (52 - 56) in einer zweiten Rückführungsschleife funktionsmäßig zusammengestellt sind, die ebenfalls eine ungerade Anzahl von Signalinversionen aufweist und eine zweite Schleifen-Schwingungsfrequenz hat, und wobei der lineare Kombinator auf ein Steuersignal (V_C) anspricht, dadurch gekennzeichnet, daß das Steuersignal die Verstärkungsfaktoren der Rückführungsschleife kontinuierlich verändert, so daß jede Zunahme des Verstärkungsfaktors der einen Schleife von einer entsprechenden Abnahme des Verstärkungsfaktors der anderen Schleife begleitet wird, um den Oszillator kontinuierlich auf eine gewünschte Frequenz zwischen der ersten und der zweiten Schleifenfrequenz abzustimmen.

2. Oszillator nach Anspruch 1, bei dem das Kombinationselement einen ersten Verstärker (1202) mit steuerbarem Verstärkungsfaktor aufweist, der auf den linearen Kombinator (1201) anspricht, um ein Signal der ersten Rückführungsschleife nach Maßgabe des Steuersignales zu verstärken, und einen zweiten Verstärker (1203) mit steuerbarem Verstärkungsfaktor aufweist, der auf den linearen Kombinator anspricht, um ein Signal in der zweiten Rückführungsschleife nach Maßgabe des Steuersignales zu verstärken, wobei jede Veränderung des zweiten Steuersignales, die den Verstärkungsfaktor eines der Verstärker mit steuerbarem Verstärkungsfaktor erhöht, den Verstärkungsfaktor des anderen entsprechend vermindert.

3. Oszillator nach Anspruch 2, bei dem der lineare Kombinator (1201) ein erstes und ein zweites Widerstandselement (1204, 1205) und eine erste und eine zweite Stromsteuervorrichtung (1206, 1207) aufweist, die auf das Steuersignal ansprechen, um Betriebsströme für den ersten und den zweiten Verstärker (1202, 1203) mit steuerbarem Verstärkungsfaktor über das erste bzw. das zweite Widerstandselement vorzusehen.

4. Oszillator nach einem der vorangehenden Ansprüche, bei dem das Kombinationselement eine Inverter/Kombinations-Einheit (21) aufweist und die Verzögerungselemente eine erste Verzögerungseinheit (23) in einem gesonderten Bereich der ersten Rückführungsschleife, eine zweite Verzögerungseinheit (24) in einem gesonderten Bereich der zweiten Rückführungsschleife und eine gemeinsame Verzögerungseinheit (22) in einem gemeinsamen Bereich beider Rückführungsschleifen aufweisen, wobei die erste Verzögerungseinheit eine Zeitverzögerung von Null oder größer aufweist und die zweite Verzögerungseinheit eine Zeitverzögerung größer als die der ersten aufweist, und wobei die Inverter/Kombinations-Einheit und die erste und die zweite Verzögerungseinheit gemeinsam ein invertierendes variables Verzögerungselement (25) definieren.

5. Spannungsgesteuerter Ringoszillator nach Anspruch 4, mit einer Mehrzahl der invertierenden variablen Verzögerungselemente (91, 92, 93), die in Reihe geschaltet sind, wobei der Oszillator in einem Frequenzbereich von mehr als 2:1 abstimmbar ist.

6. Spannungsgesteuerter Ringoszillator nach einem der Ansprüche 1 bis 3, mit einer Mehrzahl der Kombinationselemente (1001, 1002; 11k1) und einer Mehrzahl der Verzögerungselemente (1003 - 1008; 11k2, 11k3), die parallel geschaltet sind, wobei der Oszillator in einem Frequenzbereich von mehr als 2:1 abstimmbar ist.

Revendications

1. Oscillateur en anneau commandé en tension comprenant une pluralité d'inverseurs et d'éléments de retard (52-56) et un élément de combinaison (51) incluant un combineur linéai-



- re (1201) pour combiner deux signaux d'entrée, l'élément de combinaison et une première pluralité des inverseurs et éléments de retard (52-54) étant configurés de façon opérationnelle selon une première boucle de retour présentant un nombre impair d'inversions de signal et une première fréquence d'oscillation de boucle, ledit élément de combinaison et une seconde pluralité des inverseurs et éléments de retard (52-56) étant configurés de façon opérationnelle selon une seconde boucle de retour présentant également un nombre impair d'inversions de signal et une seconde fréquence d'oscillation de boucle, le combineur linéaire étant sensible à un signal de commande (V_c), caractérisé en ce que le signal de commande fait varier en continu les gains des boucles de retour de telle sorte qu'une quelconque augmentation du gain de la boucle en question soit accompagnée d'une diminution correspondante du gain de l'autre, de manière à accorder en continu l'oscillateur à n'importe quelle fréquence souhaitée entre les première et seconde fréquences de boucles.
2. Oscillateur selon la revendication 1, dans lequel l'élément de combinaison comprend un premier amplificateur à gain commandable (1202) sensible au combineur linéaire (1201) pour amplifier un signal dans la première boucle de retour en relation avec le signal de commande et un second amplificateur à gain commandable (1203) sensible au combineur linéaire pour amplifier un signal dans la seconde boucle de retour en relation avec le signal de commande, n'importe quelle variation du second signal de commande qui augmente le gain de l'un des amplificateurs à gain commandable étant efficace pour réduire en correspondance le gain de l'autre.
 3. Oscillateur selon la revendication 2, dans lequel le combineur linéaire (1201) comprend des premier et second éléments résistifs (1204, 1205) et des premier et second contrôleurs de courant (1206, 1207) sensibles au signal de commande pour produire respectivement un courant de fonctionnement pour les premier et second amplificateurs de gain commandable (1202, 1203) par l'intermédiaire des premier et second éléments résistifs.
 4. Amplificateur selon l'une quelconque des revendications précédentes, dans lequel l'élément de combinaison comprend une unité d'inverseur/combinaison (21) et les éléments de retard comprennent une première unité de retard (23) dans une section distincte de la

première boucle de retour, une seconde unité de retard (24) dans une section distincte de la seconde boucle de retour et une unité de retard commune (22) dans une section commune des deux boucles de retour, la première unité de retard présentant un retard temporel de zéro ou plus et la seconde unité de retard présentant un retard temporel supérieur à celui de la première unité de retard, l'unité d'inverseur/combinaison et les première et seconde unités de retard définissant ensemble un élément de retard variable à inversion (25).

5. Oscillateur en anneau commandé en tension selon la revendication 4, comprenant une pluralité desdits éléments de retard variable à inversion (91, 92, 93) configurés en cascade série, l'oscillateur pouvant être accordé sur une plage de fréquence de plus de 2:1.
6. Oscillateur en anneau commandé en tension selon l'une quelconque des revendications 1 à 3, comprenant une pluralité desdits éléments de combinaison (1001, 1002 ; 11k1) et une pluralité d'éléments de retard (1003-1008 ; 11k2, 11k3) configurés en cascade parallèle, l'oscillateur pouvant être accordé sur une plage de fréquence de plus de 2:1.