

than 1 kOhm.cm. The trapping layer can comprise non-doped polycrystalline silicon. The combination of a high-resistivity support substrate and a trapping layer according to the prior art makes it possible to reduce the aforementioned device/substrate coupling, and thus to ensure good performance of the RF devices. In this regard, a person skilled in the art would find a review of the performance of RF devices manufactured on the high-resistivity semiconductor substrate known from the prior art in "Silicon-on-insulator (SOI) Technology, manufacture and applications", points 10.7 and 10.8, Oleg Kononchuk and Bich-Yen Nguyen, Woodhead Publishing.

Furthermore, for the production of RF devices such as, for example, antenna switching units, contained in particular in mobile telephones, it is common to connect a plurality of transistors (for example, field effect transistors "FET") in series so as to maintain the maximum voltage applied to the terminals of the switching unit, said voltage being higher than the breakdown voltage of each individual transistor. However, the serial arrangement of a plurality of transistors has the drawback of increasing the serial resistance of the RF device, which can, in particular, degrade the linearity performance of the RF device.

The present disclosure aims to solve all or part of the aforementioned drawbacks. One particular aim of the disclosure is to propose a structure for RF use which may allow the production of RF devices with enhanced performance.

BRIEF DESCRIPTION OF THE DISCLOSURE

An aspect of the present disclosure relates to a structure for RF use comprising:

- a high-resistivity support substrate, of which a front surface defines a main plane,
- a charge trapping layer arranged on the front surface of the support substrate,
- a first dielectric layer arranged on the trapping layer,
- an active layer arranged on the first dielectric layer.

The structure is characterised in that it comprises at least one buried electrode arranged above or inside the trapping layer, the electrode comprising a conductive layer and a second dielectric layer.

According to other advantageous and non-restrictive characteristics of the disclosure, taken either separately or in any technically feasible combination:

- the conductive layer has two surfaces according to the main plane: one surface in contact with the first dielectric layer and another surface in contact with the second dielectric layer;
- the electrode comprises a plurality of insulating walls extending between the first and second dielectric layers and segmenting the conductive layer into a plurality of conductive blocks, said blocks being insulated from one another by the insulating walls;
- the electrode is arranged between the active layer and the first dielectric layer, the second dielectric layer being in contact with the active layer, according to the main plane;
- the electrode is arranged between the first dielectric layer and the charge trapping layer, the second dielectric layer being in contact with the trapping layer, according to the main plane;
- the buried electrode is discontinuous in the main plane and a plurality of charge trapping areas extend between the first dielectric layer and the charge trapping layer,

CLAIMS

1. Structure for RF use comprising:

- a high-resistivity support substrate, of which a front surface defines a main plane,
- a charge trapping layer arranged on the front surface of the support substrate,
- a first dielectric layer arranged on the trapping layer,
- an active layer arranged on the first dielectric layer,

the structure being characterised in that it comprises at least one buried electrode arranged above or inside the trapping layer, the electrode comprising a conductive layer and a second dielectric layer.

2. Structure for RF use according to the preceding claim, wherein the conductive layer has two surfaces according to the main plane: one surface in contact with the first dielectric layer and another surface in contact with the second dielectric layer.

3. Structure for RF use according to the preceding claim, wherein the electrode comprises a plurality of insulating walls extending between the first and second dielectric layers and segmenting the conductive layer into a plurality of conductive blocks, said blocks being insulated from one another by the insulating walls.

4. Structure for RF use according to any of the three preceding claims, wherein the electrode is arranged

between the active layer and the first dielectric layer, the second dielectric layer being in contact with the active layer, according to the main plane.

- 5 5. Structure for RF use according to any claim 1 to 3, wherein the electrode is arranged between the first dielectric layer and the charge trapping layer, the second dielectric layer being in contact with the trapping layer, according to the main plane.
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6. Structure for RF use according to the preceding claim taken in combination with claim 3, wherein the electrode is discontinuous in the main plane and a plurality of charge trapping areas extend between the first dielectric layer and the charge trapping layer, the trapping areas being insulated from the conductive blocks by the insulating walls.
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7. Structure for RF use according to any claim 1 and 2, wherein the electrode is arranged in the charge trapping layer, the second dielectric layer being in contact with the front surface of the support substrate according to the main plane, and wherein the electrode comprises a plurality of insulating walls extending between the first and second dielectric layers and defining a plurality of conductive blocks of the conductive layer, each conductive block being insulated from at least one trapping area forming the trapping layer, by the insulating walls.
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8. Structure for RF use according to any claim 3 or 7, wherein at least one conductive block is

electrically connected to a contact pad arranged on a free surface of the active layer, by a conductive via passing through a portion of the structure from the conductive block to the contact pad.

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9. Structure for RF use according to the preceding claim, also comprising a device in and/or on the active layer, including at least one transistor of which a gate electrode arranged on the free surface of the active layer is placed opposite at least one conductive block of the buried electrode.

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10. Structure for RF use according to any preceding claim, wherein the second dielectric layer has a thickness of 5 nm to 100 nm.

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11. Structure for RF use according to any preceding claim, wherein the conductive layer comprises a material selected among monocrystalline silicon, polycrystalline silicon and amorphous silicon.

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12. Structure for RF use according to any preceding claim, wherein the conductive layer has a thickness of 50 nm to 500 nm.

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13. Structure for RF use according to any preceding claim, wherein the conductive layer has a resistivity of several ohms.cm to several thousand ohms.cm.

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