What is claimed is:

1. A semiconductor device, comprising:

a first contact structure;

a second contact structure;

a first bit line structure disposed between the first contact structure and the second contact structure;

a first air spacer interposed between the first contact structure and the first bit line structure;

a first separation space connected to an air entrance of the first air spacer and interposed between the first contact structure and the first bit line structure;

a cover insulating pattern with a gap portion interposed between the first contact structure and the second contact structure, wherein the gap portion has a downwardly-decreasing width; and

an air capping pattern covering the cover insulating pattern to seal the first separation space.

2. The semiconductor device of claim 1,

wherein the air capping pattern includes a tail portion protruding into the first separation space.

3. The semiconductor device of claim 2,

wherein the tail portion of the air capping pattern has a thickness smaller than a width of the air entrance of the first air spacer.

4. The semiconductor device of claim 2 or claim 3,

wherein the gap portion has a minimum width less than a width of the air entrance of the first air spacer.

5. The semiconductor device of any one of claims 1 to 4,

wherein the first separation space protrudes into the cover insulating pattern so that the air capping pattern has a concave surface covering the gap portion of the cover insulating pattern.

6. The semiconductor device of any one of claims 1 to 5,

wherein the first separation space is in contact with a sidewall of the first contact structure and a sidewall of the first bit line structure.

7. The semiconductor device of any one of claims 1 to 6,

wherein the cover insulating pattern is formed of a first nitride layer.

wherein the air capping pattern is formed of a second nitride layer.

8. The semiconductor device of claim 7,

wherein the first nitride layer includes silicon nitride (SiN).

wherein the second nitride layer includes silicon carbon nitride (SiCN).

9. The semiconductor device of claim 7,

wherein the first nitride layer includes SiN having a first film density, and

wherein the second nitride layer includes SiN having a second film density smaller than the first film density.

10. The semiconductor device of any one of claims 1 to 9, further comprising:

an insulating spacer disposed between the first air spacer and a lower portion of the first contact structure and between the first air spacer and a lower portion of the first bit line structure.

11. The semiconductor device of claim 10,

wherein the cover insulating pattern is separated from the insulating spacer by the first separation space.

12. The semiconductor device of claim 10 or claim 11,

wherein the insulating spacer include an oxide layer or a nitride layer.

13. The semiconductor device of any one of claims 1 to 12, further comprising:

a second air spacer interposed between the first bit line structure and the second contact structure,

wherein the second air spacer is connected to the first air spacer.

14. The semiconductor device of claim 13,

wherein the second air spacer is shorter than the first air spacer.

15. A semiconductor device, comprising:

a first contact structure;

a second contact structure;

a first bit line structure disposed between the first contact structure and the second contact structure;

a first air spacer interposed between the first contact structure and the first bit line structure;

a plug structure interposed between the first contact structure and the second contact structure; and

a first separation space disposed between the first air spacer and the plug structure and connected to the first air spacer,

wherein the first separation space has a width increasing in a direction from the first air spacer to the plug structure; and

wherein the plug structure comprises:

a cover insulating pattern with a gap portion,

wherein the gap portion has a downwardly-decreasing width; and

an air capping pattern covering the cover insulating pattern to seal the gap portion.

16. The semiconductor device of claim 15,

wherein the first separation space is defined by a bottom surface of the plug structure, a sidewall of the first bit line structure, and a curved sidewall of the first contact structure.

17. The semiconductor device of claim 16,

wherein a distance of the curved sidewall of the first contact structure and the sidewall of the first bit line structure increases in a direction from the first air spacer to the plug structure.