Description

The invention relates generally to packaging techniques for integrated circuit devices. More particularly, the invention relates to three dimensional chip packages and packaging techniques which achieve both high volumetric packaging and high cooling efficiency to enhance the performance of a packaged system.

Packaging is increasingly the limiting factor in achieving maximum performance from Very Large Scale Integrated (VLSI) based computer systems. The limitations due to packaging arise from two major physical constraints; the maximum power density that can be cooled and the signal transit delay introduced by the package.

Conventional packages fall into two primary categories; two dimensional packages such as planar based systems and three dimensional packages such as card-on-board packages.

The planar type package is used in high end systems to allow for maximum cooling efficiency. In order to increase circuit density in planer packages (and thereby minimize signal transit delay), semiconductor manufacturers have continued to reduce the size of various integrated circuit elements and interconnections to the point where the limits of current technology are being reached.

In order to increase circuit density and gain other manufacturing advantages, various methods have been explored to interconnect a plurality of integrated circuit chips using horizontal and vertical stacking techniques and three dimensional interconnect modules which increase integrated circuit surface are by factors of 2, 3, 4 or more.

US-A-4 868 712 shows a 3-dimensional chip package comprising a plurality of substrates, each having at least one semiconductor device mounted thereon, means for physically joining said plurality of substrates to form an enclosure, each substrate having at least one electronic contact location for connecting it to another substrate, and means for providing at least one cooling channel within said enclosure into which a coolant may be introduced.

IBM TDB Vol. 27, No. 5, p,2865-2868 discloses a 3-dimensional chip package comprising a plurality of substrates, each having at least one semiconductor device mounted thereon and means for physically joining said plurality of substrates to form an enclosure, each substrate having at least one electronic contact location for connecting it to another substrate.

Further prior art three dimensional packaging schemes are typified by the teachings of Golubic in U.S. Patent No. 4,801,992, by Higgins, III in U.S. Patent No. 4,727,410, and by Brown et al in both U.S. Patent Nos. 4,502,098 and 4,823,233. These three dimensional type packages are used in mid-range systems to gain maximum packaging density and enhance system performance. However, none of these patents or other teachings in the prior art, provide a three dimensional chip package that combines enhanced packaging density with high cooling efficiency.

In fact, the need for cooling efficiency increases as circuit density increases. If not addressed, the lack of proper cooling capacity can have a serious adverse effect on system performance for densely packaged systems.

Accordingly, it would be desirable to have an integrated circuit package which can be efficiently cooled and accommodate high volumetric packaging. The resulting package would be particularly useful in enhancing the system level performance for VLSI computer processors, among other devices.

Thus, the invention as claimed is intended to provide a three dimensional chip package which enhances the performance of a packaged system, by facilitating both high volumetric packaging and high cooling efficiency.

This problem is solved by a chip pachage according to claim 1.

The channels can be sealed by hermetic seals formed from solder and the electrical interconnections between subtrates can be formed by solder filets which electrically interconnect pads on the substrate edges.

The invention features means inherent in the package structure (the channels, means for introducing coolants, etc.) for cooling a system having a very high volumetric power density.

The invention also features a three dimensional packaging scheme which facilitates the laying out of processors and shared memory elements in a symetric manner to allow each processor to have equal access (in terms of physical proximity and signal transit time) to memory.

It is an advantage of the invention to provide a three dimensional chip package and associated packaging techniques which allow for high bandwidth communication between packaged processor and memory elements.

Further, cooling channels are provided for the introduction of a liquid or gaseous coolant to improve cooling efficiency.

Further yet, it is an advantage of the invention to provide a three dimensional chip package and packaging techniques which inherently accommodate a large number of signal and power interconnects between pack-

aged components and which allow the introduction of signals and power from outside the package.

Yet another advantage of the invention is to provide methods for fabricating three dimensional chip packages which accommodate high volumetric packaging while at the same time providing for a high level of cooling efficiency.

These and other objects and features of the present invention and the manner of obtaining them, and the invention itself will be best understood by reference to the following detailed description read in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a three dimensional chip package constructed in accordance with the teaching of the invention;

FIG. 2 depicts how to provide signal and power interconnections between pairs of the silicon carriers depicted in FIG. 1;

FIG. 3 depicts how to provide a hermetic seal for the cooling channels of the package in FIG. 1;

FIG. 4 depicts how coolant can be introduced into and removed from a channel between adjacent and opposite facing carriers via holes through the surrounding carriers that coincide with the gap between the carriers to be cooled;

FIG. 5 depicts an embodiment of the invention in which two carriers facing each other are interconnected at various points using large C4 type solder interconnections; and

FIG. 6 depicts a package constructed in accordance with the teachings of the invention, where the package is comprised of the "face-to-face" carriers depicted in FIG. 5.

According to an illustrative embodiment of the invention, a chip package comprises a plurality of multichip carriers with logic and memory devices attached to the surface and containing wiring to interconnect the devices.

Reference is made to FIG. 1 which depicts a number of these planer carriers joined in "shoe box" type assembly, assembly 100, with a large number of signal and power interconnects shown between the various sides of the box.

In particular, FIG. 1 depicts portions of seven chip carriers (101-107), with chips (such as chips 150 and 151) attached to certain faces of the carriers. For example, chips 150 and 151 are shown attached to one face of carrier 101. Certain opposing faces of the carriers, for example face "A" of carrier 106 and face "B" (hidden) of carrier 107, are devoid of chips and form the wall of channels between pairs of carriers. For example, FIG. 1 depicts channel 190, between carriers 104 and 105, and channel 191, between carrier 106 and 107.

The aforementioned signal and power interconnections between carriers are illustrated in FIG. 1 by connections 135 and 136. These connections allow high bandwidth communications between processor elements and memory. Signals and power from outside assembly 100 can be introduced through connections at the ends of the box (not shown).

According to the preferred embodiment of the invention, coolant can be introduced into channels 190 and 191 to efficiently cool assembly 100. FIG. 1 also depicts hermetic seals 175 and 176 which assure that the coolant (liquid or gas) remains in the depicted cooling channels.

The planar carriers shown in FIG. 1 can be constructed using silicon based thin film packaging technology as is well known to those skilled in the art. The individual carriers can be joined using solder.

According to a preferred method of fabricating the package depicted in FIG. 1, individual pads are coated with solder, prior to fixturing the carriers in their final position, to provide for the signal and power interconnections. The pads can then be joined to their mates in a mass reflow operation during which the solder on mating pads coalesces to form a filet. This process is illustrated in FIG. 2 which depicts a preferred way in which to provide the aforementioned signal and power interconnections between carrier pairs.

In particular, FIG. 2 shows solder on individual pairs of pads, e.g., 201 and 202, before reflow, and a set of solder filets, like filets 210 and 211, that result from the solder coalescing after reflow.

Reference is made to FIG. 3 which illustrates a preferred way in which to provide a hermetic seal for the cooling channels depicted in FIG. 1. To provide such a seal a single pad can be provided on the back of carriers 301 and 302, which is coated with solder and mates to a matching long pad on the carrier to which the primary carrier is mated. The solder coated pads are shown as elements 305 and 306 in FIG. 3.

During the same mass solder reflow process mentioned hereinbefore, the solder on the long pads coalesces to form a hermetic seal between the two joined carriers. The result of this joining and sealing process is continuous solder filet 310, also depicted in FIG. 3.

As indicated hereinbefore, the channel between adjacent and opposite facing carriers, which are devoid of chips, can be used for cooling by providing a method for introducing and removing cooling liquid to/from the cooling channels. One method and carrier assembly for performing this function is illustrated in FIG. 4.

FIG. 4 depicts how coolant can be introduced into and removed from a channel between adjacent and opposite facing carriers via holes through the surrounding carriers that coincide with the gap between the car-

riers to be cooled. As shown in FIG. 4, coolant can be introduced through the holes on one side of the "shoe box" assembly and can be removed through holes on the opposite side of the assembly. These holes, shown for example as apertures 401 and 402 in FIG. 4, can be fabricated when fabricating the carriers themselves by using anisotropic etching or electrodischarge machining.

The use of the aforementioned silicon based thin film packaging technology for forming the carriers is preferred because it allows for the formation of fine grooves on the backside of the carriers which can improve thermal transfer to the cooling liquid in the channels.

FIG. 4 also depicts an example of a suitable spatial relationship, in the context of the illustrative embodiment of the invention being described, between etched apertures (e.g., apertures 401 and 402), hermetic solder filets (e.g., filets 410 and 420), the chips mounted in the package (e.g., C4 chips 450-452 which are visible, and chip 453 which is hidden from view), and coolant channel 499, shown, for the sake of illustration only, to be carrying coolant in the direction indicated by arrow 425.

An alternate embodiment of a three dimensional package and packaging concept contemplated by the invention comprises pairs of carriers facing one another, connected to each other at various points throughout their area using, for example, large C4 type solder interconnections, as well as being connected to other carriers at their edges. A suitable arrangment which has the chip carrying faces of the carriers facing one another is depicted in FIG. 5.

According to the illustrative embodiment of the invention shown in FIG. 5, chip carriers 501 and 502 have their chip carrying faces, shown as "a" and "b" respectively, interconnected using Macro C4 connections 550-553. Chips 520 and 521, on carrier 501, and chips 522 and 523, on carrier 502, are shown mounted to their respective carriers using standard C4 connections at reference numerals 570-573.

An arrangement for connecting pairs of carriers like those depicted in FIG. 5 to form a three dimensional package of the type contemplated by the invention, is depicted in FIG. 6.

In FIG. 6 it can be seen that four planar "face-to-face" carriers (actually pairs of carriers), 601-604, are arranged in a "shoe box" type assembly, assembly 600, with cooling channels 620 and 621 being fabricated between face-to-face carrier pairs 601 and 602, and pairs 603 and 604.

Other chips are shown on the face of carriers that are not of the face-to-face type. For example, chips 620 and 621 are shown on carrier 622, and solder filets, like filet 665, are shown for interconnecting pairs of carriers, like 622 and 623. The filets can be created as described hereinbefore with reference to FIGs. 1 and 2.

FIG. 6 also depicts hermetic seals 640-645, which, as described hereinbefore with reference to FIG. 3, seal depicted channels 620 and 621 to keep any coolant introduced into these channels, within the channels.

It should be noted with reference to both FIGs. 5 and 6 that when using face-to-face type carriers, the carrier not contacting the coolant directly is cooled by conduction through the large number of C4 like interconnections between itself and the carrier that is in contact with the coolant.

The above described invention will yield high performance for systems where a single processor element can be contained within a single carrier. In this case the additional carriers can be used to provide memory or additional processor elements. As indicated hereinbefore, one particular embodiment of the invention contemplated would have the internal carriers contain memory that could be shared by a number of processing elements. Using this packaging structure would allow each processor to have equal access to memory due to the spatial symmetry of the package.

For systems that cannot be contained on a single carrier the packages contemplated by the invention provide miminal path delay from carrier to carrier thus improving system performance.

As those skilled in the art will readily appreciate the above described packages and techniques provide means to cool a system having a very high volumetric power density.

Certain applications, like those employing cryogenic switches or storage devices, may require that the packaged circuits be immersed in a coolant. In such applications circuit devices may actually be mounted within the cooling channels, formed in accordance with the teachings set forth hereinabove.

Claims

1. A three dimensional chip package (100) comprising:
   (a) a plurality of planar semiconductor substrates (101-107; 601-604, 621, 622) joined in an assembly, each substrate having at least one semiconductor electronic device (150, 151; 620, 621) mounted thereon, and each substrate having at least one electronic contact location to another substrate;
   (b) means (175, 176; 640-645) for physically joining at least a subset of said plurality substrates so that opposing faces of said substrates belonging to said subset form a hermetically sealed enclosure defining a cooling channel and

riers to be cooled. As shown in FIG. 4, coolant can be introduced through the holes on one side of the "shoe box" assembly and can be removed through holes on the opposite side of the assembly. These holes, shown for example as apertures 401 and 402 in FIG. 4, can be fabricated when fabricating the carriers themselves by using anisotropic etching or electrodischarge machining.

The use of the aforementioned silicon based thin film packaging technology for forming the carriers is preferred because it allows for the formation of fine grooves on the backside of the carriers which can improve thermal transfer to the cooling liquid in the channels.

FIG. 4 also depicts an example of a suitable spatial relationship, in the context of the illustrative embodiment of the invention being described, between etched apertures (e.g., apertures 401 and 402), hermetic solder filets (e.g., filets 410 and 420), the chips mounted in the package (e.g., C4 chips 450-452 which are visible, and chip 453 which is hidden from view), and coolant channel 499, shown, for the sake of illustration only, to be carrying coolant in the direction indicated by arrow 425.

An alternate embodiment of a three dimensional package and packaging concept contemplated by the invention comprises pairs of carriers facing one another, connected to each other at various points throughout their area using, for example, large C4 type solder interconnections, as well as being connected to other carriers at their edges. A suitable arrangment which has the chip carrying faces of the carriers facing one another is depicted in FIG. 5.

According to the illustrative embodiment of the invention shown in FIG. 5, chip carriers 501 and 502 have their chip carrying faces, shown as "a" and "b" respectively, interconnected using Macro C4 connections 550-553. Chips 520 and 521, on carrier 501, and chips 522 and 523, on carrier 502, are shown mounted to their respective carriers using standard C4 connections at reference numerals 570-573.

An arrangement for connecting pairs of carriers like those depicted in FIG. 5 to form a three dimensional package of the type contemplated by the invention, is depicted in FIG. 6.

In FIG. 6 it can be seen that four planar "face-to-face" carriers (actually pairs of carriers), 601-604, are arranged in a "shoe box" type assembly, assembly 600, with cooling channels 620 and 621 being fabricated between face-to-face carrier pairs 601 and 602, and pairs 603 and 604.

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It should be noted with reference to both FIGs. 5 and 6 that when using face-to-face type carriers, the carrier not contacting the coolant directly is cooled by conduction through the large number of C4 like interconnections between itself and the carrier that is in contact with the coolant.

The above described invention will yield high performance for systems where a single processor element can be contained within a single carrier. In this case the additional carriers can be used to provide memory or additional processor elements. As indicated hereinbefore, one particular embodiment of the invention contemplated would have the internal carriers contain memory that could be shared by a number of processing elements. Using this packaging structure would allow each processor to have equal access to memory due to the spatial symmetry of the package.

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   (b) means (175, 176; 640-645) for physically joining at least a subset of said plurality substrates so that opposing faces of said substrates belonging to said subset form a hermetically sealed enclosure defining a cooling channel and

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(c) means for introducing and removing liquid or gaseous coolant to and from said cooling channel.

2. Apparatus as set forth in claim 1 wherein each cooling channel is hermetically sealed, by solder.

3. Apparatus as set forth in claim 1 or 2 wherein at least one of said electrical contact locations is formed by a solder filet (135, 136) which electrically interconnects pads on adjacent substrate edges.

4. Apparatus as set forth in claim 1 or 2 wherein at least one of said electrical contact locations is formed by a solder connection between opposing substrate faces (601-604) both of which have at least one of said semiconductor electronic devices mounted thereon.

5. Apparatus as set forth in claim 3 or 4, wherein at least one of said cooling channels is formed by a plurality of substrate surfaces which are devoid of semiconductor electronic devices.

6. Apparatus as set forth in claim 6 wherein said means for introducing and removing cooling fluid forms a part of said enclosure and includes apertures through which the fluid may be introduced and removed.

Patentansprüche

1. Dreidimensionale Chippackung (100), die folgendes umfaßt:
(a) eine Vielzahl planarer Halbleitersubstrate (101-107; 601-604, 621, 622), die in einem Aufbau zusammengefügt sind, wobei auf jedem Substrat wenigstens ein elektronischer Halbleiterbaustein (150, 151; 620, 621) angebracht ist und jedes Substrat wenigstens eine elektronische Kontaktstelle zu einem weiteren Substrat hat;
(b) Mittel (175, 176; 640-645) für die physische Verbindung von wenigstens einer Untermenge aus der Vielzahl von Substraten, so daß einander gegenüberliegende Oberflächen der Substrate aus dieser Untermenge eine hermetisch abgeschlossene, einen Kühlmittelkanal bildende Ummantelung bilden; und
(c) Mittel zur Einleitung und Ableitung eines flüssigen oder gasförmigen Kühlmittels in bzw. aus dem Kühlmittelkanal.

2. Vorrichtung gemäß Anspruch 1, wobei jeder Kühlmittelkanal durch Lot hermetisch abgeschlossen ist.

3. Vorrichtung gemäß Anspruch 1 oder 2, wobei wenigstens eine der elektrischen Kontaktstellen durch einem Lotsteg (135, 136) gebildet wird, der Verbindungsflächen auf benachbarten Substratkanten elektrisch verbindet.

4. Vorrichtung gemäß Anspruch 1 oder 2, wobei wenigstens eine elektrische Kontaktstelle durch eine Lötverbindung zwischen einander gegenüberliegenden Substratoberflächen (601-604) gebildet wird, wobei auf beiden wenigstens jeweils einer der elektronischen Halbleiterbausteine angebracht ist.

5. Vorrichtung gemäß Anspruch 3 oder 4, wobei wenigstens einer der Kühlmittelkanäle aus einer Vielzahl von Substratoberflächen gebildet wird, auf denen sich keine elektronischen Halbleiterbausteine befinden.

6. Vorrichtung gemäß Anspruch 5, wobei die Mittel zur Einleitung und Ableitung des Kühlmittels einen Teil der Ummantelung bilden und Öffnungen enthalten, durch die die Flüssigkeit eingeleitet und abgeleitet werden kann.

Revendications

1. Boîtier de puces tridimensionnel (100) comprenant :
(a) une pluralité de substrats semiconducteurs plans (101 à 107, 601 à 604, 621, 622) raccordés en un ensemble, chaque substrat comportant au moins un dispositif électronique à semiconducteur (150, 151, 620, 621) monté sur celui-ci et chaque substrat comportant au moins un emplacement de contact électronique vers un autre substrat,
(b) des moyens (175, 176, 640 à 645) pour raccorder physiquement au moins un sous-ensemble de

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ladite pluralité de substrats de sorte que les faces opposées desdits substrats appartenant audit sous-ensemble forment une enceinte hermétiquement fermée définissant un canal de refroidissement, et (c) des moyens pour introduire et enlever un agent refroidissant liquide ou agent refroidissant gazeux dudit canal de refroidissement.

2. Dispositif selon la revendication 1, dans lequel chaque canal de refroidissement est fermé hermétiquement par de la soudure.

3. Dispositif selon la revendication 1 ou 2, dans lequel au moins un desdits emplacements de contact électrique est formé par un filet de soudure (135, 136) qui interconnecte électriquement des plots sur les bords de substrats contigus.

4. Dispositif selon la revendication 1 ou 2, dans lequel au moins un desdits emplacements de contact électrique est formé par une connexion de soudure entre des faces de substrat opposées (601 à 604) dont les deux ont au moins un desdits dispositifs électroniques à semiconducteur monté sur ceux-ci.

5. Dispositif selon la revendication 3 ou 4, dans lequel au moins un desdits canaux de refroidissement est formé par une pluralité de surfaces de substrats qui sont dépourvues de dispositifs électroniques à semiconducteur.

6. Dispositif selon la revendication 6, dans lequel lesdits moyens pour introduire et enlever le fluide de refroidissement forment une partie de ladite enceinte et comprennent des ouvertures à travers lesquelles le fluide peut être introduit et enlevé.

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