

CLOCK DELAY FOR A CENTRAL PROCESSING UNIT
BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to performance optimization systems for central processing units, e.g. microprocessors and preferably, to systems for improving the efficiency of a microprocessor coupled to a plurality of data processing devices on a bus.

2. Art Background:

It is typical in many data processing systems to couple a microprocessor to a plurality of data processing devices, such as for example, printers, RAM memories, magnetic disks and the like, along a system bus. As is well known, the microprocessor includes digital circuitry which completes logical operations in accordance with clock signals provided by a clock generator. The clock generator may comprise a crystal based oscillator disposed either on the microprocessor chip itself, or external to the chip. The clock generator provides cyclic repetitive digital signals of a fixed frequency to the microprocessor. All microprocessor operations are synchronous with the clock generator signals which are applied.

Although microprocessor operations are controlled by the frequency of the clock signals, the acquisition time for communicating with other data processing devices coupled to the common bus is a function of the speed of the particular device. For example, although the microprocessor may operate at maximum speed (for example 33.3 MHz) as driven by the clock, other devices, such as random access memory (RAM) generally cannot operate at the speed of the microprocessor. In the event the microprocessor issues a read command to obtain data stored in a RAM coupled to the bus, the processor must generally wait until valid data is applied to bus data lines by the RAM to permit the data transfer operation

to be completed. During this wait period, the microprocessor must interrupt its operations during the clock cycles required for the RAM to apply valid data to the bus. Other data processing devices, such as magnetic disks and the like, also require the

5 microprocessor to delay processing operations until the data transfer is complete.

As will be described, the present invention provides methods and apparatus for increasing the performance of a microprocessor coupled to slower data processing devices. A
10 fractional increment of a predefined time may be added to particular clock cycles, to delay subsequent cycles sufficiently long to permit a slower device to complete the requested operation. At present processor speeds, the time savings of the fractional increment provided by the present invention is significant compared
15 to waiting the standard full clock cycle.

SUMMARY OF THE INVENTION

According to the present invention there is provided an apparatus for increasing performance of a central processing unit (CPU) employed in a data processing system coupled to a plurality of data processing devices, comprising:

clocking means for generating a first repetitive cyclic digital signal of a predefined frequency;

delay means coupled to said clocking means and said CPU for generating a second repetitive cyclic digital signal having a frequency which is a predefined submultiple of the frequency of said first cyclic digital signal and for extending predetermined cycles of said second cyclic digital signal by a predefined fractional increment of said cycles, such that logical operations performed in synchronism with said second cyclic digital signal by digital circuitry in said CPU are held in abeyance while said cycles are extended, said delay means extending said predetermined cycles only during operations involving signal transmissions between at least one of said data processing devices and said CPU;

whereby said logical operations performed by said CPU may be held in abeyance for less than a full one of said cycles.

Also according to the present invention there is provided in a data processing system, including a central processing unit (CPU) coupled to a plurality of data processing devices, a method of increasing performance of said CPU, comprising the steps of:

generating a first repetitive cyclic digital signal of a predefined frequency;

generating a second repetitive cyclic digital signal at a frequency which is a predefined submultiple of said frequency of said first signal;

extending predetermined cycles of said second cyclic digital signal by a predefined fractional increment of said

cycles, such that logical operations performed in synchronism
with said second cyclic digital signal by digital circuitry
in said CPU are held in abeyance while said cycles are
extended, said cycles being extended only during operations
5 involving signal transmissions between ones of said data
processing devices and said CPU;

providing said second cyclic digital signal to said CPU;
whereby said logical operations performed by said
CPU may be held in abeyance for less than a full one of
10 said cycles.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram generally illustrating the architecture of the present invention.

5 Figure 2(a) is a timing diagram illustrating a typical prior art system wherein data is provided to the CPU immediately after the completion of a clock cycle, thereby delaying the acquisition of data until the following cycle.

10 Figure 2(b) is a timing diagram illustrating the use of the present invention to increase the length of predetermined clock cycles by fractional increments.

DETAILED DESCRIPTION OF THE INVENTION

Apparatus and methods for increasing the performance of a central processing unit (CPU) employed in a data processing system coupled to a bus having a plurality of data processing devices is disclosed. In the following description for purposes of
5 explanation, specific numbers, cycle times, memory devices, CPUs, etc. are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well known circuits
10 and devices are shown in block diagram form in order not to obscure the present invention unnecessarily.

Referring to Figure 1, the present invention is illustrated in a generalized block diagram form. A CPU 10, which may be a motorola 68020, is coupled to a plurality of data processing devices
15 (DP#A...DP#N) over a bus 12. The data processing devices include, for example RAM 14 (DP#A) as well as other devices such as disk drives, printers, and other data processing resources. A clock source 16 provides a repetitive cyclic digital signal having a predetermined frequency, as is known in the art. In the presently
20 preferred embodiment, clock generator 16 outputs digital signals having a frequency of 33.333 MHz, and is driven by a crystal oscillator. The output of clock source 16 is coupled to a finite state machine 18 which, as will be described, delays predetermined cycles of the system clock signal (line 20) to permit maximum
25 utilization of CPU processing time. Although in the presently preferred embodiment, the functions of the present invention are provided by a finite state machine disposed in a programmable array logic (PAL) device, it will be appreciated by one skilled in the art that finite state machine (FSM) 18 may comprise
30 a variety of digital circuits which utilize various forms of hardware as well as software. The finite state machine outputs

a system clock signal to CPU 10 over a system clock line 20. As illustrated, a bus cycle line 22 is provided between CPU 10 and FSM 18 to permit feedback communication between CPU 10 and FSM 18. It will be noted that the embodiment illustrated in Figure 1 is diagrammatical in form, and illustrates those signals unique to the present invention. However, other control signals and lines, such as data lines, address lines and the like are not shown for simplicity. Although not described in the specification these other lines, signals and the like will be apparent to one skilled in the art.

With reference now to Figures 1 and 2, the operation of the present invention will be described. As previously discussed, clock source 16 outputs a digital clock signal of a predefined frequency that drives finite state machine 18. When CPU 10 is executing logical operations which do not involve data transfers along bus 12, CPU 10 operates at its maximum frequency. The maximum frequency clock is supplied by FSM 18 via clock line 20. In the presently described embodiment, the system clock signal has a frequency of one-half of the output of clock source 16, or approximately 16.67 MHz. As is well known, microprocessors perform logical operations in accordance with full clock cycles, such that each sequence of logical operations performed internally occur in accordance with full clock cycles such as those illustrated in Figure 2(a). In instances where CPU 10 accesses data processing devices coupled to bus 12 (e.g. in a read or write mode), many of those devices operate at different speeds than that of the microprocessor. For example, in the event CPU 10 is instructed to read data stored in RAM 14, the CPU issues a read command over bus 12. Upon receipt of this command as well as valid address information, RAM 14 accesses that portion of its memory and applies the valid data to data lines on bus 12. The time required for RAM 14 to access the data and respond to the read command of CPU 10 is generally much slower than the operating speed of the microprocessor. During the time RAM 14

is completing the read operation, CPU 10 would, in prior art systems, be maintained in a wait state for an integer number of clock cycles until valid data is applied to the data lines of bus 12. For example, if a read request is issued by CPU 10 in clock state 0, and valid data is applied just after clock state 7, CPU 10 could not access such valid data until the next full clock cycle, since the microprocessor is incapable of waiting fractions of clock periods (see Figure 2(a)).

With reference now to Figure 2(b), the operation of the present invention is illustrated. In the event CPU 10 is required to communicate with data processing devices coupled to bus 12, a bus cycle indicator signal is applied to bus cycle line 22 and received by FSM 18. In the present embodiment FSM 18 delays the fourth clock state from the beginning of the bus access cycle of the system, a predetermined fractional increment of the cycle time. In the present embodiment, FSM 18 "stretches" the fourth clock state within the bus access cycle by 100% as illustrated best in Figure 2(b). The stretching of the fourth clock state delays all internal logical operations of the microprocessor for an additional half of a cycle. Thus, although CPU 10 is unable to function based on fractions of clock periods, the effect of the present invention is to delay all internal operations of the microprocessor for an additional stretch period to permit slower devices such as RAM 14, to complete the requested data operation and provide valid data on bus 12 by clock state 7. From the perspective of CPU 10, it receives valid data from the data lines of bus 12 at the completion of the sixth clock state, and thereby obviates the need for CPU 10 to be maintained in a wait state for integral multiples of the clock cycle. For example, in the operations illustrated in Figure 2(a), absent the present invention, CPU 10 would be unable to read valid data until the completion of state 8 (beginning of state 9).

However, by using the present invention's delay system, valid data is read by CPU 10 at the completion of clock state six in the bus cycle. It will be appreciated, that although the present invention is illustrated and described with reference to particular clock states to be "stretched" and with regard to particular data processing devices coupled to bus 12, that the present invention may be utilized in any of a number of ways in order to increase the performance of CPU 10. For example, using the present invention clock states may be stretched by any predefined fractional increment of the given cycle, and that any combination or multiple of clock states may be extended as required by the particular application and system configuration.

Using the present invention, system performance is increased by eliminating wasted overhead in CPU "wait condition" clock cycles. As shown in Figures 2(a) and 2(b), the time savings using the present invention may be measured as the difference in clock cycles to complete a full bus cycle. In the present embodiment, a device communicating with the CPU 10 transmits a DSACK signal prior to ending the bus cycle. Upon sensing the DSACK signal (which must occur on a negative edge), the CPU 10 expects any valid data to be present on the lines one clock cycle later. As shown in the Figures, the present invention permits the completion of the bus cycle sooner, and therefore maximizes system performance.

Accordingly, apparatus and methods for increasing the performance of a central processing unit employed in the data processing system coupled on a bus to a plurality of data processing devices is disclosed. As the speed of processors increase, it will be appreciated that the advantages of the present invention become more pronounced. While the present invention has been particularly described with reference to the embodiment

illustrated in Figures 1 and 2, it is contemplated that many modifications and materials, cycle times, and architectures could be made by one of ordinary skill in the art without departing from the scope of the invention.

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CLAIMS

1. An apparatus for increasing performance of a central processing unit (CPU) employed in a data processing system coupled to a plurality of data processing devices, comprising:
 - 5 a clocking means for generating a first repetitive cyclic digital signal of a predefined frequency;
delay means coupled to said clocking means and said CPU for generating a second repetitive cyclic digital signal having a frequency which is a predefined submultiple of the
10 frequency of said first cyclic digital signal and for extending predetermined cycles of said second cyclic digital signal by a predefined fractional increment of said cycles, such that logical operations performed in synchronism with said second cyclic digital signal by digital circuitry in said
15 CPU are held in abeyance while said cycles are extended, said delay means extending said predetermined cycles only during operations involving signal transmissions between at least one of said data processing devices and said CPU;
whereby said logical operations performed by said CPU
20 may be held in abeyance for less than a full one of said cycles.
2. The apparatus of claim 1, wherein said first cyclic digital signal has a frequency of approximately 33.3 MHz.
- 25 3. The apparatus of claim 1, wherein said CPU comprises a Motorola 68020.
4. The apparatus of claim 1, wherein said fractional increment comprises $1/2$ of a cycle of said second cyclic
30 digital signal.
5. The apparatus of claim 4, wherein at least one of said data processing devices comprises a digital memory.



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6. The apparatus of claim 5, wherein said CPU and said data processing device are coupled to a bus, and a bus cycle generally comprising eight clock states.

5 7. In a data processing system, including a central processing unit (CPU) coupled to a plurality of data processing devices, a method of increasing performance of said CPU, comprising the steps of:

10 generating a first repetitive cyclic digital signal of a predefined frequency;

generating a second repetitive cyclic digital signal at a frequency which is a predefined submultiple of said frequency of said first signal;

15 extending predetermined cycles of said second cyclic digital signal by a predefined fractional increment of said cycles, such that logical operations performed in synchronism with said second cyclic digital signal by digital circuitry in said CPU are held in abeyance while said cycles are extended, said cycles being extended only during operations involving signal
20 transmissions between ones of said data processing devices and said CPU;

providing said second cyclic digital signal to said CPU; whereby said logical operations performed by said CPU may be held in abeyance for less than a full one of said cycles.

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8. The method of claim 7, wherein said second cyclic digital signal has a frequency of approximately 16.67 MHz.

9. The method of claim 7 wherein said CPU comprises a
30 Motorola 68020.

10. The method of claim 7, wherein said fractional increment comprises $1/2$ of a cycle of said second cyclic digital signal.

35 11. The method of claim 10, wherein at least one of said data processing devices comprises a digital memory.



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12. The method of claim 11, wherein said CPU and said data processing devices are coupled to a bus, a bus cycle generally comprising eight clock states.

5 13. An apparatus for increasing the performance of a central processing unit (CPU) substantially as hereinbefore described with reference to the accompanying drawings.

10 14. A method of increasing performance of a CPU substantially as hereinbefore described with reference to the accompanying drawings.

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