DESCRIPTION

METHOD OF PROCESSING WIRING SUBSTRATE

TECHNICAL FIELD

[0001]

The present invention relates to a method of processing a wiring substrate that includes a configuration in which conductors locally disposed on a substrate are coated with resin having inorganic members that form a filler and are dispersed in an organic member, and the wiring substrate is preferably used for a multi-layer wiring substrate.

This application claims priority from Japanese Patent Application No. 2016-235054 filed on December 2, 2016, the contents of which are incorporated herein by reference in their entirety.

BACKGROUND ART

[0002]

As a method of processing a wiring substrate suitable to a multi-layer wiring substrate, for example, a method disclosed in Patent Document 1 or Patent Document 2 is known.

Patent Document 1 discloses a method of manufacturing a multi-layer wiring substrate by use of a ceramic wiring substrate as a base substrate. Particularly, paragraph 0078 of Patent Document 1 shows that, in the middle of a manufacturing process, there is a case where the foregoing multi-layer wiring substrate is covered with an insulating film and top surfaces of conductors are not exposed.

[0003]

The above-mentioned situation is due to the reasons, such that a surface of a die

cannot practically and completely be flat, a surface of a die is difficult to be completely brought into close contact with upper faces of wirings, heights of a wiring layer are difficult to be completely aligned with each other, or the like. Consequently, there is an explanation that the upper faces of the wirings are necessary to be exposed by removing a surface of an insulating film by a wet etching method, a dry etching method, a mechanical polishing method, or a method of combining the aforementioned methods. However, a specific solution is not disclosed in Patent Document 1.

[0004]

Generally, the aforementioned insulating film does not have a simple structure made of a single member but is formed of resin having inorganic members that form a filler and are dispersed in an organic member. Therefore, as shown in FIG. 12, for example, in the case of sequentially removing the insulating film from a surface of the insulating film by carrying out dry etching, since the inorganic members and the organic member are etched together, the processed surface becomes a rough surface.

[0005]

That is, in a state where the surface of the wiring layer is exposed, the surface of the wiring layer is not flatly exposed, residues (inorganic members or organic member) of the insulating film randomly remain on the surface of the wiring layer, and furthermore the surface of the wiring layer is in a state of being rough. For this reason, in the case where a coating is formed on the exposed wiring layer, the surface of the coating stacked on the wiring layer is also in a state of being rough. Therefore, in the case of manufacturing a multi-layer wiring substrate, since it is necessary to repeat the above-described steps at various times, the closer to the upper layer of the multilayer wiring structure the wiring layer is located, the less flat of the coating surface of the wiring layer is.

[0006]

Patent Document 2 discloses a method of electroless plating a wiring layer. A first wiring layer and a solder resist layer in which acid soluble filler and acid insoluble filler which are made of an inorganic substance are mixed are provided on an insulating substrate in this order, the surface of the solder resist layer is subjected to plasma ashing and the both fillers thereby remain, and the surface of the solder resist layer is selectively removed. Thereafter, the acid soluble filler exposed from the surface of the solder resist layer is dissolved, the surface of the solder resist layer is subjected to roughening, and then a second wiring layer is electroless-plated using metal on the solder resist layer.

[0007]

Consequently, according to the description of Patent Document 2, in the manufacturing method thereof, since a plurality of recesses are formed on the surface of the solder resist layer, the adhesion strength of the second wiring layer provided thereon is improved. That is, Patent Document 2 has an object to rough the surface of the solder resist layer and discloses a reverse technique to a method of planarizing the surface of the solder resist layer.

[0008]

Currently, in multi-layer wiring substrates, there is a tendency that the number of stacked layers increases more than ever in order to increase a degree of integration per unit area. Therefore, as described above, a problem is becoming obvious in that the closer to the upper layer of the multilayer wiring structure the wiring layer is located, the less flat of the coating surface of the wiring layer is, and therefore a method of solving this has been developed.

PRIOR ART DOCUMENTS

PATENT DOCUMENTS

center thereof and penetrates therethrough; and a flange portion 85 that is formed so as to extend toward the lower outer peripheral face of the lower lid body 84. The lower lid 83 is configured so that the lower lid body 84 is inserted into the through hole 68 and the flange portion 85 is fitted into the fitting recess 80.

[0024]

Additionally, by screwing the flange portion 85 to a back surface 80a of the fitting recess 80, the lower lid 83 (top surface of the flange portion 85) is fastened and fixed to the top plate 64 (back surface 80a of the fitting recess 80).

[0025]

Accordingly, a plasma generation chamber S is formed and comparted in a space which is formed such that both an upper opening and a lower opening of the through hole 68 formed on the cylindrical body 65 are blocked by the microwave transmission window 70 and the lower lid 83.

A ring-shaped annular groove 91 is formed on the outer peripheral face of the lower lid body 84, and the annular groove 91 and an inner peripheral face 68a of the through hole 68 that blocks the annular groove 91 form an annular passage. The annular groove 91 is formed at the position opposed to the opening of a gas introduction channel 82 formed on the inner peripheral face 68a of the through hole 68, and a plasma generation gas (oxygen) that is supplied from the gas introduction channel 82 is introduced into the annular passage (annular groove 91).

[0026]

A top surface outer circumferential edge of the lower lid body 84 is cleaved, and therefore a cleaved groove (gas introduction channel 82) that communicates the plasma generation chamber S to the annular groove 91 (annular passage) is formed. In addition, the plasma generation gas introduced into the annular groove 91 is introduced into the

In FIG. 2E, a Cu coating 14 is manufactured on the seed layer 12 exposed by the openings 13s by an electroplating method.

In FIG. 2F, a Cu coating 14p1 that is patterned on the seed layer 12 is obtained by removing the dry film resist 13p. The Cu coating 14p1 according to the embodiment of the invention is used as a fine wiring (first electroconductive film) having, for example, a height of approximately 2 μm and a width of approximately 2 μm to 4 μm.

In FIG. 2G, the patterned Cu coating 14p1 is used as a mask, and a seed layer 12 is removed etching. Accordingly, a configuration is obtained in which the seed layers 12p located at the positions which overlap the patterned Cu coating 14p1 only remain.

[0036]

In FIG. 2H, a second interlayer insulating film 15 is disposed so as to coat the first interlayer insulating film 11 and the patterned Cu coating 14p1 located thereon.

FIG. 2I, the second interlayer insulating film 15 is subjected to ashing treatment until the surface of the Cu coating 14p1 is exposed (step A). Therefore, an organic member is removed from the surface layer side of the resin constituting the second interlayer insulating film 15. By carrying out the above-described step A, an organic member is only removed from the resin while leaving inorganic members until a desired depth (surface position of the Cu coating 14p1) is obtained.

Thereafter, of the second interlayer insulating film 15, the portions that were subjected to the step A (i.e., inorganic members remaining on the surface layer side of the resin which was subjected to the step A) are removed by carrying out wet cleaning. Because of this, the inorganic members, which are located above the surface of the patterned Cu coating (conductors) 14p1, remain on the resin, and form a filler, are removed by wet cleaning.

As a result, the surfaces of the exposed Cu coating (conductors) 14p2 and the

dispersed in the organic member. In the state shown in FIGS. 3A and 3B, the Cu coatings (conductors) 14p locally disposed on the substrate W is covered with the resin.

[0040]

FIGS. 4A and 4B show a state where the step A was carried out until a thickness of the second interlayer insulating film (resin) 15 becomes substantially a half. In FIGS. 4A and 4B, reference numeral L1 represents a boundary between the post-treated region by the step A and an untreated region. That is, in the second interlayer insulating film (resin) 15, the region (shown by thin black meshed pattern in FIGS. 4A and 4B) that is located lower than the surface 15sp1 and located above the portion represented by reference numeral L1 is the portion that was subjected to the step A (post-treated region). In contrast, the region (shown by a thick black meshed pattern in FIGS. 4A and 4B) that is located lower than the portion represented by reference numeral L1 is the portion (untreated region) which has not been carried out yet.

In FIG. 4B, the portion that was subjected to the step A (post-treated region) is in a state where the inorganic members included in the resin remain and the organic member is only degraded and removed. The above-described ashing treatment is also referred to as an ashing process.

[0041]

FIGS. 5A and 5B show a state where the aforementioned ashing treatment (step A) were further repeatedly carried out, and the portion from which the organic member is only removed, that is, the portion that was subjected to the step A (post-treated region) reached the surfaces of the Cu coatings (conductors) 14p locally disposed on the substrate W. In FIGS. 5A and 5B, reference numeral L2 represents a boundary between the post-treated region that is subjected to the step A and the untreated region. That is, in the second interlayer insulating film (resin) 15, the region (shown by thin black

meshed pattern in FIGS. 5A and 5B) that is located lower than the surface 15sp2 and located above the portion represented by reference numeral L2 is the portion that was subjected to the step A (post-treated region). In contrast, the region (shown by a thick black meshed pattern in FIGS. 5A and 5B) that is located lower than numeral L2 is the portion (untreated region) which has not been carried out yet.

[0042]

In FIG. 5B, the portion that was subjected to the step A (post-treated region) is in a state where the inorganic members included in the resin remain and the organic member is only degraded and removed.

Accordingly, a state is obtained where organic member does not mostly remain in the second interlayer insulating film (resin) 15 that is located above the surfaces of the Cu coatings (conductors) 14p (portion represented by reference numeral L2) and inorganic members forming a filler only remain. On the other hand, the second interlayer insulating film (resin) 15 located lower than the surfaces of the Cu coatings (conductors) 14p is in a state of not being changed from before ashing is carried out, that is, a state is maintained where the inorganic members forming a filler are dispersed in the organic member.

In the above-mentioned FIGS. 4A (4B) and 5A (5B), for the sake of convenience of explanation, it is shown that the step A is divided into two steps, but in general, FIG. 4A and FIG. 5A are carried out as a continuous process (one step A). However, as necessary, the step A may be carried out as a plurality of steps (a plurality of times).

[0043]

FIGS. 6A and 6B show a state where (step B) the inorganic members that remain in the surface layer side of the resin after being subjected to the step A is removed

by use of a wet cleaning method with respect to the wiring substrate which is in a state shown in FIG. 5A, that is, in a state where a ashing treatment (step A) was carried out until the positions of the surfaces of the Cu coatings 14p1 coincides with the top surface of the second interlayer insulating film 15. Therefore, the inorganic members that form a filler and remain in the resin located above the surfaces of the conductors are removed by wet cleaning. On the other hand, the resin located lower than the surfaces of the conductors is in an original state, that is, it is maintained in a state where the inorganic members forming a filler are dispersed in the organic member without being affected by wet cleaning.

Accordingly, the invention contributes to provision of a method of processing a wiring substrate which can carry out a process so that the surfaces 14ps3 of exposed conductors and the surface 15ps3 of the resin surrounding the conductors are on the same plane in order to manufacture a layered structure.

[0044]

FIG. 7 is an SEM picture showing the surface of the resin in a state shown in FIG. 3A (a previous state where the step A is carried out. From this picture, it was apparent that the surface of the second interlayer insulating film (resin) 15 has a profile including micro recesses provided on a substantially flat shape. The average roughness height Ra of this surface was 0.09 μm.

[0045]

FIG. 8 is an SEM picture showing the surface of the resin in a state shown in FIG. 5A (a state where the portion that was subjected to the step A (post-treated region) reaches the surfaces of the Cu coatings (conductors) 14p locally disposed on the substrate W). From this picture, it was apparent that the entire surface of the second interlayer insulating film (resin) 15 are covered with hemispherical structures, the aforementioned

structures forms projecting portions, and a gap between the structures forms a recess. The average roughness height Ra of this surface was 0.44 μm.

Accordingly, it was inferred that the second interlayer insulating film (resin) 15 which was subjected to the step A is in a state where organic member does not mostly remain and inorganic members forming a filler only remain.

[0046]

FIG. 9 is an SEM picture showing the surface of the resin in a state shown in FIG. 6A (a state where, after the step A is carried out, the inorganic members remaining on the surface layer side of the resin which was subjected to the step A is removed by use of a wet cleaning method). From this picture, it was apparent that the surface of the second interlayer insulating film (resin) 15 has a profile including micro recesses provided on a substantially flat shape. This means that, in the picture (FIG. 8) showing that the step A was carried out, it was apparent that the hemispherical structures which are present on the surface of the second interlayer insulating film (resin) 15 are removed by carrying out the step B. The average roughness height Ra of this surface was 0.14 μm.

[0047]

From the results of FIGS. 7 to 9, the following points were apparent.

By carrying out the step B subsequent to the step A, the inorganic members that form a filler and remain in the resin located above the surfaces of the conductors are removed by wet cleaning.

On the other hand, the resin located lower than the surfaces of the conductors is in an original state, that is, it is maintained in a state where the inorganic members forming a filler are dispersed in the organic member without being affected by wet cleaning.

Accordingly, the invention contributes to provision of a method of processing a wiring substrate which can carry out a process so that the surfaces of exposed conductors