to the word line WLa (hereinafter also referred to as a nonselected reading word line) connected only with the anti-fuse memories 2a and 2b as nonselected read memories.

[0041] Thereafter, a selected reading bit voltage of 0 V is applied to the selected reading bit line BLb. Accordingly, in the anti-fuse memory 2c as a selected read memory, the selected reading word voltage of 1.2 V is applied from the word line WLb to the P-type semiconductor region 8 of the rectifier element 3, and the selected reading bit voltage of 0 V is applied from the bit line BLa to the diffusion region 5 at one end of the memory capacitor 4.

[0042] When the memory gate insulating film 6 of the memory capacitor 4 in the anti-fuse memory 2c as a selected reading memory is in a data programmed state due to dielectric breakdown, forward-biased voltage from the P-type semiconductor region 8 to the N-type semiconductor region 7 is applied at the rectifier element 3 due to the selected reading word voltage of 1.2 V applied to the word line WLb. Accordingly, in the anti-fuse memory 2c, the selected reading word voltage applied to the word line WLb is applied from the rectifier element 3 to the bit line BLa through the memory capacitor 4.

[0043] As a result, a voltage which is lowered from the selected reading word voltage of 1.2 V by the value of the built-in potential through the anti-fuse memory (the selected read memory) 2c is applied to the bit line BLa. Accordingly, the bit line BLa is electrically connected through the anti-fuse memory 2c to the word line WLb, so that the selected reading bit voltage of 0 V is changed to 0.5 V. Thus, the voltage is changed.

[0044] When no dielectric breakdown occurs to the memory gate insulating film 6 of the memory capacitor 4 and thus no data is programmed in the anti-fuse memory 2c as a selected read memory, the electrical connection between

[0096] With the above-described configuration, in the semiconductor memory device 1a, the bit line contacts BC1a and BC4a (BC3a and BC6a) disposed in the periphery and arranged in one direction (in this case, the row direction) are connected with the two anti-fuse memories $2b_1$ and $2b_5$, and the two anti-fuse memories $2b_9$ and $2b_{13}$ ($2b_4$, $2b_8$, $2b_{12}$, and $2b_{16}$), respectively, and the word line contacts WC1a and WC2a (WC5a and WC6a) disposed in the periphery and arranged in the other direction (in this case, the column direction) are connected with the two anti-fuse memories $2b_1$ and $2b_2$ and the two anti-fuse memories $2b_3$ and $2b_4$ ($2b_{13}$ and $2b_{14}$, and $2b_{15}$ and $2b_{16}$) respectively. In addition, in the semiconductor memory device 1a, the remaining bit line contact BC2a (BC5a) disposed in the central region is connected with the four anti-fuse memories $2b_2$, $2b_3$, $2b_6$, and $2b_7$ ($2b_{10}$, $2b_{11}$, $2b_{14}$, and $2b_{15}$), and the word line contact WC3a (WC4a) disposed in the central region is connected with the four anti-fuse memories $2b_5$, $2b_6$, $2b_9$, and $2b_{10}$ ($2b_7$, $2b_8$, $2b_{11}$, and $2b_{12}$).

[0097] With the configuration, the bit line contacts BC1a to BC6a and the word line contacts WC1a to WC6a are shared by two or more anti-fuse memories in the semiconductor memory device 1a, thereby achieving downsizing of the entire device. In addition, the same number (in this case, four) of anti-fuse memories can be connected with, for example, the single bit line BL1b to have identical capacitance, which prevents a problem such as reduction of the reading speed at data reading operation.

[0098] Although the semiconductor memory device 1a illustrated in FIG. 5 includes the sixteen anti-fuse memories, for example, the first word line WL1b and the second word line WL2b are alternately connected with a plurality of word line contacts arranged in the row

the memory gate electrode G of the anti-fuse memory $2d_3$ on the other side where the memory gate insulating film 6 of the anti-fuse memory $2d_3$ is disposed.

[0121] The four bit line contacts BC31, BC32, BC33, and BC34 (BC39, BC40, BC41, and BC42) arranged in the row direction in the periphery of the planar layout of the semiconductor memory device 31 are connected with the corresponding single anti-fuse memories $2d_1$, $2d_5$, $2d_9$, and $2d_{13}$ ($2d_4$, $2d_8$, $2d_{12}$, and $2d_{16}$), respectiely. With the configuration, the bit line contacts BC31, BC32, BC33, and BC34 (BC39, BC40, BC41, and BC42) arranged in the row direction in the periphery apply bit voltages only to the respective single anti-fuse memories $2d_1$, $2d_5$, $2d_9$, and $2d_{13}$ ($2d_4$, $2d_8$, $2d_{12}$, and $2d_{16}$).

[0122] In this manner, the bit line contacts BC31, BC32, BC33, BC34, BC39, BC40, BC41, and BC42 in the periphery apply bit voltages only to the respective single anti-fuse memories $2d_1$, $2d_5$, $2d_9$, $2d_{13}$, $2d_4$, $2d_8$, $2d_{12}$, and $2d_{16}$. However, the bit line contacts BC35, BC36, BC37, and BC38 arranged in the central region apply bit voltages to the two anti-fuse memories $2d_2$ and $2d_3$, the two anti-fuse memories $2d_6$ and $2d_7$, the two anti-fuse memories $2d_{10}$ and $2d_{11}$, and the two anti-fuse memories $2d_{14}$ and $2d_{15}$, respectively. In other words, the single bit line contacts BC35, BC36, BC37, and BC38 are shared by the two anti-fuse memories $2d_2$ and $2d_3$, the two anti-fuse memories $2d_6$ and $2d_7$, the two anti-fuse memories $2d_{10}$ and $2d_{11}$, and the two anti-fuse memories $2d_{14}$ and $2d_{15}$, respectively, which leads to downsizing of the entire device accordingly.

[0123] With the above-described configuration, in each of the anti-fuse memories $2d_1$, $2d_2$, $2d_3$, $2d_4$, $2d_5$, $2d_6$, $2d_7$, $2d_8$, $2d_9$, $2d_{10}$, $2d_{11}$, $2d_{12}$, $2d_{13}$, $2d_{14}$, $2d_{15}$, and $2d_{16}$ of the semiconductor memory device 31 illustrated in FIG. 7, the voltage application from the memory gate electrode G to

Ga of the anti-fuse memory $2h_3$ on the other side where the memory gate insulating film 6 of the anti-fuse memory $2h_3$ is disposed.

[0215] The four the bit line contacts BC71, BC72, BC73, and BC74 (BC79, BC80, BC81, and BC82) arranged in the row direction in the periphery of the planar layout of the semiconductor memory device 61 are connected only with the respective single anti-fuse memories $2h_1$, $2h_5$, $2h_9$, and $2h_{13}$ ($2h_4$, $2h_8$, $2h_{12}$, and $2h_{16}$). With the configuration, the bit line contacts BC71, BC72, BC73, and BC74 (BC79, BC80, BC81, and BC82) arranged in the row direction in the periphery apply bit voltages only to the respective single anti-fuse memories $2h_1$, $2h_5$, $2h_9$, and $2h_{13}$ ($2h_4$, $2h_8$, $2h_{12}$, and $2h_{16}$).

[0216] In this manner, the bit line contacts BC71, BC72, BC73, BC74, BC79, BC80, BC81, and BC82 in the periphery apply bit voltages only to the respective single anti-fuse memories $2h_1$, $2h_5$, $2h_9$, $2h_{13}$, $2h_4$, $2h_8$, $2h_{12}$, and $2h_{16}$. However, the bit line contacts BC75, BC76, BC77, and BC78 arranged in the central region apply bit voltages to the two anti-fuse memories $2h_2$ and $2h_3$, the two anti-fuse memories $2h_6$ and $2h_7$, the two anti-fuse memories $2h_{10}$ and $2h_{11}$, and the two anti-fuse memories $2h_{14}$ and $2h_{15}$, respectively. In other words, the single bit line contacts BC75, BC76, BC77, and BC78 are shared by the two anti-fuse memories $2h_2$ and $2h_3$, the two anti-fuse memories $2h_6$ and $2h_7$, the two anti-fuse memories $2h_{10}$ and $2h_{11}$, and the two anti-fuse memories $2h_{14}$ and $2h_{15}$, respectively, which leads to downsizing of the entire device accordingly.

[0217] In the above-described configuration, in each of the anti-fuse memories $2h_1$, $2h_2$, $2h_3$, $2h_4$, $2h_5$, $2h_6$, $2h_7$, $2h_8$, $2h_9$, $2h_{10}$, $2h_{11}$, $2h_{12}$, $2h_{13}$, $2h_{14}$, $2h_{15}$, and $2h_{16}$ of the semiconductor memory device 61 illustrated in FIG. 16, the voltage application from the memory gate electrode Ga