

"AN ELECTRONIC TIMEPIECE"

This invention relates to electronic timepieces.

Electronic wrist watches are known in which a liquid crystal display device produces an analog time display simulating that produced by the hands of a mechanical watch. In such wrist watches, a graduated time scale is formed by printing separately from the liquid crystal display device, so that the position of the "hands" in relation to the time scale appears to differ depending upon the direction of angle of observation due to the influence of the thickness of the display device and parallax effects. In addition, a considerable amount of labour is necessary to adjust the position of printing of the time scale in relation to the positions of the "hands".

According to one aspect of the present invention there is provided an electronic timepiece comprising: a display device comprising a plurality of segment electrodes having elongate sections which are arranged in a generally circular array, a plurality of common electrodes of sector-like shape arranged in three concentric rings of electrode units with each sector-like electrode being spaced from and opposing a group of an equal number of the segment electrodes to define therewith display elements; first means defining circuit paths connecting corresponding ones of the segment electrodes in each of the groups of segment electrodes, a display medium disposed between the segment electrodes and the common electrodes, the electrode units of the outer one of the three concentric rings of electrode units having radially projecting indicia parts spaced at regular

intervals in a circumferential direction thereof, the segment electrodes which are opposed to the indicia parts being formed longer by a length of the indicia parts than the remaining segment electrodes; second means for producing time information corresponding to at least 5 hours and minutes; and third means for causing the display elements comprising two of said concentric rings of electrode units except for the outer concentric ring of electrode units and the segment electrodes opposed to them to display the time information and for causing the display elements comprising said outer concentric ring of electrode 10 units and the segment electrodes opposed to it to display the graduated time scale.

The electronic timepiece may include fourth means for producing a plurality of pulse trains each of which has voltages selected from among a plurality of predetermined voltages having different values, 15 fifth means for applying at least one of the pulse trains for display to the segment electrodes of the display elements to be displayed in response to the time information and the segment electrodes electrically connected thereto, and for applying at least one of the pulse trains for non-display to the remaining segment electrodes, and 20 sixth means for applying to the common electrodes of some of the display elements at least one of the pulse trains having voltage values and phase relations effective to cause the display elements to display time information and for applying to the common electrodes of the remaining display elements at least one of the pulse trains having 25 voltage values and phase relations ineffective to cause the remaining display elements to display time information.

The fourth means may be arranged to produce predetermined voltages having values of 0, V_0 , $2V_0$ and $3V_0$.

The electronic timepiece in one embodiment includes seventh means for applying to other ones of the common electrodes of the display elements at least one of the pulse trains having voltage values and phase relations effective to cause the display of graduation display elements in turn at one second periods in response to the seconds time information.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figures 1A and 1B are circuit diagrams of an electronic timepiece according to the present invention;

Figure 2 is a plan view of a segment electrode arrangement of a display device of the electronic timepiece of Figures 1A and 1B;

Figure 3 is a plan view of a common electrode arrangement of the display device of the electronic timepiece of Figures 1A and 1B;

Figures 4 to 6 are circuit diagrams of parts of the electronic timepiece of Figures 1A and 1B;

Figure 7 is a timing chart of voltage pulses to explain the operation of the electronic timepiece shown in Figures 1A and 1B;

Figure 8 is an illustration of a display produced by the display device of the electronic timepiece of Figures 1A and 1B; and

Figures 9 to 12 illustrate another embodiment of an electronic timepiece according to the present invention.

Referring to Figures 1A and 1B, there is illustrated an

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electronic timepiece according to the present invention. The output signal from a quartz crystal oscillator 1 is frequency divided by a frequency divider 2 and is supplied to a decimal counter 3 to count units of seconds.

5 A carry output from the counter 3 is supplied to a seconds counter 4. Decimal counters 5, 6 count units of minutes and counters 7, 8 count units of hours from carry outputs of the preceding counter stage. These counters are adapted to produce binary coded decimal outputs. A duodecimal counter 9 is adapted
10 to count time upon receipt of the output from the counter 4 and produces a carry output which is supplied to the counter 7.

A timing pulse generating circuit 10 produces timing pulses successively at terminals P_1 to P_3 upon receipt of an output pulse of, for example, 128 Hz from the frequency divider 2.

15 Opening and closing of gate circuits 11 to 16 having AND logical function is controlled by these timing pulses, thereby to control the supply of outputs from the counters 3 to 8 to OR gate circuits 17, 18. Decoders 19, 20 convert the codes of outputs from the gate circuits 17, 18. An output conversion circuit 21
20 is adapted to alter the order of generation of signals in accordance with the odd number value and even number value of the output date from the gate circuit 18. These outputs are applied to a segment voltage supplying circuit 22 adapted to select the voltage to be applied to segment electrodes which will be described in
25 greater detail hereinafter. A common electrode, which will also

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be described in greater detail later, is adapted to be supplied with a voltage selectively by a common voltage supplying circuit 23. A pulse cyclically generated at the output terminal P_1 of the timing pulse generator 10 is divided by 2 by means of a flip-flop circuit 24, and is applied to a voltage selector 25. Voltages 0 , v_0 , $2v_0$ and $3v_0$ are periodically generated at terminals S_0 , S_1 , C_0 , C_1 respectively in synchronism with the signal applied to the voltage selector 25. A reference numeral 26 denotes an inverter.

10 Figures 2 and 3 illustrate the electrode arrangement of a liquid crystal display device of the electronic timepiece of Figures 1A and 1B.

 A segment electrode arrangement 27 shown in Figure 2 consists of 60 segment electrodes $27a$ radially arranged, 10 of which are connected as illustrated to terminals e_1 - e_{10} of the segment voltage supply circuit 22. Other segment electrodes are connected as follows. In the following description the segment electrodes are counted in the clockwise direction from the segment electrode $27a$ connected to the terminal e_1 . The tenth segment electrode is connected to the eleventh segment electrode. Similarly the ninth segment electrode is connected to the twelfth segment electrode. The first segment electrode and the twentieth segment electrode, the twentieth segment electrode and the twenty-first segment electrode, the nineteenth segment electrode and the twenty-second segment electrode, and the eleventh segment electrode

and the thirtieth segment electrode are connected to each other, respectively. Similar connections are made up to the sixtieth segment electrode.

Figure 3 shows a common electrode arrangement 28.

5 There will be seen that there is an outer common electrode 28d, an intermediate common electrode 28b and an inner common electrode 28a each of which is divided in the circumferential direction into six sections. The outer common electrode 28d carries indicia or marks M_1 to M_{12} formed thereon corresponding to positions of
10 1 o'clock to 12 o'clock.

Grooves 26c separating the adjacent sections of the common electrodes 28a, 28b are positioned between the tenth and eleventh segment electrodes 27a, twentieth and twenty-first segment electrodes, thirtieth and thirty-first segment electrodes, fortieth
15 and forty-first segment electrodes, fiftieth and fifty-first segment electrodes and sixtieth and first segment electrodes, respectively, counted in the clockwise direction.

The liquid crystal display device is constituted by an assembly of display sections including a liquid crystal material
20 interposed between the segment electrode arrangement of Figure 2 and the common electrode arrangement of Figure 3. Detailed description of the liquid crystal display device is omitted.

Figure 4 shows, in detail, the output conversion circuit 21 and the segment voltage supplying circuit 22 which are constituted

by analog switching circuits 44-53, AND gate circuits 29-38,
OR gate circuits 39-43 and inverters 54-58.

Figure 5 shows, in detail, the voltage selecting circuit
25 which is constituted by switching circuits 59 to 74 and
5 inverters 75, 76.

Figure 6 shows in detail the common voltage supplying
circuit 23 which is constituted by AND gate circuits 77-82,
switching circuits 83-92 and inverters 93-97.

Operation of the electronic timepiece shown in Figures 1A
10 and 1B will now be described. Referring to Figure 5, voltages
 v_0 , $2v_0$ and $3v_0$ are applied to terminals 13, 14; 12, 15; 10, 17
respectively. Further, a voltage 0 is applied to the terminals
11, 16. For ease of explanation it is assumed that the liquid
crystal display device produces no display when the voltage is
15 lower than $|v_0|$ and produces a display when the voltage is
higher than $|2v_0|$.

A pulse train shown by waveform A in Figure 7 is applied
to the terminal P_0 of Figure 5 so that the switching circuits
67, 69, 71, 73 and 68, 70, 72, 74 are opened and closed alternately.
20 On the other hand pulses shown by waveform A are generated at
the terminal Q of the flip-flop circuit 24 triggered by the
pulses generated at the terminal P_1 . In consequence, the switching
circuits 59, 61, 63, 65 and the switching circuits 60, 62, 64, 66
shown in Figure 5 are opened and closed alternately to produce
25 two voltages out of the four voltages 0, v_0 , $2v_0$, $3v_0$. Therefore

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pulse b_1 of the waveform B in Figure 7 is produced and the potential 0 is maintained at the terminal S_0 , while voltages $2v_0$ and 0, $3v_0$ and 0; v_0 and 0 and v_0 and $2v_0$ are generated alternately at the terminals S_1 , C_0 , C_1 and C_2 respectively. On the other hand if pulse b_2 is produced a voltage $3v_0$ is generated at the terminal S_0 and voltages v_0 and $3v_0$, 0 and $3v_0$, $2v_0$ and $3v_0$ and $2v_0$ and v_0 are alternately generated at terminals S_1 , C_0 , C_1 and C_2 respectively.

The operation of the electronic timepiece will be explained assuming a time of 10 o'clock, 5 minutes and zero seconds (exactly 5 past 10). In this state, the counters 3 to 9 are counting, respectively, 0, 0, 5, 0, 0, 5, 5.

As pulses are cyclically generated from the terminal P_1 of the timing pulse generating circuit 10 shown in Figure 1A, the gate circuits 11, 14 for units of seconds are opened, so that data in the counters 3, 4 concerning seconds is delivered to gate circuits 17, 18. Therefore, logic 0 is generated at terminals $2^0 - 2^2$ of the gate circuit 18 so that logic 1 and logic 0 are produced at terminals $\bar{h}$ and h respectively while logic 1 is produced at the terminal x_0 of the decoder 19.

Referring now to Figure 4, since the outputs from the gate circuits 29, 39 are logic 1, the potential generated at the terminal S_0 appears at the terminal e_1 . The potential generated at the terminal S_1 appears at other terminals $e_2 - 2_{10}$, because the switching circuits 47, 49, 51, 53 are OFF. With regard to the

decoder 20 shown in Figure 6, the voltage generated at the terminal C_0 appears at the terminal k_1 because logic 1 appears at the terminal y_0 . In this state, since the terminal P_3 of the timing pulse generating circuit 10 is logic 0 the terminal $\bar{P}_3$ is logic 1 so that the AND gate circuits 77-82 are open. Therefore, the switching circuit 83 is turned ON so that the voltage present at the terminal C_0 appears at terminal g_1 . The voltage present at the terminal C_1 appears at terminals $k_2 - k_6, g_2 - g_6$.

Therefore, a voltage differential $|3v_0|$ between the voltages applied to the terminals e_1 and g_1 is applied to the liquid crystal material periodically so that the display corresponds to the electrode S shown in Figure 2 which is turned ON. The voltage v_0 is periodically applied between other electrodes so that the display corresponding to those other electrodes is not produced.

Referring now to the terminal P_2 of the timing pulse generating circuit 10, a pulse periodically generated at terminal P_2 opens the gate circuits 12, 15 so that the output data "5" and "0" from the counters 5,6 passes therethrough. In consequence logic 1 appears at terminal x_5 of the decoder 19 and at terminal y_0 of the decoder 20. Moreover logic 1 and logic 0 are maintained at terminals $\bar{h}$ and h respectively.

In consequence, the output from the OR gate circuit 41 shown in Figure 4 is logic 1 so that the switching circuit 48 is turned ON to permit the voltages present at the terminal S_0 to appear at the terminal e_6 . The voltage present at the terminal S_1 appears at

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the terminals $e_1 - e_5$ and $e_7 - e_{10}$.

As will be seen from Figure 6 the voltage present at the terminal C_0 appears at the terminals g_1, k_1 while the voltage present at the terminal C_1 appears at the terminals $g_2 - g_6$ and

5 $k_2 - k_6$. Therefore the display corresponding to the electrode M shown in Figure 2 and connected to terminal e_6 and common electrodes opposed to the terminals g_1, k_1 produces a display.

Referring now to the terminal P_3 of the timing pulse generating circuit 10, the pulses periodically derived from this terminal open the gate circuits 13, 16 to permit the output from the counters 7, 8 to pass therethrough. In consequence, the voltage generated at the terminal S_0 appears at the terminal e_{10} of the segment voltage supplying circuit 22. Meanwhile, the voltage present at the terminal C_0 appears at the terminal k_6 of the common electrode supplying circuit 23, while the voltage present at the

15 terminal C_1 appears at the terminals $k_1 - k_5$ thereof. When a pulse is generated at the terminal P_3 , the output from the AND gate circuits 77 - 82 shown in Figure 6 is logic 0 so that the voltage present at the terminal C_1 appears at the terminals $g_1 - g_6$.

20 Therefore, the display corresponding to the electrode H connected to the terminal e_{10} and the common electrode connected to the terminal k_6 produces a display. Thus a display corresponding to the electrodes H, M, S are produced i.e. a display of 10 hours 5 minutes and 0 seconds.

25 Hereinafter a description will be made as to the display of

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a graduated time scale. Terminals m_1 to m_6 of the common electrode 28d shown in Figure 3 are connected in common to the terminal C_2 shown in Figure 5. As stated already, the voltages v_0 and $2v_0$ are generated at the terminal C_2 at the half period of the pulse output from the terminal Q of the flip-flop circuit 24, and voltages $2v_0$ and v_0 are formed in the next half period of output pulse from the terminal Q. On the other hand, at the terminal S_0 the voltage 0 and $3v_0$ are formed in the earlier half and later half periods of the output pulse from the terminal Q. Further, voltages $2v_0$, 0 and voltages v_0 , $3v_0$ are formed at the terminal S_1 , in the earlier and later half periods of the output pulse. In consequence, a voltage $|2v_0|$ is supplied between the segment electrode and the common electrode 28d irrespective of whether this segment electrode is selected to produce a display or not so that the display between the common electrode 28d and the segment electrodes is continuously produced to indicate time graduations of a graduated time scale.

Figure 8 illustrates the time display of the electronic timepiece of Figures 1A and 1B. The numerals around the graduations may be provided by printing or by means of a liquid crystal display device.

Figures 9 and 12 illustrate another embodiment of an electronic timepiece according to the present invention.

Figure 9 shows a circuit interposed between the output

conversion circuit 21 shown in Figures 1A and 1B and the segment voltage supplying circuit 22. An inverter 98 inverts the output level derived from the output conversion circuit 21. The gate circuits 99, 100 have AND functions, while the gate circuit 101 has an OR function.

Figure 10 shows a modification of the common electrode voltage supplying circuit 23. Gate circuits 102, 103 have AND functions. A reference numeral 104 denotes a circuit constituted by switching circuits 83-88 and inverters 93-95 as shown in Figure 6, while reference numeral 105 denotes a circuit constituted by switching circuits 89-92 and inverters 95-97. Reference numeral 106 denotes a common voltage supplying circuit for the common electrode 28d which is constituted by switching circuits 107-114 and inverters 115-118 as shown in Figure 11.

Figure 12 is a detailed circuit diagram of the voltage selecting circuit. This voltage selecting circuit is constituted by switching circuits 119-134 and inverters 135, 136.

In this embodiment the hours and minutes indications are produced in the same manner as previously described and a seconds indication is produced as follows.

The units of seconds is selected when a pulse is generated at a terminal P of the timing pulse generating circuit 10 shown in Figure 1A. As this pulse is generated the gate circuit 99 (Figure 9) is opened so that the inverted logical level of seconds data is delivered to the segment voltage supplying circuit 22

through the gate circuit 101. Therefore, a voltage corresponding to non-display, i.e. the voltage generated at the terminal S_1 , is applied to the terminal of the segment electrode which should produce a display according to the data. On the other hand the voltage corresponding to the display, i.e. the voltage generated at the terminal S_0 , is applied to the terminals of the segment electrodes which should not produce a display according to the data. Meanwhile, the switching circuits 111, 113 shown in Figure 11 are opened by the pulse from the terminal P_1 . Also the voltage present at the terminal C_0 appears at the output of the switching circuit connected to terminal y_k at which the displaying output from the decoder 20 is derived, while the voltage present at the terminal C_2 is generated at the outputs of other switching circuits. Therefore, as far as the output to be displayed is concerned, the voltage present at the terminal C_0 is generated at the terminal m_k , while, in the case of the outputs which should not be displayed, the voltage present at the terminal C_2 appears at terminals m_n ($n = 1$ to 6). In consequence, the voltage present at the terminal C_0 shown in Figure 12 and the voltage present at the terminal S_1 are applied to the common electrode 28d for display of seconds (Figure 3) and to the segment electrode (Figure 2), so that voltages $|v_0|$ and 0 are periodically applied. Therefore, the graduated time scale to which these voltages are applied do not produce a display while other display sections receives voltages $3|v_0|$ and $|v_0|$ to produce a display. Consequently, the graduations

of the graduated time scale are so energised to indicate the elapse of seconds.

5 As described above a graduated time scale is formed as an electro-optical display device which represents the shape of the pointer or hands so that the necessity for adjustment of graduations is completely eliminated. In addition, since the variation of apparent position of the pointer or hands in relation to the graduations due to variation of angle or direction of observation is avoided, erroneous reading of the time indication
10 does not take place. Further, the present invention offers an additional advantage that the graduated time scale can be used for displaying seconds information.



CLAIMS

1. An electronic timepiece comprising: a display device comprising a plurality of segment electrodes having elongate sections which are arranged in a generally circular array, a plurality of common electrodes of sector-like shape arranged in three concentric rings of electrode units with each sector-like electrode being spaced from and opposing a group of an equal number of the segment electrodes to define therewith display elements; first means defining circuit paths connecting corresponding ones of the segment electrodes in each of the groups of segment electrodes, a display medium disposed between the segment electrodes and the common electrodes, the electrode units of the outer one of the three concentric rings of electrode units having radially projecting indicia parts spaced at regular intervals in a circumferential direction thereof, the segment electrodes which are opposed to the indicia parts being formed longer by a length of the indicia parts than the remaining segment electrodes; second means for producing time information corresponding to at least hours and minutes; and third means for causing the display elements comprising two of said concentric rings of electrode units except for the outer concentric ring of electrode units and the segment electrodes opposed to them to display the time information and for causing the display elements comprising said outer concentric ring of electrode units and the segment electrodes opposed to it to display the graduated time scale.



2. An electronic timepiece as claimed in claim 1 including fourth means for producing a plurality of pulse trains each of which has voltages selected from among a plurality of predetermined voltages having different values, fifth means for applying at least one of the pulse trains for display to the segment electrodes of the display elements to be displayed in response to the time information and the segment electrodes electrically connected thereto, and for applying at least one of the pulse trains for non-display to the remaining segment electrodes, and sixth means for applying to the common electrodes of some of the display elements at least one of the pulse trains having voltage values and phase relations effective to cause the display elements to display time information and for applying to the common electrodes of the remaining display elements at least one of the pulse trains having voltage values and phase relations ineffective to cause the remaining display elements to display time information.

3. An electronic timepiece as claimed in claim 2 in which the fourth means is arranged to produce predetermined voltages having values of 0, V_0 , $2V_0$ and $3V_0$.

4. An electronic timepiece as claimed in claim 2 or 3 including seventh means for applying to other ones of the common electrodes of the display elements at least one of the pulse trains having voltage values and phase relations effective to cause the display of graduation display elements in turn at one second periods in response to the seconds time information.

5. An electronic timepiece substantially as herein described with reference to and as shown in the accompanying drawings.