

ABSTRACT OF THE DISCLOSURE

An interface circuit of a memory device including a plurality of memory dies including a plurality of registers corresponding to the plurality of memory dies, respectively, the plurality of registers each configured to store command information related to a data operation command, a demultiplexer circuit configured to provide input command information to a selected register from among the plurality of registers according to at least one of a first address or a first chip selection signal, the input command information being received from outside the interface circuit, and a multiplexer circuit configured to receive output command information from the selected register from among the plurality of registers and output the output command information according to at least one of a second address or a second chip selection signal may be provided.

FIG. 4