ABSTRACT

MEMORY CELL WITH STORED CHARGE ON ITS GATE

A memory cell with a stored charge on its gate comprising; (A) a channel forming region, (B) a first gate formed on an insulation layer formed on the surface of the channel forming region, the first gate and the channel forming region facing each other through the insulation layer, (C) a second gate capacitively coupled with the first gate, (D) source/drain regions formed in contact with the channel forming region, one source/drain region being spaced from the other, (E) a first non-linear resistance element having two ends, one end being connected to the first gate, and (F) a second non-linear resistance element composed of the first gate, the insulation layer and either the channel-forming region and at least one of the source/drain regions.

FIGURE 1A