Claims

What is claimed:

1. A semiconductor device, comprising:

a semiconductor die including a notch formed in an edge of an active surface of the semiconductor die;

an encapsulant deposited around the semiconductor die and into the notch with a surface of the encapsulant that is coplanar with the active surface of the semiconductor die; and

a fan-in interconnect structure formed over the semiconductor die.

2. The semiconductor device of claim 1, wherein a back surface of the semiconductor die is coplanar with a surface of the encapsulant.

3. The semiconductor device of claim 2, further including a backside protection layer formed over the back surface of the semiconductor die.

4. The semiconductor device of claim 1, wherein the encapsulant covers a sidewall of the semiconductor die with a thickness of less than 50 micrometers (μm) and greater than zero μm .

5. The semiconductor device of claim 1, wherein the fan-in interconnect structure includes one or more conductive layers with each of the conductive layers limited to within a footprint of the semiconductor die.

6. The semiconductor device of claim 1, wherein the notch includes a step cut.

7. A semiconductor device, comprising:

a semiconductor die including an active surface and a notch formed in an edge of the active surface;

an encapsulant disposed around the semiconductor die and in the notch, wherein a surface of the encapsulant is coplanar with the active surface; and

a fan-in interconnect structure contained completely within a footprint of the semiconductor die.

8. The semiconductor device of claim 7, wherein a back surface of the semiconductor die is exposed from the encapsulant.

9. The semiconductor device of claim 8, further including a backside protection layer formed over the back surface of the semiconductor die.

10. The semiconductor device of claim 7, wherein the semiconductor die is disposed over a standardized carrier.

11. The semiconductor device of claim 7, wherein the notch includes a step cut.

12. A semiconductor device, comprising:

a semiconductor die including a notch formed in an edge of an active surface of the semiconductor die;

an encapsulant deposited around the semiconductor die and into the notch with a surface of the encapsulant that is coplanar with the active surface of the semiconductor die; and

a fan-in interconnect structure formed over the semiconductor die, wherein the fan-in interconnect structure is contained completely within a footprint of the semiconductor die.

13. The semiconductor device of claim 12, wherein a back surface of the semiconductor die is coplanar with a surface of the encapsulant.

14. The semiconductor device of claim 13, further including a backside protection layer formed over the back surface of the semiconductor die.

15. The semiconductor device of claim 12, wherein the encapsulant covers a sidewall of the semiconductor die with a thickness of less than 50 micrometers (μm) and greater than zero μm .

16. The semiconductor device of claim 12, wherein the semiconductor die extends outside a footprint of the fan-in interconnect structure.

17. The semiconductor device of claim 12, wherein the notch is disposed outside a footprint of the fan-in interconnect structure.

18. The semiconductor device of claim 12, wherein the notch includes a step cut.

19. A semiconductor device, comprising:

a semiconductor die including a notch formed in an edge of an active surface of the semiconductor die;

an encapsulant deposited around the semiconductor die and into the notch with a surface of the encapsulant that is coplanar with the active surface of the semiconductor die;

a fan-in interconnect structure formed over the semiconductor die; and

a passivation layer formed over the fan-in interconnect structure, wherein the passivation layer contacts the encapsulant.

20. The semiconductor device of claim 19, wherein a back surface of the semiconductor die is exposed from the encapsulant.

21. The semiconductor device of claim 20, further including a backside protection layer formed over the back surface of the semiconductor die.

22. The semiconductor device of claim 19, wherein the semiconductor die is disposed over a standardized carrier.

23. The semiconductor device of claim 19, wherein the fan-in interconnect structure is contained completely within a footprint of the semiconductor die.

24. The semiconductor device of claim 19, wherein the notch includes a step cut.