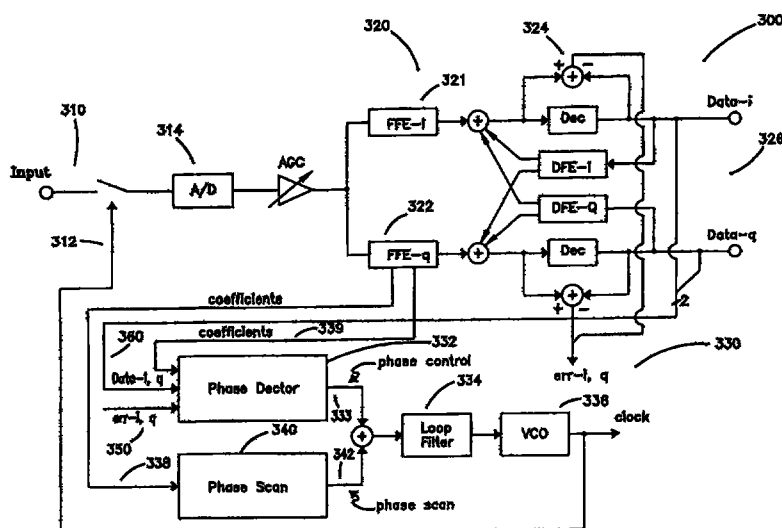




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04L 7/02	A1	(11) International Publication Number: WO 98/39873 (43) International Publication Date: 11 September 1998 (11.09.98)
(21) International Application Number: PCT/US98/04179 (22) International Filing Date: 4 March 1998 (04.03.98) (30) Priority Data: 60/039,802 4 March 1997 (04.03.97) US 09/033,769 3 March 1998 (03.03.98) US (71) Applicant: LEVEL ONE COMMUNICATIONS, INC. [US/US]; 9750 Goethe Road, Sacramento, CA 95827 (US). (72) Inventors: TAKATORI, Hiroshi; 932 South Beach Drive, Sacramento, CA 95831 (US). LING, Stanley, K.; 1040 Fulton Avenue #6, Sacramento, CA 95825 (US). GAT- TANI, Amit; 2356 American River Drive #A, Sacramento, CA 95825 (US). CAMAGNA, John, R.; 469 Bancraft Drive, El Dorado Hill, CA 95762 (US). (74) Agent: SHARP, Janice, A.; Merchant, Gould, Smith, Edell, Welter & Schmidt, Suite 400, 11150 Santa Monica Boule- vard, Los Angeles, CA 90025 (US).		(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Burasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). Published With international search report.

(54) Title: APPARATUS AND METHOD FOR PERFORMING TIMING RECOVERY



(57) Abstract

A timing recovery circuit is disclosed that prevents phase error over-compensation. The timing recovery circuit includes a phase scanner for determining when phase error over-compensation has occurred and generating a signal for preventing dual phase compensation in response thereto, thereby providing an accurate recovered clock signal. The timing recovery circuit also includes a feed-forward equalizer having a plurality of taps providing coefficients for filtering and adapting the input timing recovery circuit to an input signal. The phase scanner compares the tap coefficients to generate signal for preventing phase over-compensation by the feed-forward equalizer. A phase detector is provided for sampling coefficients from the feed-forward equalizer, error signals and output data and generating a phase signal used to generating the recovered clock signal. The signal for preventing phase over-compensation is mixed with the phase signal to generate the recovered clock signal.