Figure 1 Multi-Level Interconnection Architecture I

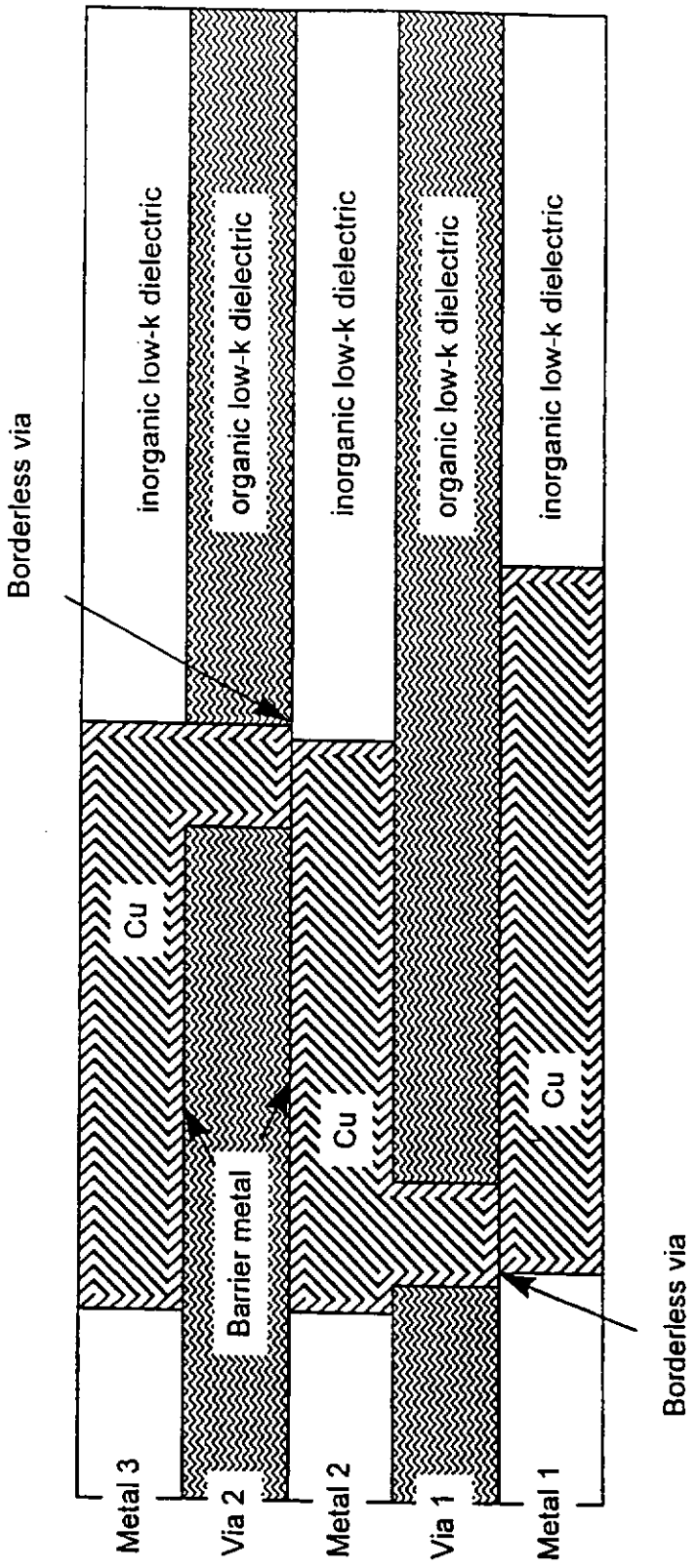


Figure 2 Multi-Level Interconnection Architecture II

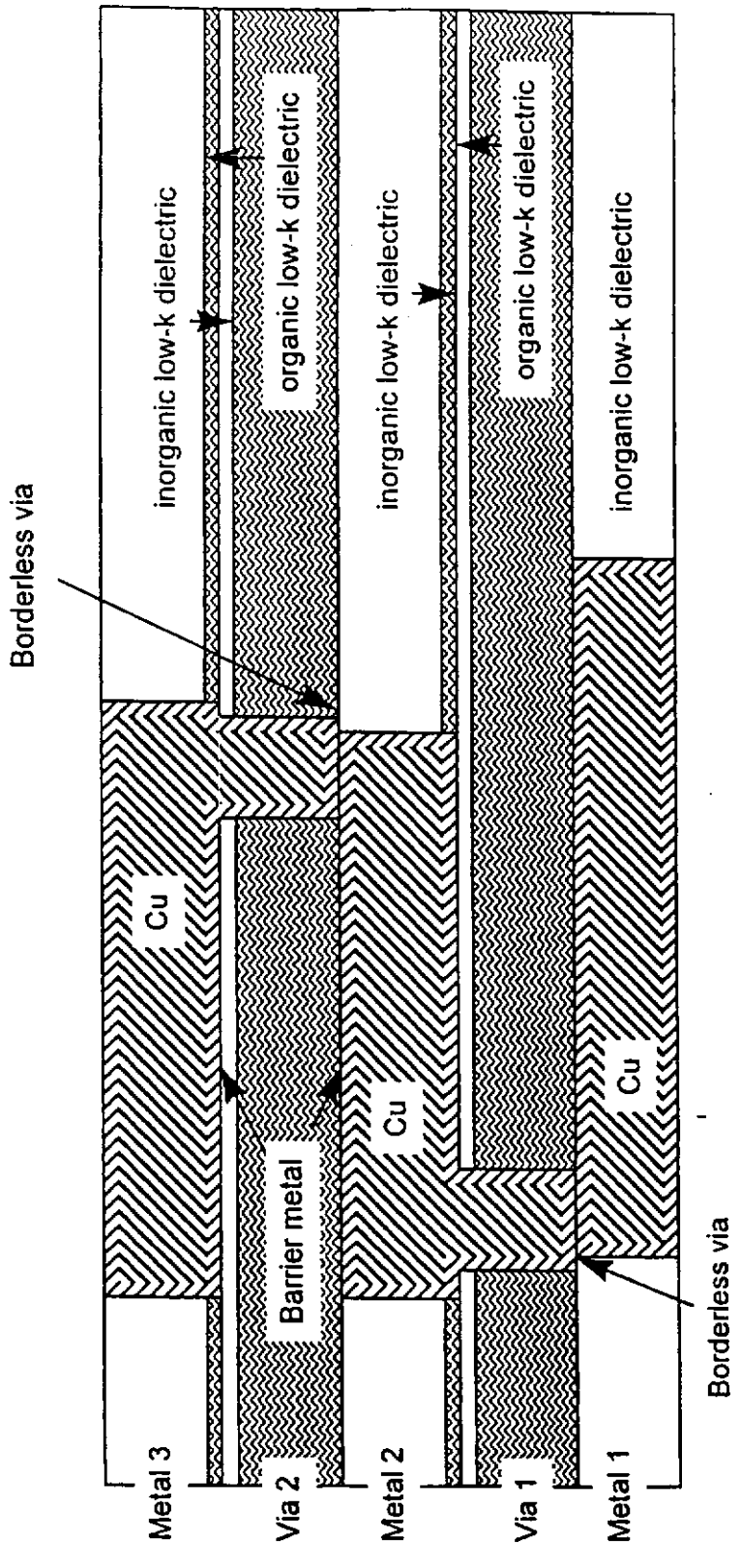
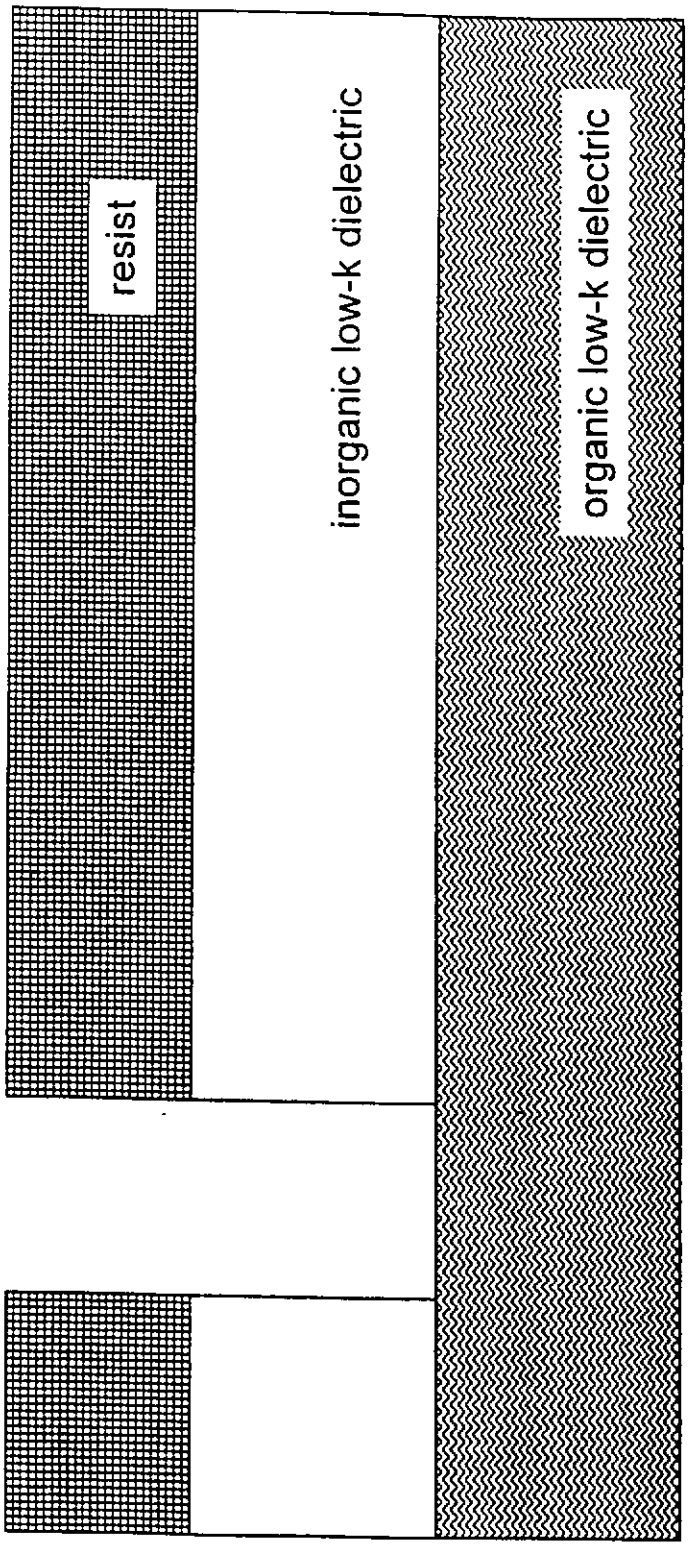


Figure 3

Step 1 Organic low-k dielectric deposition
Step 2 Inorganic low-k dielectric deposition
Step 3 Resist spin and bake

Figure 4
Step 4 Via mask and resist development
Step 5 Metal trench inorganic low-k dielectric etch



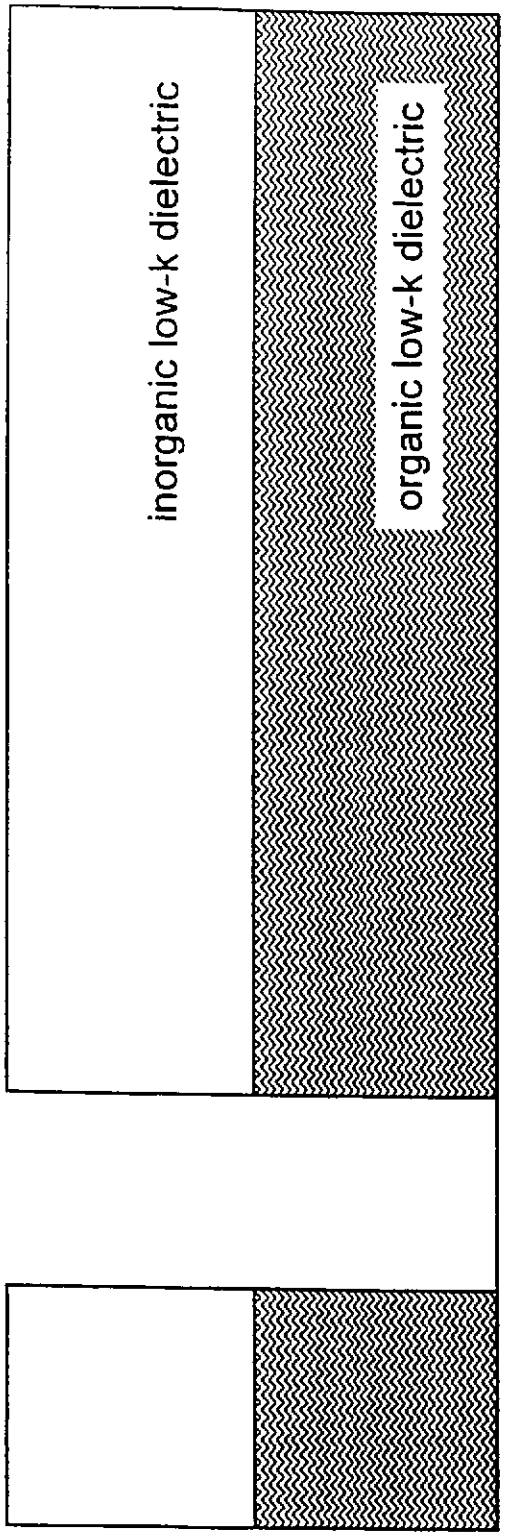
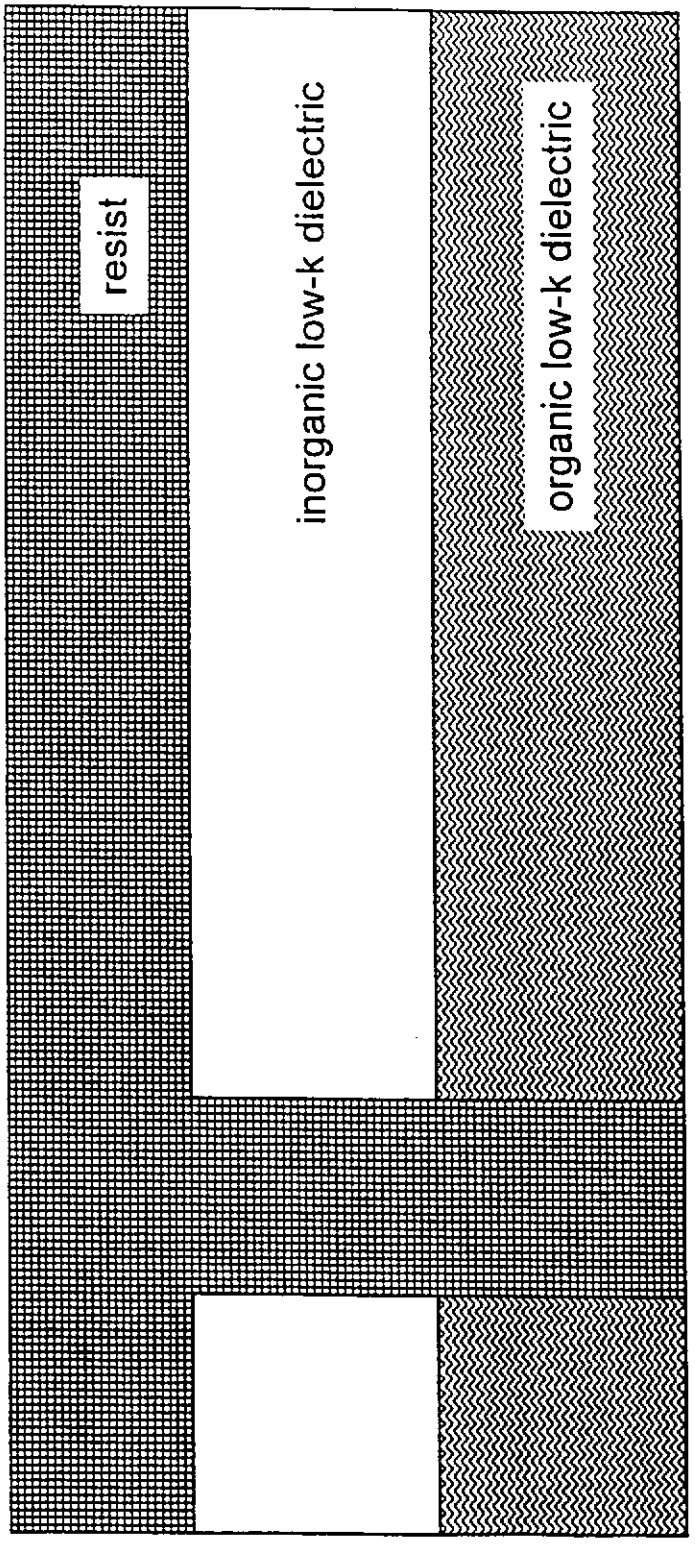


Figure 5
Step 6 Via organic low-k dielectric etch

Figure 6

Step 7 Resist spin and bake



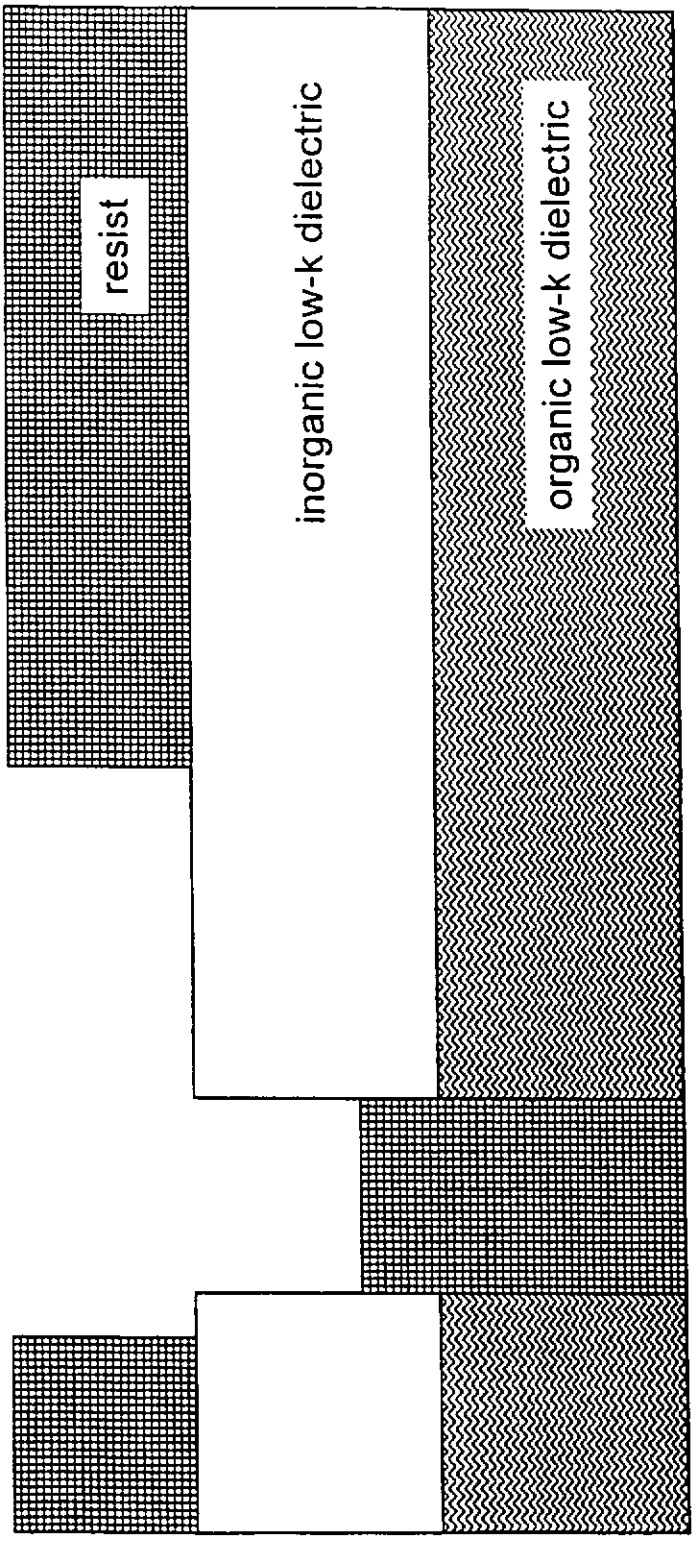


Figure 7
Step 8 Metal trench mask and resist development

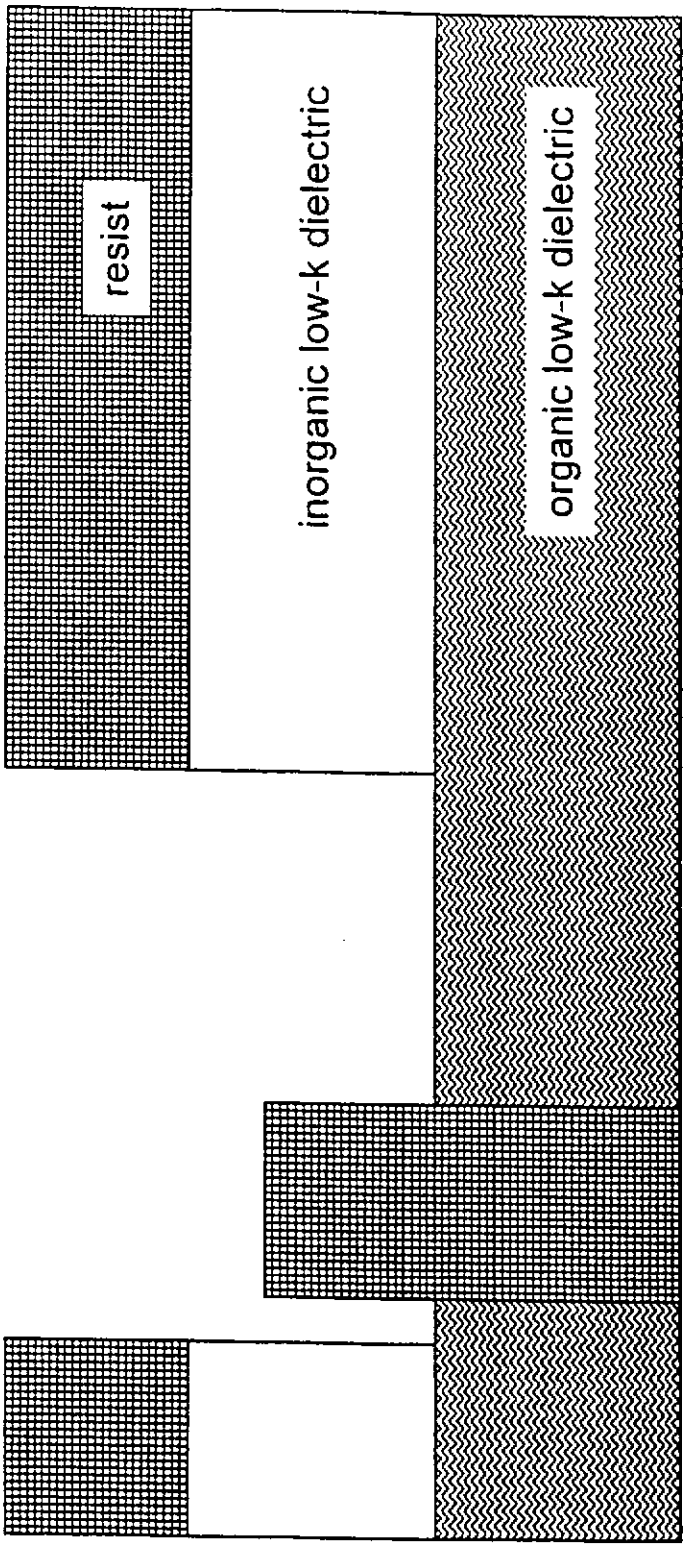


Figure 8
Step 9 Inorganic low-k dielectric etch

Figure 9

Step 10 Selective removal of resist

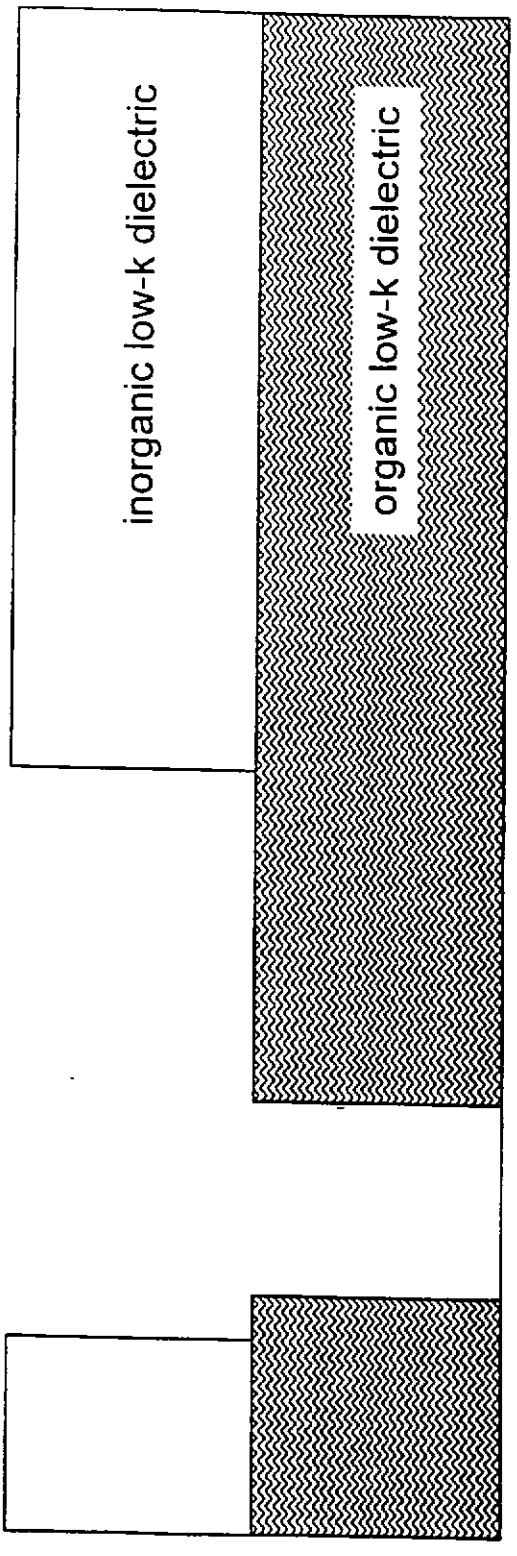


Figure 10

Step 11 Cu interconnect processing

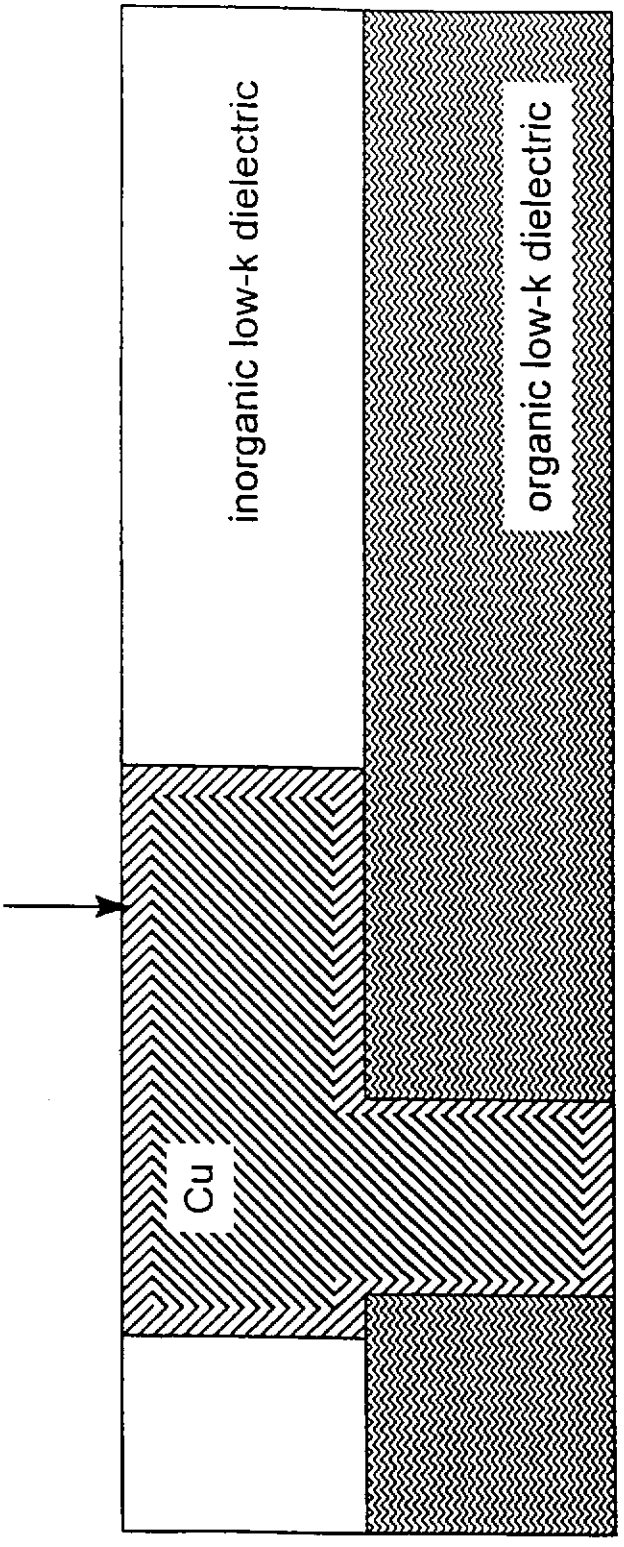


Figure 11

Step 1 Organic low-k dielectric deposition
Step 2 Inorganic low-k dielectric deposition
Step 3 Resist spin and bake

Figure 12

Step 4 Via mask and resist development
Step 5 Inorganic low-k dielectric etch

Figure 13

Step 6 Resist removal

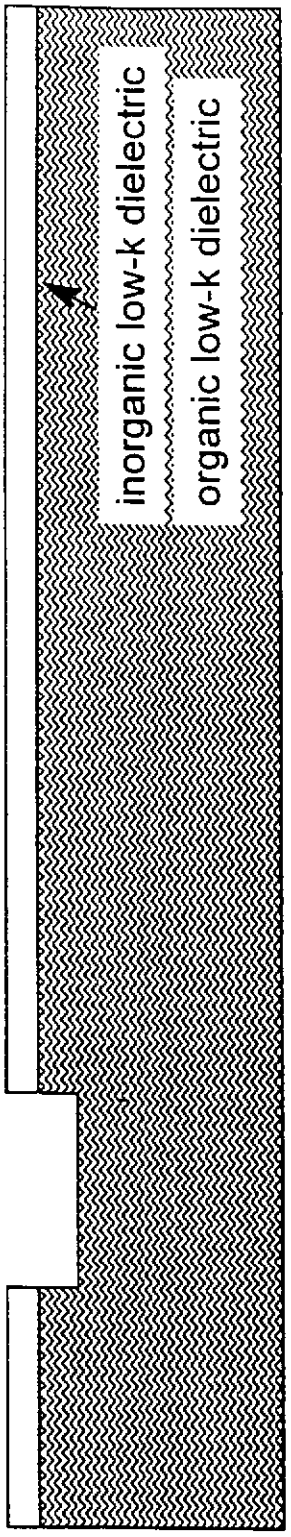


Figure 14

Step 7 Organic low-k dielectric deposition
Step 8 Inorganic low-k dielectric deposition
Step 9 Resist spin and bake
Step 10 Metal trench mask and resist development

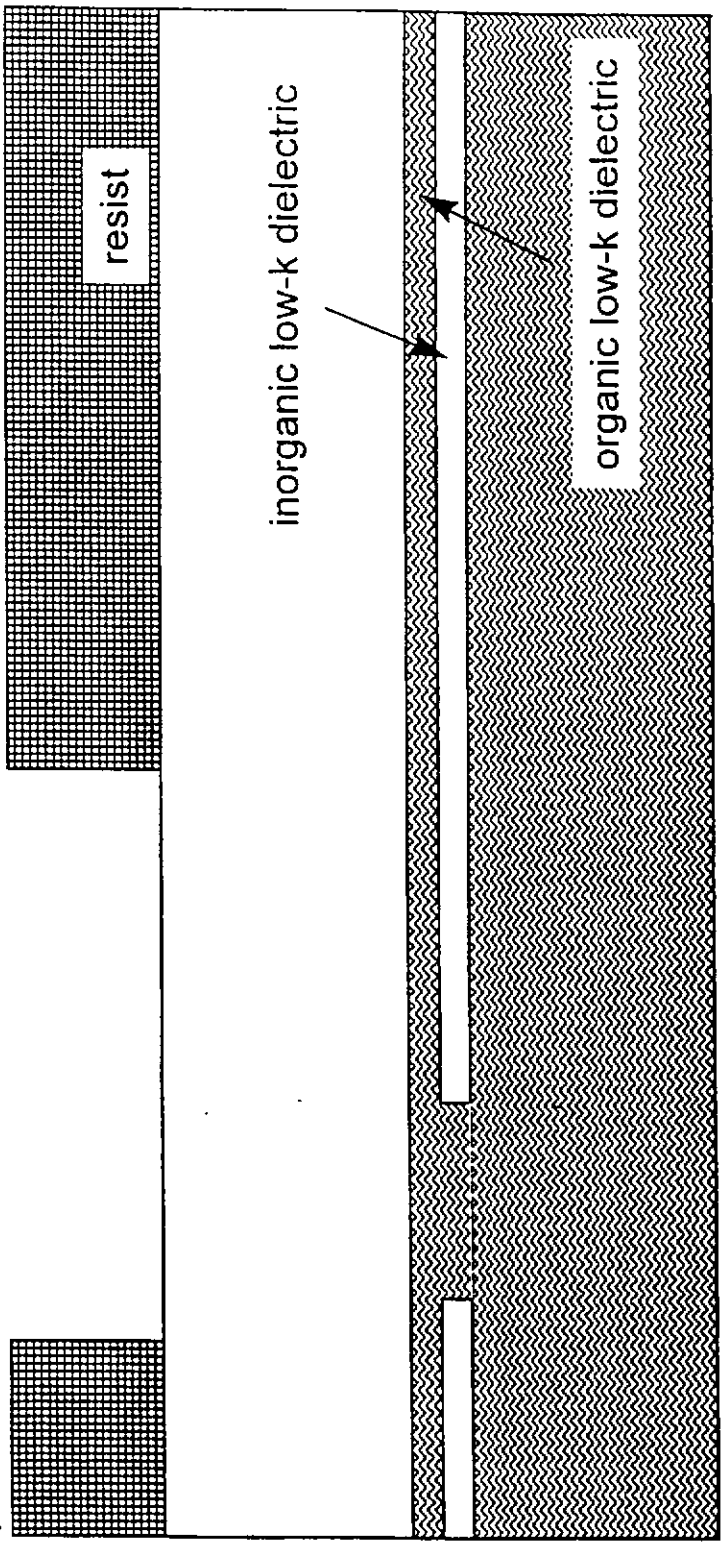


Figure 15

Step 11 Inorganic low-k dielectric etch

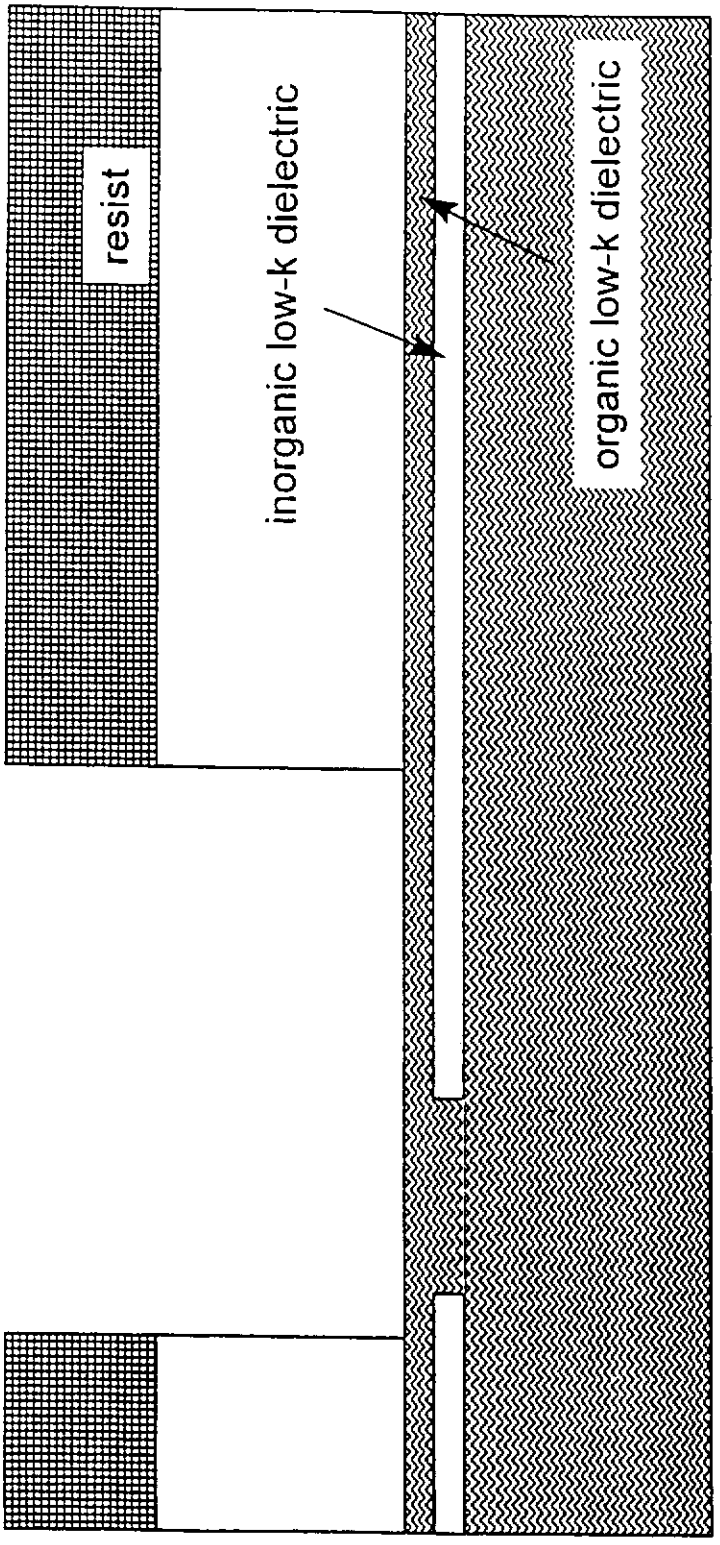
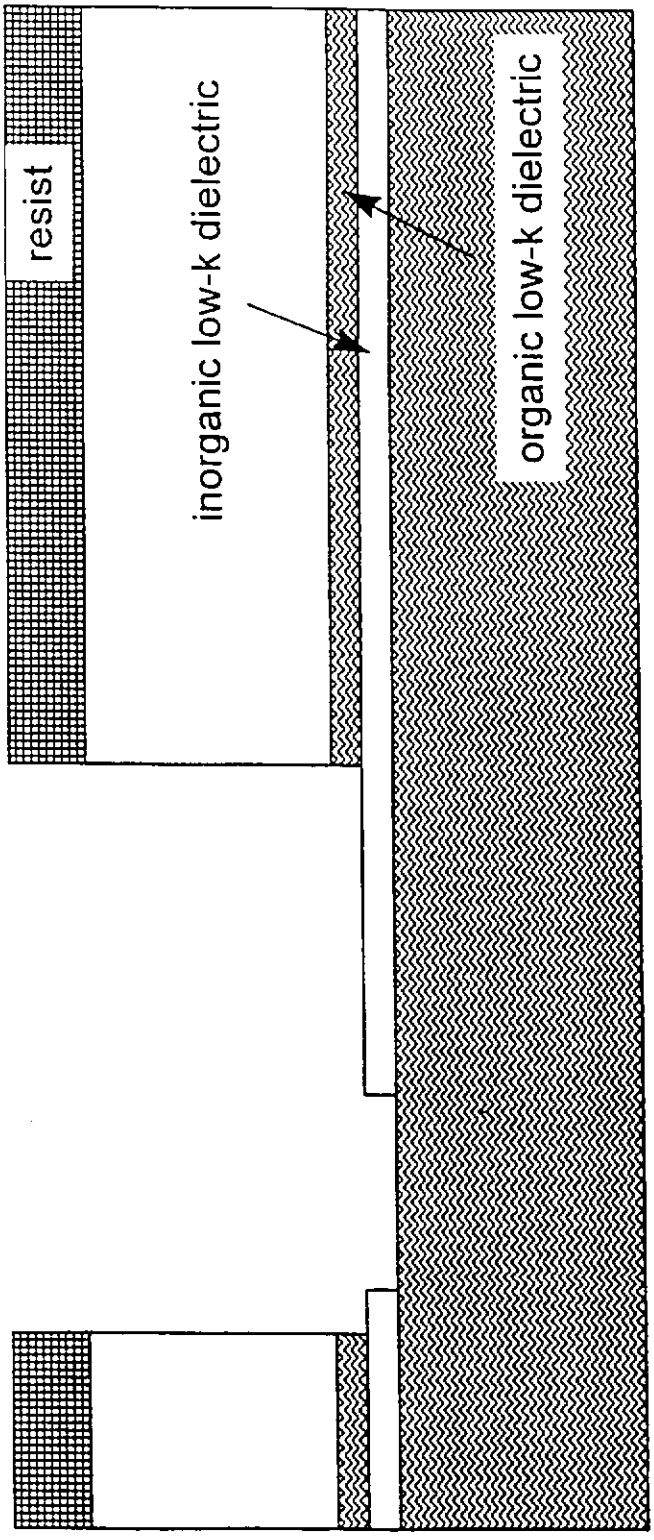


Figure 16

Step 12 Organic low-k dielectric etch



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Figure 17

Step 13 Organic low-k dielectric etch

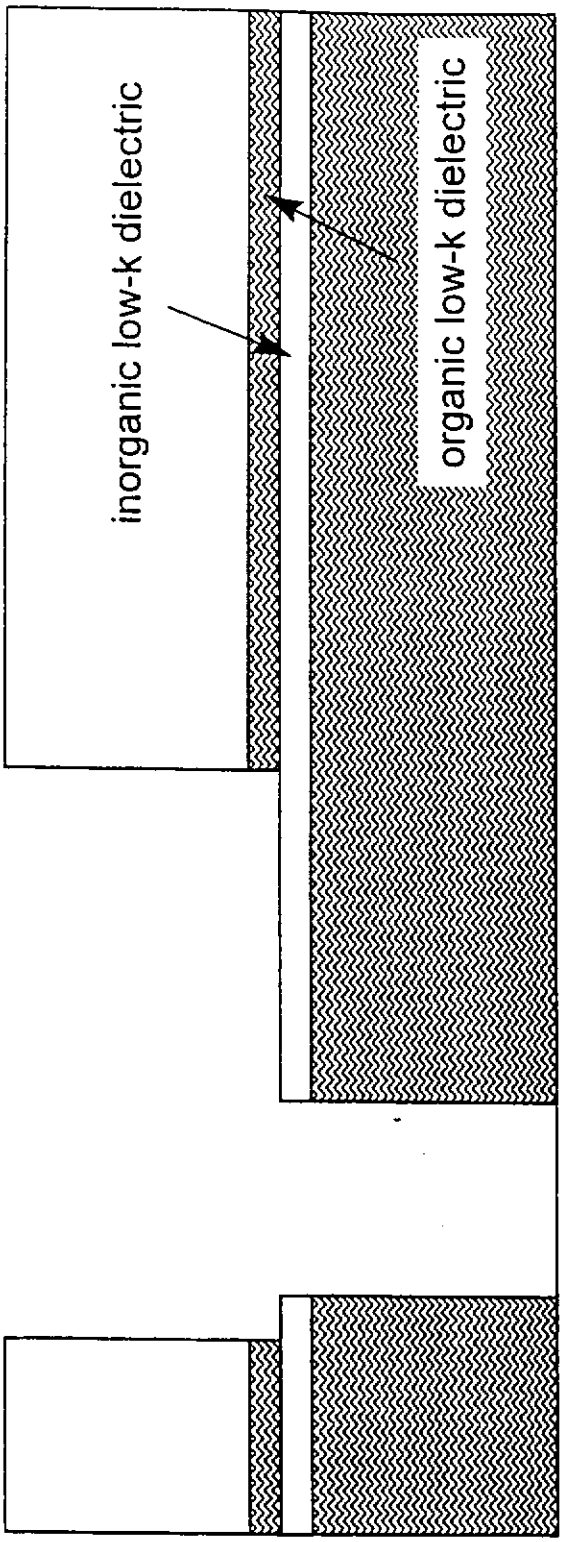


Figure 18

Step 14 Cu interconnect processing

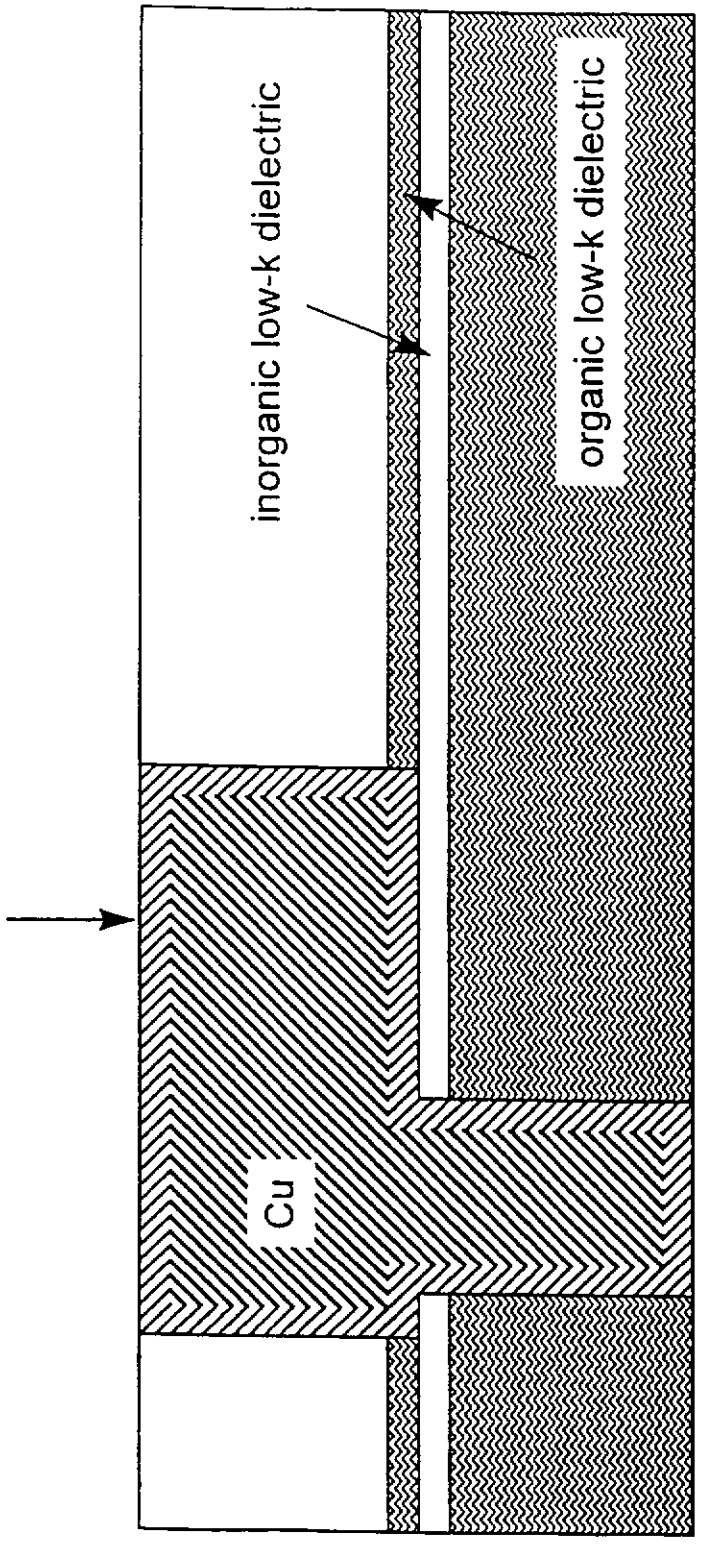


Figure 19

Step 1 Organic low-k dielectric deposition
Step 2 Inorganic low-k dielectric deposition
Step 3 Organic low-k dielectric deposition
Step 4 Inorganic low-k dielectric deposition
Step 5 Resist spin and bake

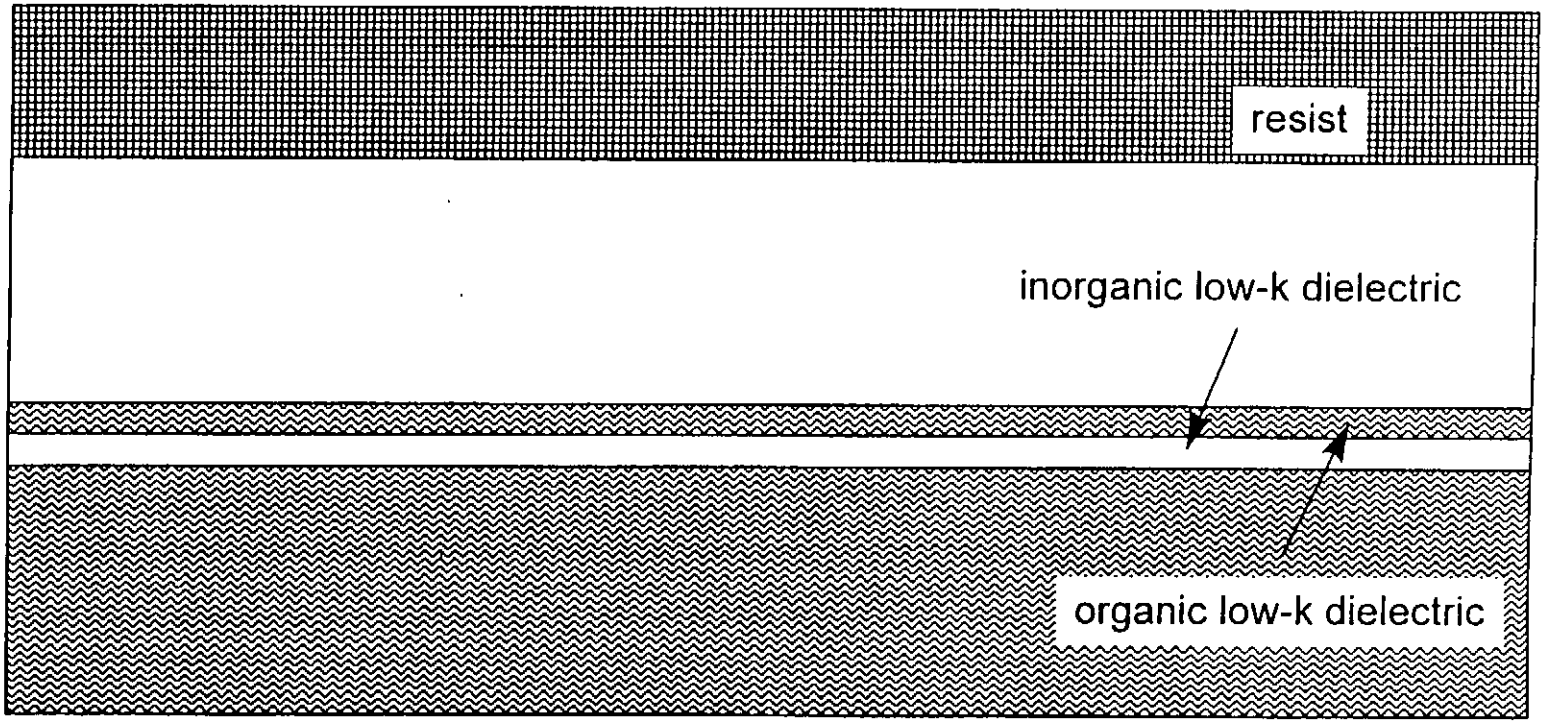
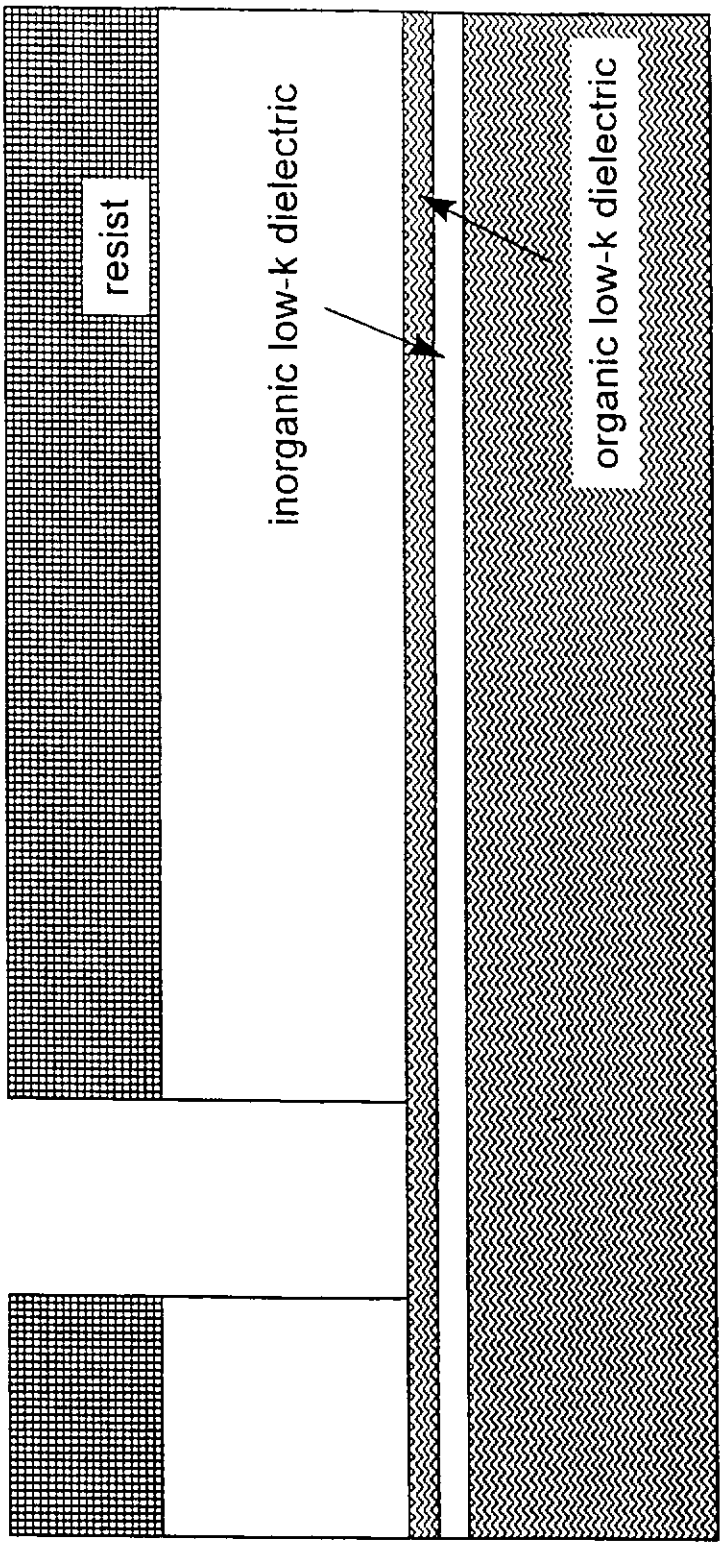


Figure 20

Step 6 Via mask and resist development
Step 7 Inorganic low-k dielectric etch



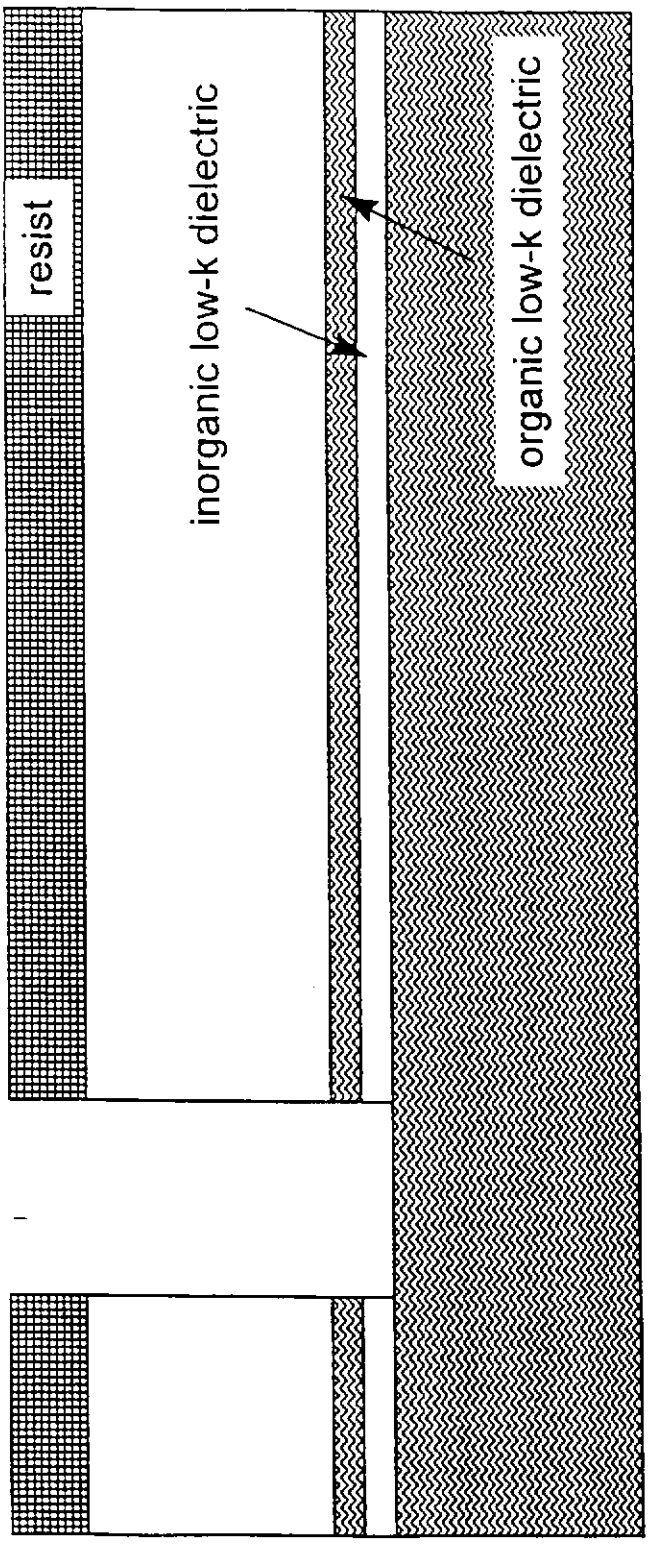


Figure 21

Step 8 Organic low-k dielectric etch
Step 9 Inorganic low-k dielectric etch

Figure 22

Step 10 Selective resist removal

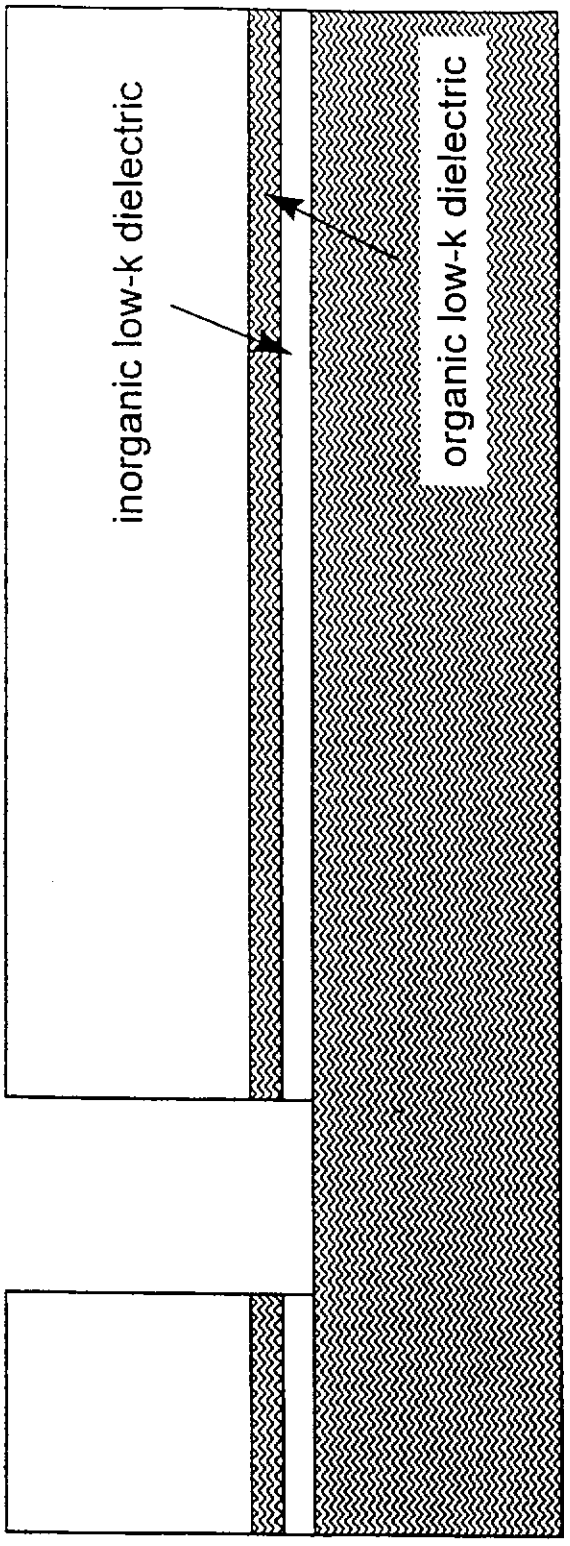


Figure 23

Step 11 Resist spin and bake

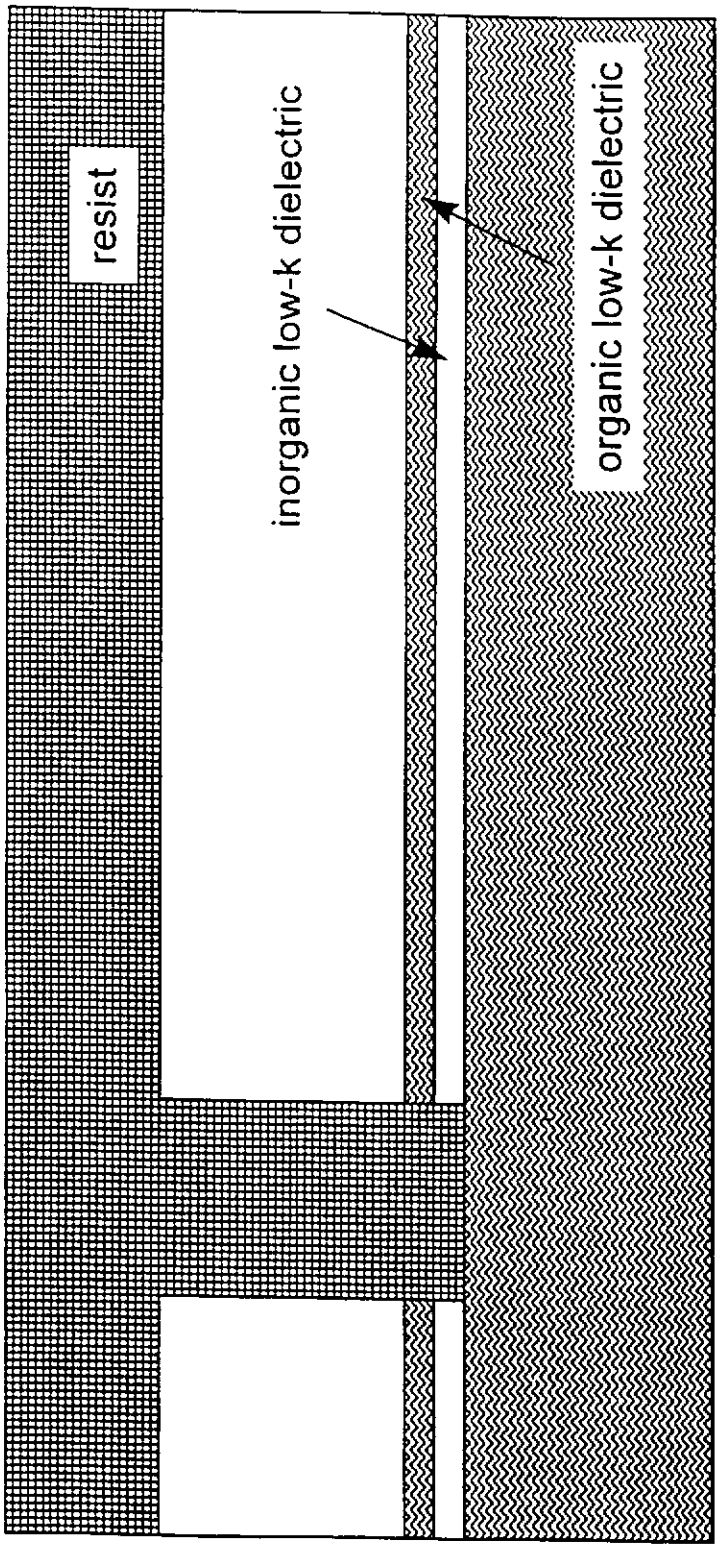


Figure 24

Step 12 Metal trench mask and resist development

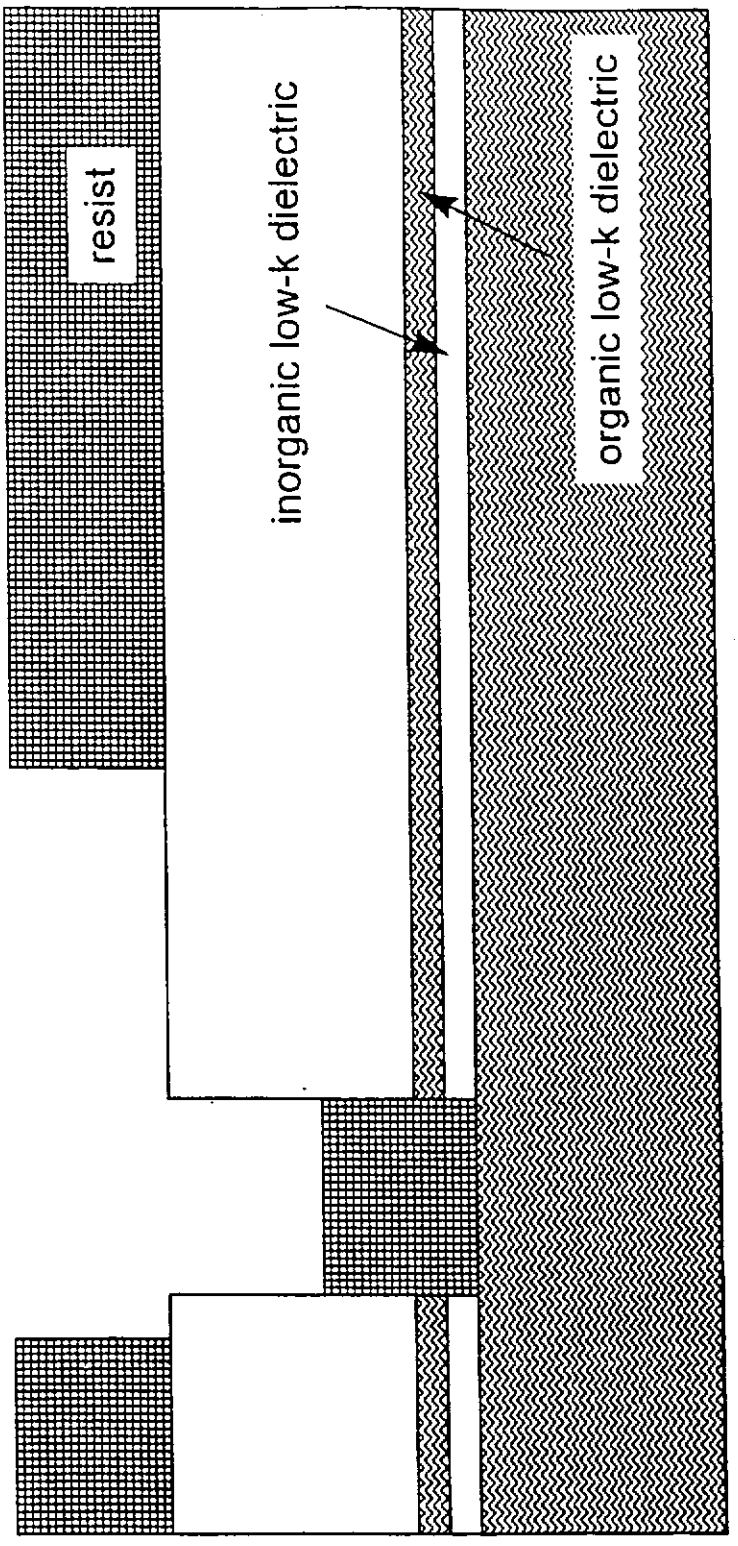


Figure 25

Step 13 Inorganic low-k dielectric etch

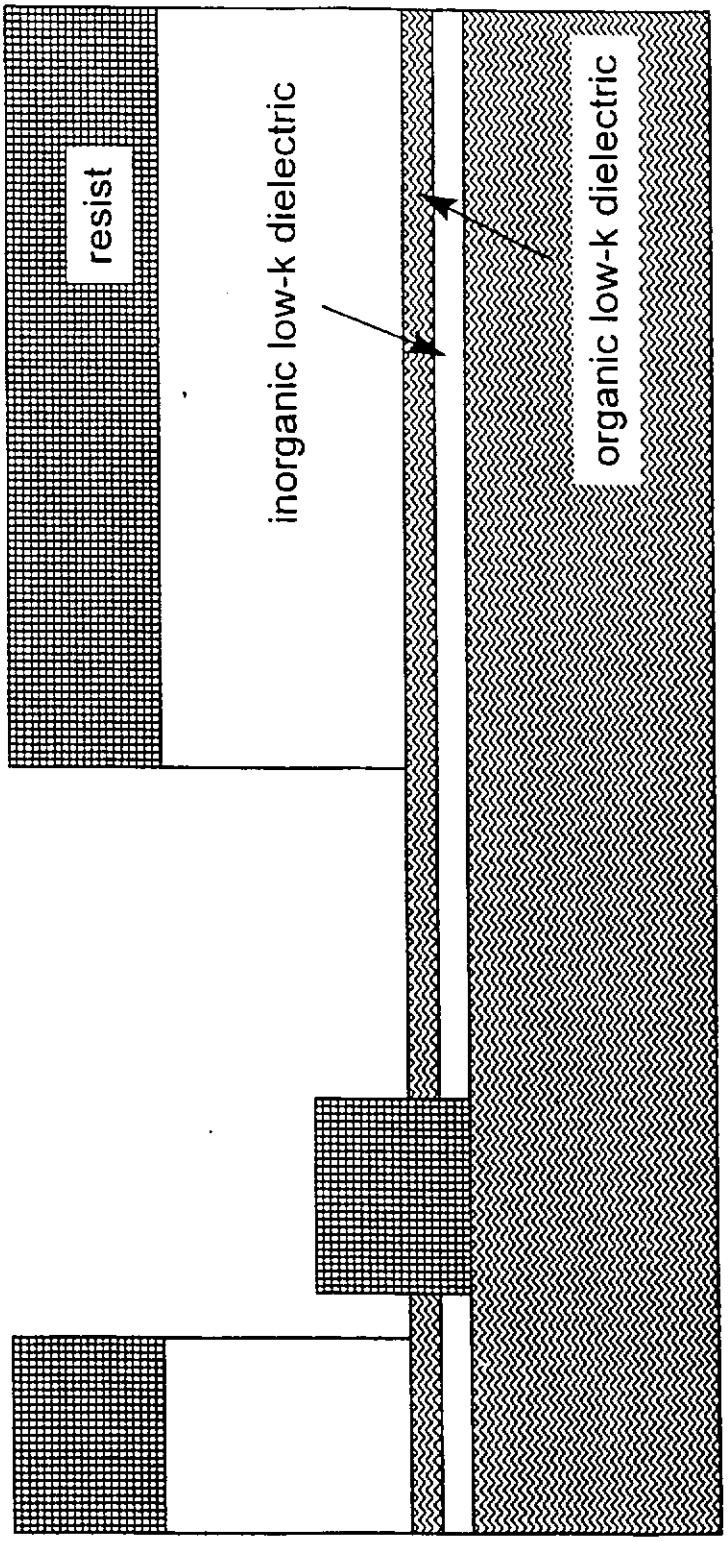


Figure 26

Step 14 Organic low-k dielectric etch

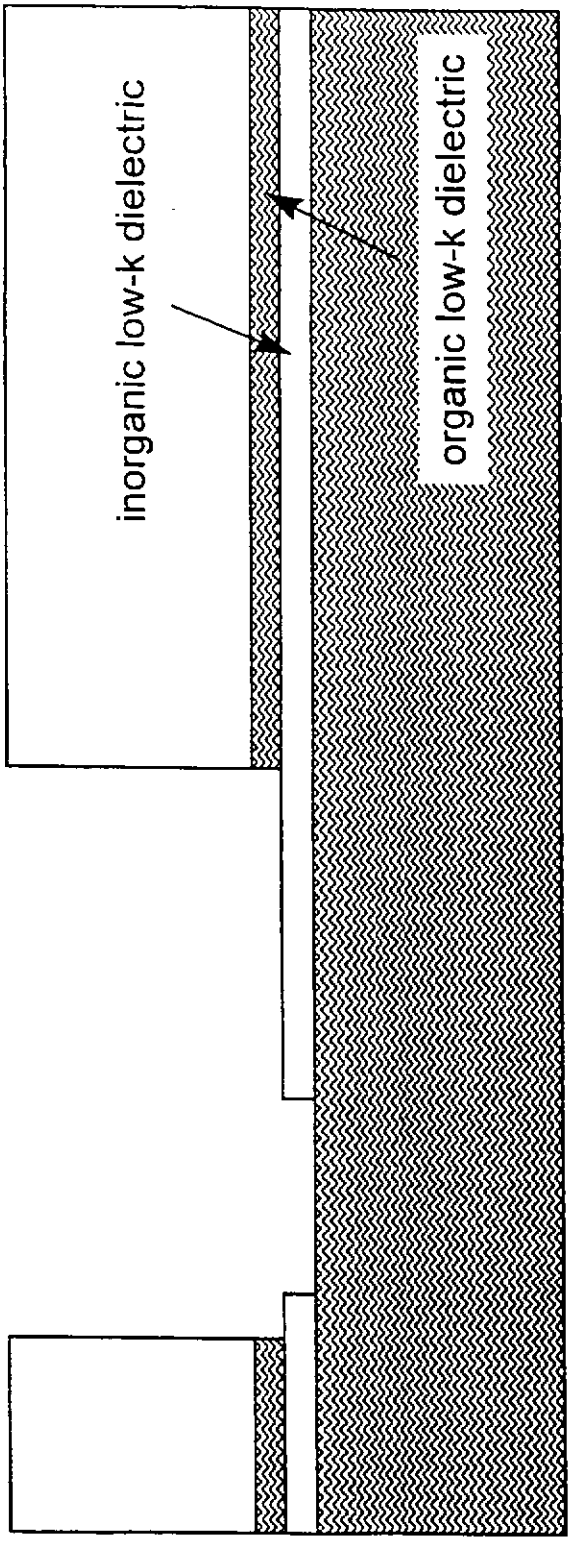
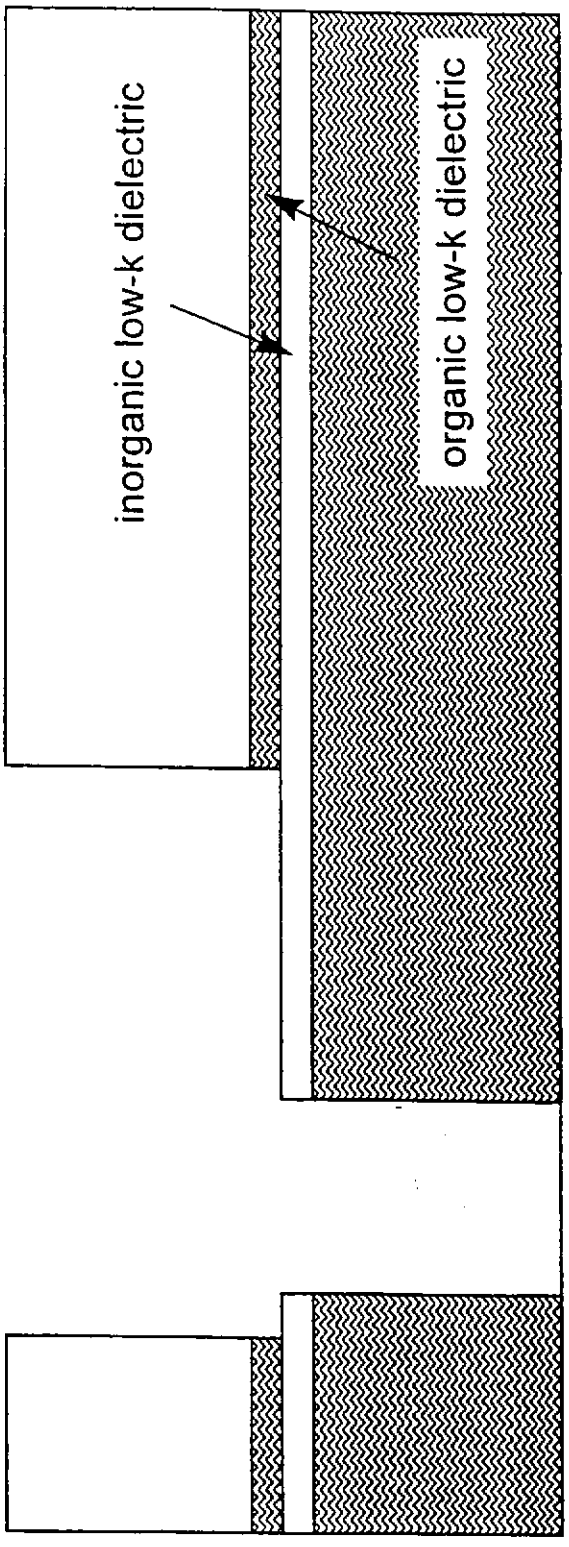


Figure 27

Step 15 Via inorganic low-k dielectric etch



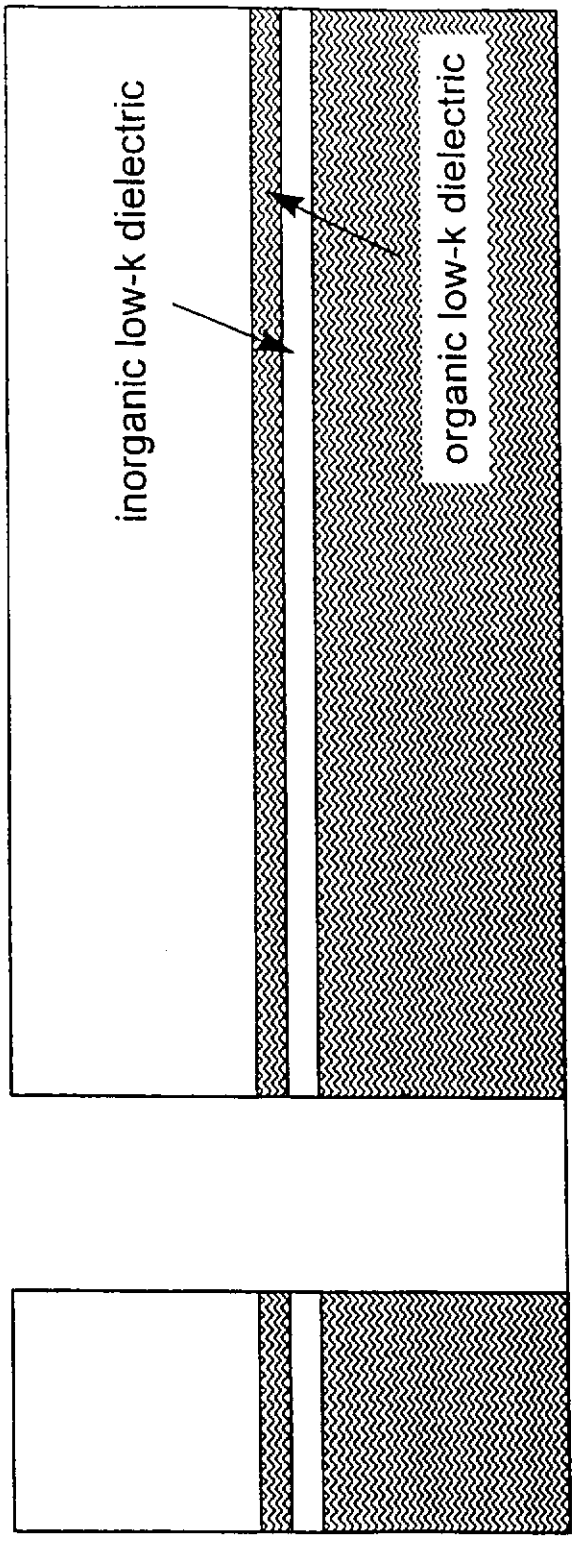


Figure 28

Step 10 Organic low-k dielectric etch

Figure 29

Step 11 Resist spin and bake

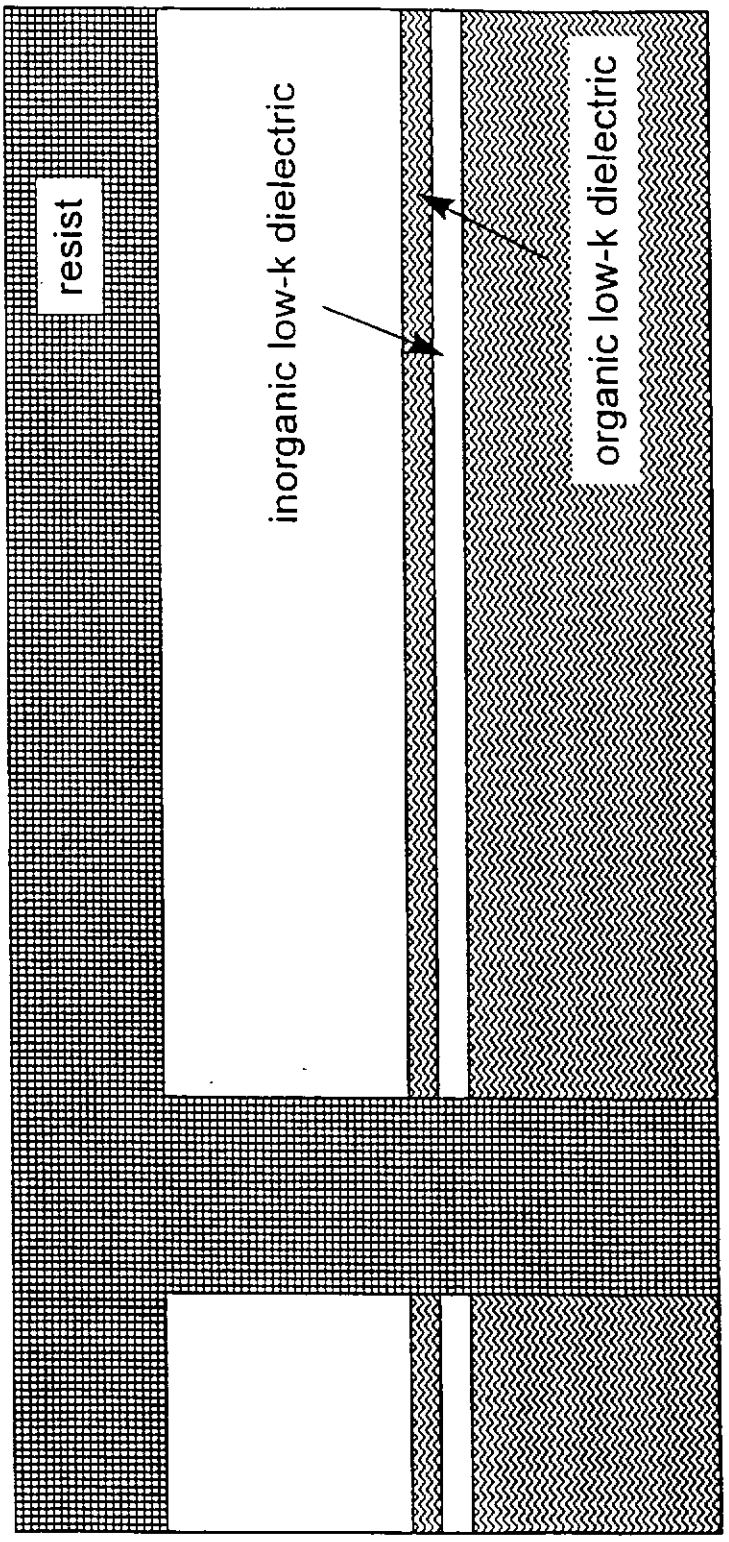


Figure 30

Step 12 Metal trench mask and resist development

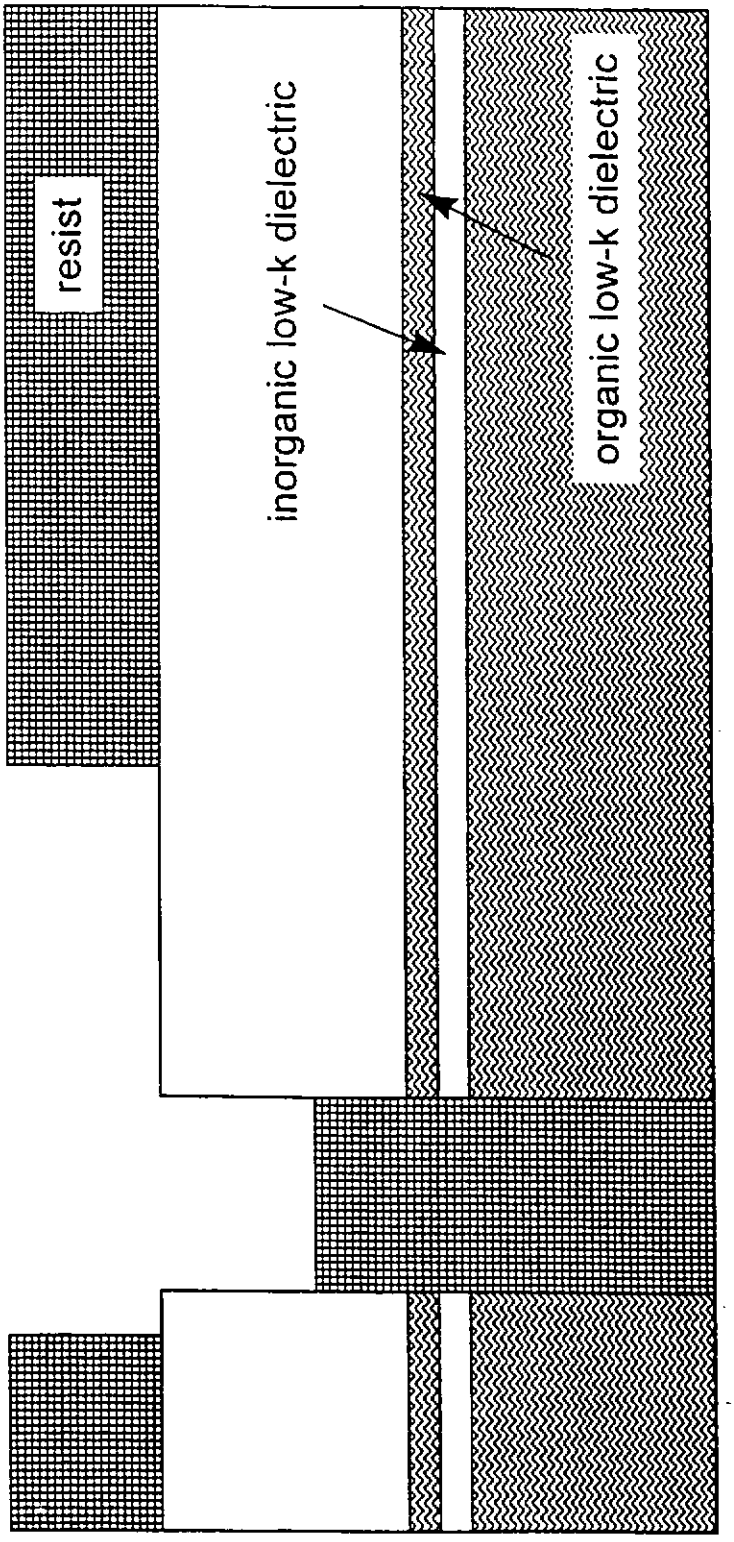


Figure 31

Step 13 Inorganic low-k dielectric etch

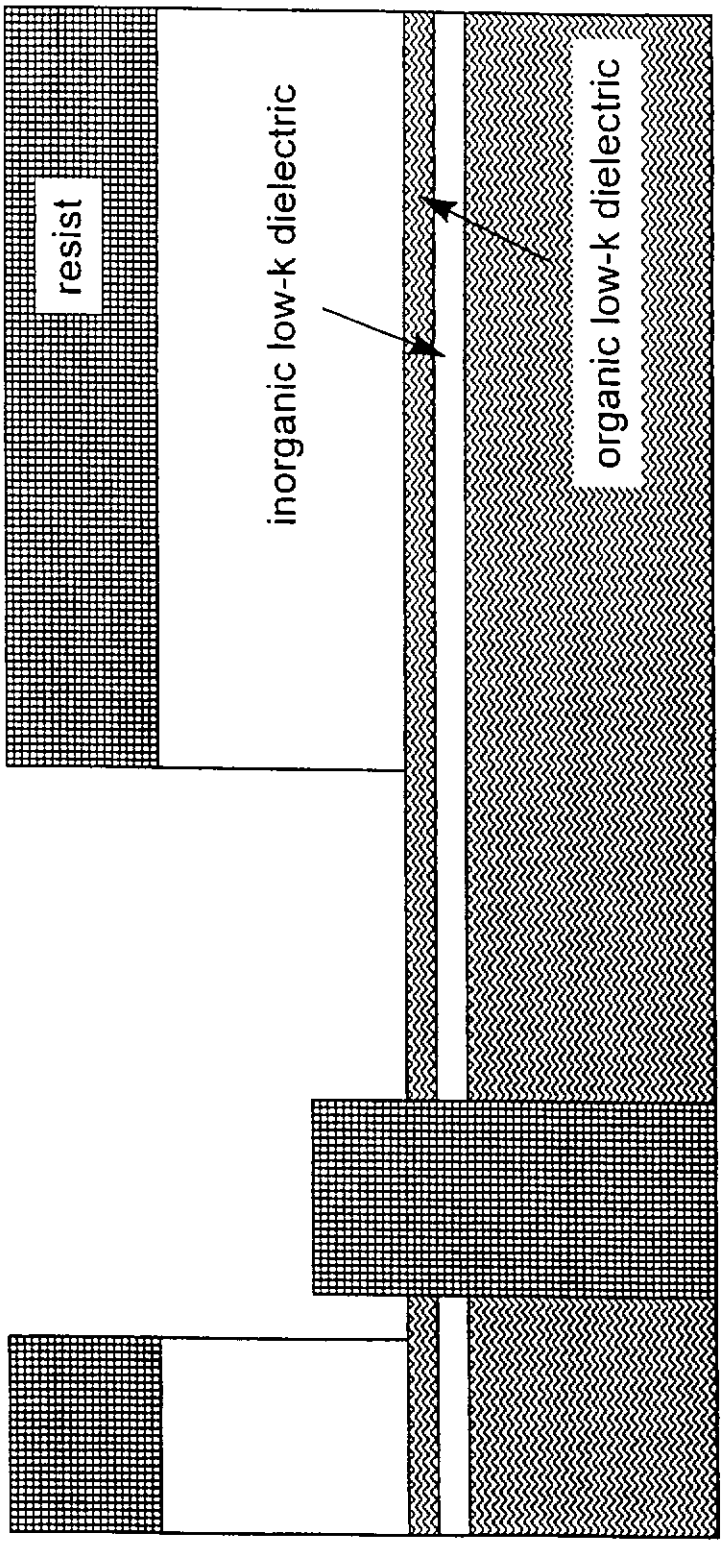


Figure 32

Step 14 Organic low-k dielectric and resist etch

