

PATENT SPECIFICATION

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(54) ELECTRONIC TIMEPIECE

(71) We, CITIZEN WATCH CO., LTD., a Japanese corporate body of 1-9-18, Nishishinjuku, Shinjuku-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

Background of the Invention

Field of the Invention

This invention relates to an electronic timepiece in which a given time count unit signal is synthesized based on a time reference signal, and in which a time keeping operation and time display operation is effected in response to the time count unit signal. More particularly, the invention relates to an electronic timepiece with a regulator circuit, of which the power consumption is reduced so that a battery life may be prolonged.

Description of the Prior Art

Heretofore, when an operation voltage of an electronic timepiece is predetermined, the selected voltage of its display part is the operation limit voltage of its display elements and that of the remainder of the timepiece is a battery voltage. For example, the operation voltage of a timepiece circuit is predetermined at 1.5 volts and that of a liquid crystal display circuit is preset at 3.0 volts.

However, several improvements have to be considered in the above systems with a view to reducing the power consumption.

Firstly, it is not necessary for a timepiece circuit to operate at the voltage of a battery cell. If the operation voltage of the timepiece circuit is lowered to a limit voltage determined by theoretic and practical limitation a supply voltage is also reduced to the limit voltage, further the impedance of the timepiece circuit is invariable and the power consumption may be reduced in proportion to the square of the supply voltage.

Secondly, of course, the minimum voltage for circuit operation of an integrated circuit depends on its circuit parameters, but, for example, the threshold voltage of each transistor in an integrated circuit, especially in C-MOS FET (Complementary Metal Oxide Silicon Field Effect Transistors), deviates depending upon the condition of the process of manufacturing an integrated circuit, whereby the current consumption deviates in proportion to the square of the number of the difference voltage between a supply voltage and a minimum operation voltage. Therefore, the wasteful power consumption reaches to a large rate in a practical timepiece circuit design when taking its voltage margin into account concerning the distribution of the deviations and fluctuations of the threshold voltage of the FET and that of the battery voltage. Thus, if the battery cell and the timepiece circuit are coupled with each other through a circuit means having a voltage matching function for the voltage difference as explained, the power consumption will be reduced very much.

Thirdly, it is meaningless when there exists each of the above circuit blocks individually. It is necessary that a signal is delivered from one circuit block to another circuit block and the circuit system is designed to become the conventional circuit block effects as a whole system such as transferring signals to the display elements or pulse motor. For this purpose, it is required that a level shift circuit amplifies the signal voltage lower than the battery voltage and delivers the enlarged signal to the other circuit. Unless the level shift circuit, a complementary transistor circuit, consumes much power when a low level amplitude signal is applied to an input of high voltage operation circuit.

Summary of the Invention

An object of this invention is to provide in a timepiece means for reducing the

power consumption without harming any timepiece characteristics.

For the above-mentioned purpose, this invention provides a timepiece system comprising a voltage control circuit which is easily manufactured in an integrated circuit.

In this invention, the circuit impedance of a block producing a signal, e.g., a crystal oscillating circuit as a time reference signal source, is left as it is. The operation voltage of an oscillation amplifying circuit is predetermined at a stable value lower than the battery voltage, the crystal oscillator operates under a low power condition. Successive circuit means for handling energy, e.g., means for driving a pulse motor, driving mechanical time keeping mechanism including a motor and wheel trains so as to display time or means for displaying the kept time in an electronic time keeping means are made operated at the higher battery voltage and as the result, the reduction of the power consumption is obtained without deterioration of the timepiece characteristics.

Brief Description of the Drawings

The above and other features of this invention will be described in greater detail hereinafter with reference to the accompanying drawings in which:

Figure 1 is a block diagram of an electronic timepiece system comprising a simple voltage control circuit to explain the operation of this invention;

Figures 2A and 2B are circuits relating to modifications of the voltage level shift circuit of Figure 1 and Figure 3;

Figure 3 is a block diagram showing another embodiment of an electronic timepiece of somewhat complicated but better operation, provided with a better voltage circuit;

Figure 4 is a block diagram of a further embodiment of an electronic timepiece with a simple voltage drop circuit;

Figure 5I and Figure 5II are a circuit diagram showing in detail one form of the integrated circuit of the embodiment of Figure 4;

Figure 6 is a graph showing voltage-current characteristics of C-MOS timepiece circuit system according to this invention;

Figure 7A and 7B are timing charts showing pulse trains to explain the system of rough frequency adjustment according to this invention;

Figure 7C is a timing chart and table showing resetting mode;

Figure 7D is a schematic view of inserting odd second and even second signals; and

Figures 8A and 8B are timing chart showing pulse trains to explain the system of resetting operation according to this invention.

Figures 1 and 6 are provided to help understanding the operation and the effect of the voltage control circuit in the timepiece C-MOS circuit system.

Detailed Description of Preferred Embodiments

In the embodiment of Figure 1, reference numeral 1 illustrates high frequency time reference signal source comprising a crystal oscillator element 2, coupling condenser 3, bias setting resistor 4 and an inverter 5. The output from the time reference signal source is delivered to the frequency divider 6 so as to synthesize the time count unit signal. Reference numeral 8 depicts a battery cell, of which power supply source voltage is applied to the inverter 5 via a resistor 7 and is applied to the frequency divider 6 through a diode 9.

The output of the frequency divider 6 is applied to further frequency divider 11 through a voltage level shifter 10 constituting a complementary metal-oxide-semiconductor (C/MOS) circuit which raises the voltage level. Then the output of the frequency divider 11, i.e., time count unit signal is fed to a time keeping counter means 12 for counting the time count unit signal so as to drive a time display means 13 consisting of, for example, a liquid crystal cell. Thus, the voltage across the battery cell 8 is applied directly to the level shifter 10, frequency divider 11, time keeping means 12 and time display means 13.

The resistor 7 has a resistance value such that a voltage derived from the battery cell 8 and applied to the signal source 1 has a value slightly higher than the oscillation starting voltage of the oscillator 2 and is also slightly higher than the frequency starting voltage of the frequency divider 6. Therefore, the time reference signal source 1 and frequency divider 6 do not waste much power when effecting their functions. On the other hand the circuit forming the elements following steps 10 to 13 consume extremely small power even though full battery voltage is applied thereto since the frequency of the applied signal has been reduced by the frequency divider 6 so that the number of the state variations is decreased. As the result, the over-all power consumption is reduced, and thereby the life of the battery cell is lengthened.

Figure 2 shows modifications of the voltage level shifter 10 of Figure 1. This level shifter 10 is useful especially for level-shifting in C/MOS circuits in which the differences of voltage levels are large, since it is small in power consumption and easily

incorporated into an integrated circuit. The detailed explanation on the level shifter 10 will now be made. A signal X_L is a signal whose level is lower than the high level voltage signals. A signal X_H is a signal produced from the signal X_L and is at a higher voltage level than the signal X_L being as high as the power source voltage. The negative level of the voltages of the signals X_L and X_H are assumed to be different from each other. In the case when the positive level voltages are substantially equal to each other, the NOR circuit made of a C/MOS circuit is replaced by a NAND circuit, for example, in a flip-flop type level shifter as shown in Figure 2A. Figure 2B shows a case where the NOR circuit in Figure 2A is made of a C/MOS circuit.

In Figure 2B, there are two current paths each comprising two N-channel transistors are connected in parallel with each other and two P-channel transistors corresponding thereto are connected in series with each other. The source electrode of each of the transistors of each channel is connected to a power source and the drain electrodes of the P and N channel transistors of each current path are connected together. Therefore, if at least one of two inputs of the NOR circuit is at the high level the output is set at the low level. As the result, the logical value of the output is not influenced with the remaining input signal and is independent of the level of the remaining input signal. In addition, even if the remaining input signal is at a halfway-voltage level being neither the high level or low level, there is no component of a through current flowing because of the short-circuiting of the power source through both the P and N-channel transistors. Therefore, the high level of the signal X_L in the NOR circuit may be at an insufficient voltage level. However, there is a single condition which is required. Namely, for example, it is essential that the output voltage of the NOR circuit can be changed from the high level to the low level by a high level signal of a voltage slightly below voltage X_L when a feed-back input signal is not the input signal X_L in the NOR circuit. For this purpose, the mutual conductance G_m of the N-channel transistor receiving the input signal X_L should be made large and that of the P-channel transistor should be made small. In addition, even if the P-channel transistor is turned on, the N-channel transistor of the input signal X_L is turned on at the input X_L by a slightly lower voltage. Therefore the output level should be compulsorily set to the low level even if insufficient. The reason why the set level may be insufficient is because the output level is gradually dropping to the complete logical level by

itself since the NOR circuit forms a positive feed-back loop. The same condition is required by the NOR circuit at the side of the input $\bar{X}_L$. In other words, the mutual conductance G_m of the N-channel transistor at the side of the input $\bar{X}_L$ is required to be large and that of the P-channel transistor not positioned at the side of the input $\bar{X}_L$ is required to be small.

This level shifting circuit results in a limited current flow during a transient state. Therefore, the power consumption is of no account in the level shifting at a low frequency. This is because in response of the output signal to the variations of the input logical value, the state is inverted speedily due to the high velocity of the NOR circuit in responding to the variations. The time of the transient state is short because the state reaches another ordinary state since a positive feed-back loop is formed.

Figure 3 shows another improved embodiment of the circuit of this invention.

Reference numeral 31 depicts a voltage controlling voltage drop circuit having a function corresponding to that of components 7 and 9 of Figure 1, 32 a time reference signal source composed of a crystal oscillator circuit, 33 a frequency divider functioning as a time counter unit signal synthesizing means, 34 a voltage level shift circuit, 35 an electronic time keeping counter means, 36 a DC/DC converter and 37 a time display means.

A thick line between blocks indicates an energy path and a thin line illustrates a signal path. The output voltage at 318 from the voltage controlling voltage drop circuit is regulated such that it becomes equal to the sum of the threshold absolute value of the transistors 311, 312. In an inverter circuit composed of complementary type transistors, i.e., N-channel enhancement type transistor 311 and P-channel enhancement type transistor 312, its gate terminal 316 and terminal 317 are coupled to each other. The drain current increases suddenly when the voltage across the terminals of the inverter is larger than the sum of the threshold voltage V_{TN} of the transistor 311 and the absolute value of the threshold voltage $|V_{TP}|$ of the transistor 312. The inverter is used to produce a stable reference voltage like a constant voltage Zener diode.

When an extremely small current is supplied through a high value resistor 314 to the inverter circuit and the voltage source across the power source terminals of the inverter is of low impedance as a result of a source follower circuit constituting a transistor 315, a voltage drop occurs by the amount of the threshold voltage V_{TN} of the

(16)

power supplying transistor 315 between the gate input voltage and source output voltage in the source follower circuit. For the purpose of compensating the voltage drop, use may be made of a circuit in which the gate and source of the transistor 313 are connected with each other and the circuit is designed such that a voltage higher than $(V_{TN} + |V_{TP}|)$ by V_{TN} may be supplied to the gate of the transistor 315. The power source voltage from a battery cell 38 is applied to lines 30, 39 and there is produced the voltage $(V_{TN} + |V_{TP}|)$ controlled in accordance with the threshold voltage of the transistor 315. For example, let the battery power source voltage be 1.58 volts, V_{TN} 0.4 volts and V_{TP} -0.3 volts, $(V_{TN} + |V_{TP}|)$ results in 0.7 volts.

The output voltage from the voltage drop circuit is not varied when the voltage of the battery cell lowers due to a higher power consumption of the battery cell due to, for example, providing an alarm sound requiring a large power. The oscillation frequency of the crystal oscillator 32 is kept constant. In the case when the threshold voltage of the transistor is varied as $V_{TN} = 0.3$ volts, $V_{TP} = -0.34$ volts, the output voltage becomes 0.65 volts accordingly so that a voltage equal to the voltage $(V_{TN} + |V_{TP}|)$ is always applied to the oscillator 32 and frequency divider 33.

The output voltage of the circuit 31 is finely adjustable by adjusting the value of the resistor 314 and mutual conductance of the transistors 311, 312, 313. The transistor 315 results in the voltage $(V_{TN} + |V_{TP}|)$ on the line 319 being derived from the line 318 at low impedance, the transistor 315 operating as a voltage follower power amplifier because of the impedance conversion. The differentiated impedance on the line 318 can be an extremely low value by enlarging the mutual conductance of the transistor 315. As the result, the output voltage is kept constant even if a load current changes suddenly and thus the reliability of the circuit operation is improved.

The Figure 4 is a block diagram of another embodiment of the timepiece shown in detail in the integrated circuit of Figures 5I and 5II. A thick line indicates an energy path and a thin line illustrates a signal path. Reference numeral 400 designates a simple voltage dropper circuit which reduces the power consumption of the timepiece and 401 a time reference signal source including a crystal oscillator element of 32 KHz, 402 a time count unit signal synthesizing means, 403 a time keeping means, 404 a voltage level shift circuit and 405 a driving circuit of which the output is for driving a pulse motor for driving watch hands (not shown). The voltage dropper circuit 400 constitutes a

current control provided with a voltage control resistor 407 utilizing a field effect transistor 408. The voltage dropper circuit 400 produces a voltage lower than the power source voltage provided by battery cell 406. In this embodiment, the low voltage is at about a half of the power source voltage which is shown as $V_{m/2}$ and the connection point of the resistor 407 and field effect transistor 408 is at $2/3$ voltage of the power source voltage and is shown as $V_{m/3}$.

The time reference signal source 401, time count unit signal synthesizing circuit means 402 and time keeping means 403 are operated by the low voltage, the level of the output signals therefrom is raised by the circuit 404 so that the output for driving the pulse motor may be synthesized by the driving circuit 405.

The timepiece according to this embodiment has two reset function for stopping the even number seconds and a function for course frequency adjustment. The controllable range of the frequency is ± 15 PPM and the combination of a trimmer capacitor, etc. enables extremely highly precise frequency adjustment.

This system will now be described in greater detail by means of a practical circuit shown in Figures 5I and 5II. Reference numeral 500 depicts a low voltage operating circuit means comprising a time count unit signal synthesizing means 581 comprising flip-flops 520, 521, 522 and Exclusive OR circuit 531, etc. The output ϕ from an oscillator inverter 530 is not a complete rectangular wave form and is delivered to the input of the time count unit signal synthesizing means 581 through an inverter 532 with a low mutual conductance for shaping wave forms. The output of the time count unit signal synthesizer 581 is counted down to 0.5 Hz by means of toggle-type flip-flops 501 to 516.

D-type flip-flop 517 is for delaying the output of the flip-flop 516 and the combination of the output signal from the flip-flops 516, 517 produces the signals Q_A , Q_B for driving a pulse motor M connected to terminals 550, 570 for driving watch hands (not shown). A level shift circuit comprises four NOR circuits 541 to 544 with two inputs respectively. A terminal 560 is a frequency control terminal, a terminal 591 is a reset terminal for stopping the even number seconds and a terminal 540 is a reset terminal for stopping the desired number second. Ordinarily a 64 Hz signal is derived from a terminal 564 and reversely the insertion of a 64 Hz signal into the terminal 564 enables the operation of circuits following after the flip-flops 510.

Under an ordinarily-operating condition, the circuit 500 corresponding to the time

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reference signal source 401, time count unit signal synthesizer 402 and time keeping means 403 in Figure 4 is operated by the voltage $V_{m1/2}$ produced by means of the low voltage converter 599.

The integrated circuit according to this embodiment is operable at each of the voltages $V_{m1/2}$, $V_{m2/2}$, V_{m1} , by selectively short-circuiting the terminals 533, 5532 and 5531.

Next, rough frequency adjustment will be explained with reference to timing charts of Figures 7A and 7B. In case that rough frequency adjustment is not effected, the terminal 560 is kept open. This open state results in signal ϕ_{ADD} ="H" (high level) and ϕ_B ="L" (low level) since signal F_C is at "L". As the result, rough frequency adjustment is not effected. On the other hand, rough frequency adjustment can be effected if the output terminal 560 is connected to the output terminal 570 or 550. If the output terminals 560, 570 are connected with each other, a logical level of the output ϕ_B is kept at "L" and thereby the output ϕ_{ADD} becomes Q_A which is an inverted value of Q_A . Furthermore, if the terminal 560, 550 are connected with each other, the output ϕ_{ADD} is kept at "H" and ϕ_B is completely equivalent to Q_B . The output Q_A is synchronized with the leading edge of the output Q_{16} from the flip-flop 516 and Q_B is

synchronized with the trailing edge of Q_{16} . The outputs Q_A , Q_B are both 0.5 Hz and have a pulse width of substantially 7.8 msec. The outputs ϕ_{21} , ϕ_{22} have 1/4 duty cycle and frequency of 2^{14} Hz. The output ϕ_{21} is also utilized as a clock signal for D-type flip-flops 521, 522. The flip-flops of this embodiment are trailing edge trigger type ones as distinct from toggle-type flip-flops.

The output ϕ_{22} of the OR gate 596 in the time count unit signal synthesizer is equal to $Q_{21}+Q_{22}$. If the terminal 560 is opened or the terminals 560 and 570 are connected with each other, the output ϕ_{21} is always at "H" and thereby ϕ_{22} is always at "H". If the terminals 560, 550 are connected with each other, ϕ_{21} has the same wave form as that of Q_B though the voltage level between "H" and "L" is different since the level shift has been effected. "L" is maintained for 1 cycle ($1/2^{14}$ sec.) synchronized with the trailing edge of ϕ_{21} every two seconds. As the result, one pulse is subtracted from the output from AND gate 597 every two seconds. The output ϕ_{EXT} of NOR gate 598 is equal to $\phi_{21}+\phi_{22}$, the output ϕ_{15} from Exclusive OR gate 531 is equal to $\phi_{EXT}+\phi_{ADD}$. ϕ_{ADD} is always at "H" and as the result the output ϕ_{15} from Exclusive gate 531 is equal to the frequency of 2^{13} Hz from which one pulse is subtracted every two seconds. Accordingly,

the connection of the terminals 560 and 550 results in a frequency adjustment of $-1/2^{13}$ per 0.5 Hz, that is, about -15 PPM ($0.5/2^{13}$).

If the terminals 560, 570 are connected with each other, the output ϕ_{EXT} has the same wave form as one delivered to the time count unit signal synthesizer through the wave form shaping inverter. ϕ_{ADD} has a wave form of reverse phase as compared with Q_A .

However, there is a time delay during passing through C/MOS gate from 531 to 517, etc. and as the result, the delay of phase is produced as shown in the timing charts. Therefore the output ϕ_{15} is added exclusively by the Exclusive-OR gate. It can be clearly seen on the timing chart whether the frequency control is accomplished or not if the number of leading edges or trailing edges is counted for a certain period, for example, from immediately before where ϕ_{ADD} becomes "L" to immediately after where ϕ_{ADD} becomes "H". Namely, the output ϕ_{15} is

greater by one than ϕ_{EXT} in respect of the number of leading edges or trailing edges counted over the certain period and as the result, it is equal to the result of adding one pulse to the output of the oscillator.

As seen from the above, the phase lags by 15 PPM when the terminal 560 is connected with the terminal 550 and is ahead when the terminal 560 is connected with the terminal 570.

Referring to the insertion of a reset signal RST to stop the second hand, four signal modes are shown in Figure 7C regarding the timing of the insertion of a reset signal. Here let four periods be Q_{A1} , Q_{A2} , Q_{B1} , Q_{B2} .

In Figure 7D, the signal RST is delivered when the even second stop signal is inserted into an even second and the signal STP is delivered when the desired stop signal is inserted.

In both cases, the flip-flops 510 through 515 are reset instantly.

In Figures 8A and 8B, the periods Q_{A1} , Q_{A2} , Q_{B1} , Q_{B2} are arranged from the left side on the timing chart wherein wave forms are shown upon the insertion of a reset signal.

In the case when the even number second is stopped the signal RST and driving pulse are not overlapped with each other. Therefore the pulse width of the drive pulse for the pulse motor M is kept constant and as a consequence there is no possibility that the second hand of the timepiece operates unstably.

When the desired second stop signal is inserted under each of four modes, the operation is as follows:

(1) the periods Q_{AI} and Q_{AH} . Instant stop is effected, reset is released and then the side of the terminal 550 operates after one second from the release thereof.

(2) the periods Q_{BI} and Q_{BH} .

Instant stop is effected, reset is released and then the side of the terminal 570 operates after one second from the release thereof.

When the even number second stop signal is inserted under each of four modes, the operation is as follows:

(1) the periods Q_{AI} and Q_{AH}

Instant stop is effected, reset is released and then the side of the terminal 550 operates after one second from the release thereof.

(2) the periods Q_{BI} and Q_{BH}

The signal of the terminal 570 is delivered in the instant of resetting and then stops, and if the reset is released, the side of the terminal 550 operates after one second from the release thereof.

As seen from the above, the terminal 570 is for the even number second output and the terminal 550 is for the odd number second output. In conclusion, the second hand always stops at an even number second and starts from an odd number second after one second from releasing the reset if the even number second stop signal is inserted.

In Figure 6, are shown voltage current characteristics of a timepiece showing the effect of this invention. A curve (I) shows characteristics in the case where the terminals 5532 and 5531 are short-circuited with each other in Figure 5, wherein both functions of voltage drop and level shift operate effectively. A curve (II) shows the case that the terminals 533 and 5331 are short-circuited with each other and the timepiece circuits are all operated at the voltage ($V_{DD}-V_{TH}$) so as to indicate voltage-current characteristics of the conventional timepiece circuit systems. The curve (I) shows that the timepiece circuit operates normally on the right side from a point P along points P S W V T as the power source voltage is raised up from zero volt and operates along points T U V W X as the power source voltage is lowered. The curve (II) illustrates that when the timepiece circuit operates from a voltage lower than that of the curve (I), the point P moves to the point Q and normally operates on the right side (high voltage side) of the point Q. In this case, the operating point is shifted from the point Q to the point R of the voltage.

A curve (III) is positioned at a position corresponding to the displacement of the

curve (I) in the right direction and shows the operating characteristics when the terminals 5532 and 5531 are not connected with each other so that the supply voltage is higher. An integrated circuit for use in the timepiece circuit of this invention is designed such that the same integrated circuit may be used for large scale crystal clock operating at a higher voltage as well as a crystal wristwatch operating at a lower voltage.

According to a current axis, the normal operating characteristics is more than $0.45\mu A$ in the curve (II) and is more than $0.35\mu A$ in the curves (I), (III).

Referring to operation starting current, the curves (I), (II), (III) illustrate about equivalent, i.e., $0.4\mu A$ or so, but they are different in current increase in the area wherein the operation starting voltage is exceeded. Namely, in the area, the curve (II) increases by a rate of square number of the voltage while the curves (I) and (III) only increase linearly. In addition, the curve (III) shows that the rate of the current increase is substantially equal to that of the curve (I) though the operating voltage is higher.

Referring to the power consumption, the curve (II) shows that it increases in proportion to a cube of the supply voltage while the curve (I) shows that it increases in proportion to a square thereof.

In the system shown by the curve (I), if the supply voltage is 1.58 volts, the range of the operation voltage is from 1.35 to 1.65 volts and the various voltages of the threshold value are 0.2 volts respectively, $V_{TN}+|V_{TP}|$ and become equal to 0.95 volts under the worst condition. In this case, if the curve (I) is shifted by 0.1 volt in the left direction, the current consumption is about $0.6\mu A$ at the voltage of 1.58 volts. In reverse, if $V_{TN}+|V_{TP}|$ is equal to 1.35 volts, the current consumption is $0.35\mu A$, i.e., $0.5\mu A$ on an average. Adapting this to the curve (II), the current consumption is about $2\mu A$ in case of $V_{TN}+|V_{TP}|=0.95$ volts and is about $0.45\mu A$ in case of $V_{TN}+|V_{TP}|=1.35$ volts, i.e., $1.2\mu A$ on an average. Even in the curve (II), the current consumption is a half of $2.5\mu A$ in the conventional integrated circuit for a timepiece since there is effected a counter-measure to lower the power consumption in the system.

The construction of the circuit of the timepiece of this invention is applicable to as Integrated Injection Logic (I²L) circuit, Complementary Metal Oxide Silicon (CMOS) circuit, complementary bipolar circuit and the other well-known integrated circuits.

WHAT WE CLAIM IS:—

1. An electronic timepiece including a

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(1) the periods Q_{AI} and Q_{AII} .
Instant stop is effected, reset is released and then the side of the terminal 550 operates after one second from the release thereof.

(2) the periods Q_{BI} and Q_{BII} .

Instant stop is effected; reset is released and then the side of the terminal 570 operates after one second from the release thereof.

When the even number second stop signal is inserted under each of four modes, the operation is as follows:

(1) the periods Q_{AI} and Q_{AII}

Instant stop is effected, reset is released and then the side of the terminal 550 operates after one second from the release thereof.

(2) the periods Q_{BI} and Q_{BII}

The signal of the terminal 570 is delivered in the instant of resetting and then stops, and if the reset is released, the side of the terminal 550 operates after one second from the release thereof.

As seen from the above, the terminal 570 is for the even number second output and the terminal 550 is for the odd number second output. In conclusion, the second hand always stops at an even number second and starts from an odd number second after one second from releasing the reset if the even number second stop signal is inserted.

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The construction of the circuit of the timepiece of this invention is applicable to as Integrated Injection Logic (I²L) circuit, Complementary Metal Oxide Silicon (CMOS) circuit, complementary bipolar circuit and the other well-known integrated circuits.

WHAT WE CLAIM IS:—

1. An electronic timepiece including a





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5 time reference signal source for generating
a time reference signal, a time count unit
synthesizing means for synthesizing a time
count unit signal from the time reference
signal, a time keeping means for counting
the time count unit signal, a time display
means or a time display drive means for
displaying or for causing to be displayed
time information kept by the time keeping
means, and a battery cell for supplying
10 electric energy to said source and to each
said means, wherein; the electric timepiece
further comprises a voltage source circuit
means energised by the battery for
15 producing a second voltage which is lower
than the battery voltage, the second voltage
being applied to at least one of said time
reference signal source, said time count
unit synthesizing means and said time-
20 keeping means so that electrical energy
from the battery is supplied to at least one
of said source and said means at a voltage
which is lower than the battery voltage, and
a voltage level shift means for raising the
25 level of the signal in the signal transfer path
between the output and the input of circuit
means energised by different voltages.
2. An electronic timepiece according to
claim 1, wherein said second voltage is
30 supplied to said time reference signal
source.
3. An electronic timepiece according to
claim 1 or claim 2, wherein said second
voltage is supplied to said time unit signal
35 synthesizing means.

4. An electronic timepiece according to
any preceding claim, wherein said second
voltage is supplied to said time keeping
means.

5. An electronic timepiece according to
any preceding claim, wherein said voltage
source circuit means comprises a reference
voltage producing first circuit means and a
power controlling second circuit means
which controls electric power according to
said reference voltage.

6. An electronic timepiece according to
claim 5, wherein said first circuit means
comprises a series coupled circuitry of a
nonlinear semi-conductor device and a
resistor device.

7. An electronic timepiece according to
claim 6, wherein said nonlinear
semiconductor device is composed of a
field effect transistor.

8. An electronic timepiece according to
claim 5, wherein said second circuit means
comprises a field effect transistor in
voltage follower operation.

9. An electronic timepiece substantially
as hereinbefore described with reference
to, and as illustrated in, the accompanying
drawings.

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