WHAT IS CLAIMED IS:

1. A method for forming semiconductor packages comprising:

disposing a plurality of ~~one or more~~ semiconductor chips on a top side of a non-singulated semiconductor wafer;

disposing a stiffening layer above the plurality of semiconductor chips without contacting the non-singulated semiconductor wafer; ~~and~~

molding the plurality of semiconductor chips with a molding material, wherein during the molding process, the molding material flows into a first space between the stiffening layer and the non-singulated semiconductor wafer and a second space between the stiffening layer and the plurality of semiconductor chips; and

singulating the molded semiconductor chips on the non-singulated semiconductor wafer with the stiffening layer into individual units.

2. The method of claim 1, further comprising:

curing the molding material;

wherein the stiffening layer provides support to the package during the curing.

3. The method of claim 1, wherein the stiffening layer is silicon or glass.

4. The method of claim 1, wherein the stiffening layer directly contacts the semiconductor chips.

5. The method of claim 1, wherein a thermally conductive layer is provided between the stiffening layer and the top surface of the semiconductor chips.

6. The method of claim 1, wherein a temporary adhesive is provided on the surface of the stiffening layer facing the semiconductor chips.

7. The method of claim 1, wherein the stiffening layer is completely removed from the molding material.

8. The method of claim 7, wherein the removing is performed by mechanical grinding or chemical etching.

9. The method of claim 1, wherein the stiffening layer is partially thinned.

10. The method of claim 9, wherein the thinning is performed by mechanical grinding or chemical etching.

11. ~~The method of claim 1~~A method for forming semiconductor packages comprising:

disposing one or more semiconductor chips on a top side of a wafer;

disposing a stiffening layer above the semiconductor chips; and

molding the semiconductor chips with a molding material between the stiffening layer and the wafer, wherein the stiffening layer covers a top side of the molding material only on a periphery of the wafer.

12. The method of claim 11, wherein the stiffening layer is in the shape of a ring.

13. The method of claim 11, wherein the stiffening layer is in the shape of a square or a rectangle.

14. The method of claim 1, wherein the stiffening layer substantially covers a top side of the molding material.

15. The method of claim 11, wherein the stiffening layer is removed by singulating semiconductor packages on the wafer.

16. A method for forming semiconductor packages comprising:

disposing a plurality of ~~one or more~~ semiconductor chips on a top side of a non-singulated semiconductor wafer;

disposing a stiffening layer in contact with the top side of the non-singulated semiconductor wafer only on the periphery of the non-singulated semiconductor wafer; ~~and~~

molding the plurality of semiconductor chips with a molding material, wherein during the molding process, the molding material flows into spaces being bound~~ed~~ by an inside-facing surface of the stiffening layer at the periphery of the non-singulated semiconductor wafer and between the plurality of chips; and

singulating the molded semiconductor chips on the non-singulated semiconductor wafer into individual units.

17. The method of claim 16, further comprising:

curing the molding material;

wherein the stiffening layer provides support to the package during the curing.

18. The method of claim 16, wherein the stiffening layer is silicon or glass.

19. The method of claim 16, wherein the stiffening layer is in the shape of a ring.

20. The method of claim 16, wherein the stiffening layer is in the shape of a square or a rectangle.

~~21. A semiconductor package comprising:~~

~~a semiconductor chip disposed on a top side of a portion of a wafer; and~~

~~a molding material encapsulating at least the sides of the semiconductor chip, the molding material having been molded between the portion of the wafer and a stiffening layer disposed over the molding material.~~

~~22. The semiconductor package of claim 21, wherein:~~

~~the stiffening layer substantially covers the molding material.~~

~~23. The semiconductor package of claim 22, wherein:~~

~~the stiffening layer directly contacts the surface of the semiconductor chips.~~

~~24. The semiconductor package of claim 22, wherein:~~

~~the stiffening layer has been completely removed from the semiconductor package.~~

~~25. The semiconductor package of claim 22, wherein:~~

~~the molding material completely encapsulates the semiconductor chip, the molding material having been molded between the portion of the wafer and a stiffening layer disposed over the molding material only at the periphery of the wafer.~~

~~26. The semiconductor package of claim 25, wherein:~~

~~the stiffening layer has been completely removed by singulation of the semiconductor package.~~

~~27. A semiconductor package comprising:~~

~~a semiconductor chip disposed on a top side of a portion of a wafer; and~~

~~a molding material encapsulating at least the sides of the semiconductor chip, the molding material having been molded in an area above the portion of the wafer bounded by an inside surface of a stiffening layer disposed over the molding material.~~

~~28. The semiconductor package of claim 27, wherein:~~

~~the stiffening layer has been completely removed by singulation of the semiconductor package.~~

21. The method of 16, wherein the stiffening layer is removed by singulating the molded semiconductor chips on the non-singulated semiconductor wafer.

22. A method for forming semiconductor packages comprising:

disposing a plurality of semiconductor chips on a top side of a semiconductor wafer, wherein the semiconductor wafer comprises one or more through silicon interconnects which extend from the top side of the semiconductor wafer;

disposing a stiffening layer above the plurality of semiconductor chips on the semiconductor wafer;

molding the plurality of semiconductor chips with a molding material, wherein during the molding process, the molding material flows into a space between the stiffening layer and the semiconductor wafer; and

singulating the molded semiconductor chips on the semiconductor wafer into individual units.

23. The method of claim 22 comprising polishing a back side of the semiconductor wafer to expose end portions of the through silicon interconnects while the stiffening layer is still in contact with the molding material prior to singulating the molded semiconductor chips on the semiconductor wafer.

24. The method of claim 23 comprising providing conductive bumps that are electrically coupled to the exposed end portions of the through silicon interconnects prior to singulating the molded semiconductor chips on the semiconductor wafer.

25. The method of claim 24 comprising removing the stiffening layer from the molded semiconductor chips before singulating the molded semiconductor chips on the semiconductor wafer into individual units.

26. The method of claim 1 wherein the non-singulated semiconductor wafer comprises one or more through silicon interconnects which extend from the top to back side of the non-singulated semiconductor wafer.

27. The method of claim 11 wherein the stiffening layer is silicon or glass.

28. The method of claim 11 wherein the semiconductor wafer comprises one or more through silicon interconnects which extend from the top side of the semiconductor wafer.

29. The method of claim 27 comprising polishing a back side of the semiconductor wafer to expose end portions of the through silicon interconnects.

30. The method of claim 28 comprising providing conductive bumps to the exposed end portions of the through silicon interconnects.