ABSTRACT

An epitaxial semiconductor material particularly suitable for a high switching rectifier has misfit dislocations (28, 30, 32) formed in the depletion region (16) adjacent a PN junction (20). A method is described for forming each Si/Ge misfit dislocation region (Fig. 2) epitaxially on a capped Si substrate (10). These misfit dislocation layers are formed in a step in a CVD reactor chamber at a lowered temperature. To enhance switching speed gold, and preferably gold and platinum, is diffused through the Si body and forms relatively large concentrations at the misfit dislocation sites. In a modification (Fig. 3) the misfit dislocations are provided just outside the depletion region (16).

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