

PATENT SPECIFICATION

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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Semiconductor Device

We, TEXAS INSTRUMENTS INCORPORATED, a corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to semiconductor devices and methods of making same.

The present invention is a method of making a semiconductor device having therein two spaced rectifying junctions, said method comprising epitaxially depositing from the vapour phase a single crystal layer of semiconductor material on a single crystal substrate of said semiconductor material with inclusion one in each of the two consisting of said layer and said substrate of two impurities determining the same conductivity type and of different concentrations and the further inclusion in that one of the two containing the greater impurity concentration of a further impurity of a concentration intermediate to those of the other two impurities, determining the opposite conductivity type, and of substantially greater diffusion coefficient than that of the impurity of said greater concentration, and simultaneously diffusing the two impurity concentrations in said one of the two across the boundary between the two to form said junctions in the other of the two.

A description of the general technology relating to epitaxial methods and devices is given in the publication by Sigler, J. and Watelski, S. entitled *Epitaxial Technique in Semiconductor Device*, Solid State Journal, 2, (1961). This technology in-

cludes the growing on a single crystal semiconductor substrate of a single crystal layer of the same semiconductor material from the vapour phase. This is carried out by heating the substrate to a predetermined elevated temperature and supplying in the presence of the heated substrate a vapour of a semiconductor compound and hydrogen. The semiconductor compound is normally a halide compound of the semiconductor, and the heat and hydrogen reduce the compound to an acid of the halide and the elemental semiconductor, the latter depositing on the substrate and growing as a single crystal to produce a continuation of the original substrate. Many variations in and substitutions to the above method are possible, as described in the Sigler publication, supra, and as will be more particularly pointed out hereinafter.

Although use of epitaxial methods are becoming more prominent in semiconductor manufacture because of the various advantages associated therewith, it is nevertheless desirable to continue the manufacture of most of the devices whose operating characteristics are identical to devices made according to older methods. In this sense, epitaxial technology provides a new and improved method of making devices whose operating characteristics are unchanged over the older devices, although in many instances the device structure itself will be different.

The present invention takes advantage of and utilizes epitaxial techniques in conjunction with diffusion technology to provide devices having essentially the same applications as some of the equivalent devices made according to older methods, wherein the characteristics are improved and the device structure has advantages heretofore realized. In particular, the invention is

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Simultaneously

diffusion

concerned with a semiconductor device having a pair of rectifying junctions formed by the simultaneous diffusion of two impurities of opposite conductivity determining types and of different diffusion rates. A portion of the body of the semiconductor device is epitaxially grown on a single crystal substrate, and simultaneous therewith or subsequent thereto, whichever is more advantageous as will be explained hereinafter, there is carried out the simultaneous diffusion of two impurities contained in the body to form a pair of junctions. The impurities are either incorporated in the original substrate so that the junctions are diffused in the epitaxial layer, or the impurities are deposited with the epitaxial layer so that the junctions are diffused in the substrate. The simultaneous diffusion of opposite type impurities of differing diffusion coefficients to form a pair of rectifying junctions is very advantageous in that the width of the region between the junctions (normally the base region of a transistor) may be made as narrow as desired and controlled to very close tolerances. Moreover, as will become apparent hereinafter, the absolute impurity concentrations can be closely controlled as a consequence of using epitaxial methods. All of these advantages and others to be discussed hereinafter make possible the manufacture of devices more expediently at lower costs and with closer tolerances than heretofore possible.

The invention will now be described, by way of example, with reference to the accompanying drawings, wherein like reference numerals refer to like parts throughout the several figures, and in which:

Fig. 1 is an illustrative sectional view of a furnace for epitaxially growing on a single crystal semiconductor substrate a single crystal layer of the semiconductor material;

Fig. 2 is an elevational view in section of a semiconductor body having a pair of rectifying junctions made by the method of the invention;

Fig. 3 is a sectional view in elevation of a portion of the semiconductor body of Fig. 2 and a graphical illustration of the impurity concentrations as a function of distance through the body; and

Fig. 4 is an illustrative view of a transistor made according to the method of the invention.

According to one aspect of the invention a semiconductor device is made by an epitaxial process wherein two impurities of opposite conductivity determining types and of different diffusion coefficients are contained within a single crystal semiconductor substrate, and by an epitaxial process according to the Sigler publication, supra, a single crystal layer of the semiconductor

material is grown on the substrate to provide a continuation thereof. In another aspect the two impurities are included in the semiconductor compound used to produce epitaxial growth from the vapour phase, in which case the impurities are contained within the epitaxial layer. Simultaneously with and/or subsequent to the epitaxial growth of the layer, the two impurities are simultaneously diffused from the portion of the semiconductor body wherein they are contained into the epitaxial layer or the original substrate, whichever is the case. That is to say, the impurities are diffused from the region of higher impurity concentration to the region of lower impurity concentration. The concentration of the faster diffusing impurity is less than that of the slower diffusing impurity, so that after diffusion, the slower impurity will be in a concentration sufficient to cause the formation of a rectifying junction by compensation of the faster impurity. On the other hand, the faster impurity "outruns" the slower and forms another rectifying junction spaced from the junction formed by the slower impurity. In the case where the two impurities are contained within the original substrate, the semiconductor compound used to provide the epitaxial layer is also doped with an impurity of the same type as that of the slower diffusing impurity to provide the epitaxial layer with the desired electrical conductivity of the same type as the slower impurity. In the case where the two impurities are contained within the epitaxial layer, the original substrate is doped with this impurity.

In order to facilitate the description of the invention, reference will be had to an n-p-n silicon transistor wherein two impurities of opposite conductivity determining types are contained within a single crystal silicon substrate and a single crystal silicon layer is epitaxially grown thereon. In this case the rectifying junctions are formed within the epitaxial layer by diffusion. However, it is expressly recognized that the method is also applicable to the provision of the two impurities in the compound of the semiconductor in the vapour phase used to produce the growth of the epitaxial layer.

In such case, the junctions are formed within the original substrate by diffusion. The method is also applicable to any semiconductors capable of being diffused with impurities and which are susceptible of epitaxial growth.

A single crystal silicon substrate, usually in the form of a wafer, is doped uniformly throughout with both a p-type and n-type impurity. For example, boron is suitable as a p-type impurity and arsenic is suitable as an n-type impurity, the former having a greater diffusion coefficient than the latter.



amounts

The arsenic is more heavily concentrated for the reason noted above. The wafer is provided by any suitable means, such as growing a single crystal ingot from a silicon melt into which has been added the proper amount of the impurities, and slicing a wafer from the ingot so that the faces lie in one crystal plane. This is normally the 1, 1, 1 plane for silicon. The faces of the wafer are then mechanically and/or chemically polished by conventional methods to perfect them to the highest possible degree.

A single crystal silicon layer is then epitaxially grown on a face of the wafer. As shown in Fig. 1 the wafer now designated at 4 is placed within a furnace designated generally at 2, which comprises an enclosure having an inlet and an outlet and means for locally heating the wafer to the desired elevated temperature. The furnace comprises a quartz tube 8 having an outlet 10 adjacent one end thereof and having an inlet 12 adjacent the other end. A removable stopper or plug 14 blocks one end of the tube and provides access to the interior thereof. Passing through the plug are two electrical connections 16 and 16' that support and are electrically connected to a graphite platform 18 which is used as a resistance heater. The wafer 4 rests on this platform. The electrical connections are connected to a current supply for passing current through the platform for heating the wafer.

Current is passed through the heater 18 to raise the temperature of the silicon wafer to about 1000°C to 1300°C. A vapourized mixture of hydrogen and a silicon-halide compound doped with a suitable n-type conductivity determining impurity is passed through the inlet 12 and over the face of the wafer. The above temperature range is sufficiently high to cause the reduction of the silicon-halide compound in the presence of hydrogen to elemental silicon and an acid of the halide. The elemental silicon deposits on the surface of the wafer and grows as a single crystal to provide a continuation of the wafer crystal. Because of the impurity contained in the vapourized mixture, the epitaxial layer grown on the face of the wafer is doped and results in the conductivity type of this impurity, which, in this case is n-type conductivity.

Simultaneous with the epitaxial growth, the impurities contained in the wafer migrate by diffusion into the epitaxial layer. The extent of diffusion will, of course, be determined by the temperature of the wafer and layer and the duration of time that the elevated temperature is maintained, wherein specific times and temperatures will be set forth below. For silicon, however, diffusion is slight at 1000°C and is quite extensive at 1300°C, subject, of course, to the duration

of time in which the wafer is maintained at these temperatures. In the method of this invention, the epitaxial growth is continued until the layer reaches the desired thickness. The time required to achieve this thickness may be sufficiently long to cause the impurities contained in the substrate to diffuse to the desired depth into the layer to form therein a pair of spaced, rectifying junctions. In the event that the epitaxial layer thickness is obtained before the diffusion has been sufficiently carried out, the flow of the vapourized mixture is stopped, and the wafer is maintained at the elevated temperature to continue the diffusion without the continued growth of the layer. Or, alternately, the flow is stopped, the temperature of the wafer lowered, and the wafer removed from the furnace and subsequently heated to complete the diffusion.

The foregoing is a description of the general steps for carrying out the method. In general the epitaxial growth is carried out in accordance with the description in the Sigler publication supra. Any suitable furnace that provides an enclosure and localized heating can be used. The localized heating of the wafer without corresponding heating of the furnace walls merely prevents depositing the semiconductor material on the walls of the furnace.

There is shown in Fig. 2 the epitaxial silicon body made according to the foregoing description with two rectifying junctions separating the body into three regions of alternating conductivity type. The dashed line 20 represents the mechanical interface between the original substrate wafer 4 and the epitaxial layer, now designated at 22. Ideally, the mechanical interface is perfect and constitutes a continuation of the substrate crystal, although in practice there are some irregularities at this interface. The simultaneous diffusions of the two impurities contained in the wafer produces a first junction 24, caused by the faster diffusing boron, and a second junction 26, caused by the slower diffusing and more heavily concentrated arsenic. The epitaxial layer is doped with an impurity such as phosphorus as alluded to above, but the concentration of the phosphorus is sufficiently low to be dominated by the boron between the junctions 24 and 26. Thus the portion 28 of the epitaxial layer between the surface of the layer and the junction 24 constitutes a first region of a first conductivity type, n-type in this example; the portion 30 of the layer between the two junctions 24 and 26 constitutes a second region of the opposite conductivity type, p-type in the example; and the entirety of the original substrate and the portion of the layer between the interface 20 and the junction 26 constitutes a third region of the same conductivity type

as that of the first region.

In Fig. 3 there are shown a sectional view in elevation of a portion of the body of Fig. 2 and a graphical illustration of the impurity concentration in atoms per cubic centimeter as a function of distance in microns throughout the crystal. The abscissa of the graph represents, on a linear scale, the distance in microns on either side of the interface 20, where the interface is identified at zero on the graph. The dimensions of the original substrate are illustrated to the left of zero, whereas the epitaxial layer dimensions are illustrated to the right of zero. The ordinate illustrates the impurity concentration profile, on a logarithmic scale, throughout the several regions of the silicon body.

The absolute magnitudes of the impurity concentrations and distances shown in the graph of Fig. 3 are those selected for an n-p-n silicon transistor capable of operating at very high frequencies. The features of the transistor that give such an operating characteristic are the very narrow base region and the electric field gradient in the base region as a result of an impurity concentration gradient. For example, a wafer is sliced from a single crystal ingot grown from a silicon melt into which is added both arsenic and boron to provide a boron concentration of about 5×10^{17} atoms/cm³ and an arsenic concentration of about 10^{18} atoms/cm³. The wafer (or substrate) is then sliced to a thickness of about 0.06 inch with the faces thereof lying approximately in the 1, 1, 1 crystal plane. After lapping and chemically polishing the faces of the wafer, it is placed in the furnace and heated to about 1250°C for epitaxial growth according to the Sigler publication, supra.

For the device under consideration, that being an n-p-n silicon transistor of narrow base region width, an epitaxial furnace of dimensions of about 2 inches in diameter and 10 inches long is supplied with a vapour mixture of hydrogen and impurity doped silicon tetrachloride. Referring again to Fig. 1 a mixing bottle is supplied from a first source of hydrogen doped with phosphene and a second source of hydrogen/silicon-tetrachloride mixture. The outlet of the mixing bottle is connected directly to the inlet of the furnace, and the source supplies are in ratios and are of flow rates to provide a flow into the furnace of about 40-50 litres/minute of hydrogen, with about 1% volume content of silicon-tetrachloride, and with a phosphene content of about 4-5 parts per billion parts of silicon-tetrachloride. That is, for every billion atoms of silicon-tetrachloride, there are 4-5 atoms of phosphene. As seen from Fig. 1 the phosphene is conveniently mixed with a separate supply of hydrogen initially, and the silicon-tetra-

chloride is likewise mixed with a separate supply of hydrogen, although the ultimate mixture is specified in terms of so many parts of phosphene per billion parts of silicon-tetrachloride. Reference is again had to the Sigler publication, supra, for details of an illustrative mixing apparatus.

The flow into the furnace is maintained for about 1 to 1½ hours while the wafer is maintained at the elevated temperature. Then the flow is stopped, the temperature of the wafer reduced to room temperature and the wafer removed from the furnace. This process produces a single crystal silicon layer grown on the face of the wafer the thickness of which is about 0.01 inch. The phosphorus concentration in the layer resulting from the epitaxial growth is about 10^{15} atoms/cm³. During the epitaxial growth, the boron diffuses from the wafer into the layer to a depth of about 2.0 microns, and is sufficient in concentration to compensate the phosphorus impurity to a depth of about 1.6 microns, at which depth there is formed a junction as shown in Fig. 3. Simultaneously, the arsenic diffuses from the wafer into the layer to a depth of about 0.7 micron, and is sufficient in concentration to compensate the boron impurity to a depth of about 0.1 micron, at which depth another junction is formed. From Fig. 3 it can be seen that the region 30 bounded by the junctions and in which the boron impurity predominates exhibits an impurity concentration gradient, the higher concentration being adjacent junction 26 and decreasing toward junction 24. Moreover, the narrowness of this region is apparent, being about 1.5 microns in width. Because of the simultaneous diffusion of both the boron and arsenic impurities, the width of this region can be very accurately governed, since the diffusion of each is subject to the exact same conditions, whereas diffusions in sequence permit error due to variations in diffusion conditions.

In the example above-described with reference to an n-p-n transistor, the original wafer and the region between the interface 20 and junction 26 constitute the high impurity concentrated emitter, the region 30 constitutes the graded base, and the region 28 constitutes the collector. A section is cut from the silicon body to provide a bar transistor as shown in Fig. 4, and suitable electrical connections 50, 52, and 54 are attached to the regions 28, 30 and 4, respectively.

The various times, temperature, impurities, impurity concentrations, flow rates, etc. specified above can be varied according to the desired device. For example, other impurities than those specified are well-known in the semiconductor art and can be used provided they are in the proper concentra-



tions for the corresponding diffusion coefficients. Moreover, semiconductor materials other than silicon can be used. If germanium is chosen as the semiconductor material, it is well understood that, in general, the same impurities that are effective in determining a particular conductivity type in silicon are also effective in determining the same conductivity type in germanium. However, the faster diffusing impurities in silicon generally are the slower diffusing in germanium. Compound semiconductors can also be used, and suitable impurities and their diffusion coefficients are well known. The requirements of the method of this invention state, however, that the relative concentrations and relative diffusion coefficients of the impurities used must be chosen to produce a pair of rectifying junctions in the semiconductor when simultaneously diffused into a region of conductivity type the same as the slower diffusing impurity. However, there are no particular requirements as to the depths to which the impurities must be diffused or the absolute concentrations thereof, as this will vary according to the particular device. In this connection the invention has been described with reference to an n-p-n silicon transistor of very narrow base width and the impurity concentration of which is graded throughout the base.

The flow rates and concentrations of the various constituents for the epitaxial process have been described with reference to a silicon n-p-n narrow base transistor. However, the Sigler publication, supra, discloses variations and modifications to these parameters, and it is expressly understood that the particular flow rates and concentrations given above are for illustrative purposes only. These parameters will vary according to the particular device under consideration.

The invention is not limited to the simultaneous diffusion of two impurities from the original substrate into the epitaxial layer, but, alternatively, the original substrate can be doped with a single impurity of relatively low concentration, such as about 10^{15} atoms/cm³ of phosphorus, and the vapourized epitaxial mixture can be doped with two opposite type impurities. Here, the migration of impurities by diffusion is from the epitaxial layer to form a part of rectifying junctions in the original substrate. In this event, the regions of the semiconductor body shown in Fig. 3 are reversed.

The advantages gained by fabricating the device by epitaxial growth are manifold as compared to older methods of simultaneously diffusing two impurities into a semiconductor body to form therein a pair of rectifying junctions. In the older methods of growing a portion of a semiconductor

body from a melt doped with a first impurity, and subsequently adding two opposite type impurities and continuing the growth while the impurities diffuse into the body, there is much difficulty encountered in controlling the exact concentration of the impurities. This is largely due to the segregation of the impurities in the melt upon freezing of the semiconductor during growth, and the non-uniformity of mixing of the impurities in the melt. Moreover, the junctions formed in a melt-grown process are curved due to the crystal growth, and thus the junction locations from the end of the crystal vary throughout the diameter thereof.

Another previous method includes the simultaneous diffusion of two impurities from the vapour state into a semiconductor body. It is common knowledge that it is very difficult to control accurately the concentration of the impurities at the surface of the body, where this concentration determines the concentration of the diffused impurity within the body.

In the present invention the concentrations of the various impurities can be very accurately controlled in the original substrate material and in the epitaxially grown layer. In fact, the impurity control that can be exercised by epitaxial methods far exceeds that possible by the older methods.

By using epitaxial methods, very little, if any, of the semiconductor material is wasted in production. Finally, the junction profiles are flat, in contrast to the older melt-grown method, because of the flat interface between the substrate and the epitaxial layer.

The invention is not intended to be limited to the specific details mentioned above in connection with the description of the preferred embodiment thereof, but modifications and substitutions within the scope of the invention as defined in the appended claims will become apparent to those skilled in the art.

WHAT WE CLAIM IS:—

1. A method of making a semiconductor device having therein two spaced rectifying junctions, said method comprising epitaxially depositing from the vapour phase a single crystal layer of semiconductor material on a single crystal substrate of said semiconductor material with inclusion one in each of the two consisting of said layer and substrate of two impurities determining the same conductivity type and of different concentrations and the further inclusion in that one of the two containing the greater impurity concentration of a further impurity of a concentration intermediate to those of the other two impurities, determining the opposite conductivity type, and of substantially greater diffusion coefficient than that of the impurity of said

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greater concentration, and simultaneously diffusing the two impurity concentrations in said one of the two across the boundary between the two to form said junctions in the other of the two.

2. A method according to claim 1, wherein said one of the two is the substrate.

3. A method according to claim 1, wherein said one of the two is the layer.

10 4. A method according to any preceding claim wherein said simultaneous diffusion is carried out simultaneously with said epitaxial deposition.

5. A method of making a semiconductor device having therein two spaced rectifying junctions, substantially as hereinbefore described with reference to the accompanying drawings.

6. A semiconductor device having therein two rectifying junctions and made by the method of any preceding claim.

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