

“Battery charging device”.

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DESCRIPTION

The present invention refers to a battery-charging device.

5 Battery chargers are generally known in the state of the technique, for example cellular telephone batteries, as batteries of the Litio.Ion type.

The charging of these batteries comes about according to a known constant current (CC) and constant voltage (CV) procedure. During the battery charging phase the charger works according to a current regulation
10 procedure, that is a constant current is supplied to the battery. In the meantime the voltage on the battery grows until it reaches its steady state charge value; in proximity of this value, the charge current starts diminishing until it nullifies itself and the charger enters the voltage regulation phase, that is the battery is supplied with a constant voltage.

15 Generally in this procedure high precision of the regulated current as well as the regulated voltage is required. The values generally required are 10% for the charge current and 1% for the regulated voltage. In addition it is necessary to control that the temperature of the device does not exceed the thermal limits also depending on the charger device used.

20 Among the various types of battery charger devices one that is generally used is shown in Figure 1.

The device comprises means CA, D2 suitable for regulating the current of a battery LOAD, means VA, D1 suitable for regulating the voltage and means PA, D3 suitable for regulating the power.

25 The device comprises a couple of PMOS transistors M1 and M2 having the source terminal connected to an input voltage V_{in} ; the drain terminal of the transistor M2 is connected to the battery LOAD having its other terminal connected to ground and the drain terminal of the transistor M1 is connected to the source terminal of a transistor M3. The latter has the
30 drain terminal connected to a resistor R having its other terminal connected

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to ground. The gate terminal of the transistor M3 is driven by an operational amplifier 1 having the inverting and non-inverting input terminals connected respectively to the drain terminals of the transistors M1 and M2.

5 A current generator I1 and the cathodes of the diodes D1-D3 having the anodes connected to the respective operational error amplifiers VA, CA and PA are connected to the gate terminals of the transistors M1 and M2. The amplifier VA has in input on the inverting terminal a reference voltage Vref and on the non-inverting terminal the voltage Vout at the terminals of the battery LOAD, the amplifier CA has in input on the inverting terminal a
10 reference voltage V1 and on the non-inverting terminal the voltage Vout and the amplifier PA has in input on the inverting terminal the temperature of the charger device Tdie and on the non-inverting terminal a reference temperature Tref.

During the charging phase of the battery LOAD there is the current
15 regulation phase; the control of the PMOS transistors M1 and M2 is carried out by the error amplifier CA because the error amplifier VA is unbalanced, the voltage Vout being less than the voltage Vref. When the voltage Vout reaches the voltage Vref, the control of the transistors M1 and M2 passes to the amplifier VA that supplies all the current needed to directly bias the
20 diode D1 while the diode D2 is cut off.

If the temperature of the charger device is higher than the reference temperature Tref, the control passes to the amplifier PA that directly biases the diode D3.

25 So that the regulated current on the charge is very precise the voltages between drain and source of the MOS transistors M1 and M2 have to be equal to each other. As both the MOS transistors have the same voltage between the gate and source terminals, the charge current is equal to that of reference $\frac{V1}{R}$ multiplied by the ratio of the areas of the MOS transistors M1, M2. For this reason the amplifier 1 is introduced to maintain the drain

terminals of the transistors M1 and M2 at the same potential.

In view of the state of the technique, object of the present invention is to provide a battery-charging device that has a simpler circuitry than that of known chargers and that in addition has greater precision.

5 In accordance with the present invention, this object is achieved by means of a device suitable for charging a battery comprising at least a first and a second transistor, said transistors being connected to an input voltage and having output terminals, the output terminal of said first transistor being connected to said battery, said device comprising a drive circuit of said
10 transistors, said drive circuit comprising first means suitable for regulating the current in said battery during the charging phase of said battery, characterised in that said first means are suitable for keeping the voltage on the output terminals of said transistors the same during the charging phase of said battery.

15 Thanks to the present invention a battery charging device can be produced which has a lower number of components and a lower occupation of area in the chip where the device is integrated. With said device we also have high precision in the phases of regulating the current and the voltage in the battery.

20 The characteristics and the advantages of the present invention will appear evident from the following detailed description of an embodiment thereof, illustrated as non-limiting example in the enclosed drawings, in which:

 Figure 1 shows a battery charger in accordance with the known art;

25 Figure 2 shows a diagram of a battery charger according to the present invention;

 Figure 3 shows a circuit implementation of the battery charger of Figure 2;

30 Figure 4 shows the diagrams of the time trend of the voltage V_{out} , of the output current I_{out} and of the temperature T_p in the charging phase of

the battery obtained with the device of Figure 3 in the case that no regulation of the temperature is carried out;

Figure 5 is an enlargement of a part of the diagram of the time path of the current I_{out} of Figure 4;

5 Figure 6 shows the diagrams of the time trend of the voltage V_{out} , of the output current I_{out} and of the temperature T_p in the charging phase of the battery obtained with the device of Figure 3 in the case that regulation of the temperature is carried out.

With reference to Figure 2 a diagram of a battery-charging device
10 according to the present invention is shown. The device comprises a couple of PMOS transistors M10 and M20 having the source terminal connected to an input voltage V_{in} . The drain terminal of the transistor M10 is connected to the battery LOAD having its other terminal connected to ground. The charging device comprises a circuit 100 suitable for driving the gate
15 terminals of the transistors M10 and M20. The drain terminal of the transistor M20 is also connected to circuit 100; more precisely said terminal is connected to the drain terminal of a transistor M30 being part of a current mirror M30-M31. Said current mirror is suitable for mirroring on the
20 transistor M10 the current I_{30} proportional to the current I_{ref} coming from a homonymous current generator. The latter is controlled by an operational amplifier PA1 having in input on the inverting terminal the reference voltage V_{ref2} and on the non-inverting terminal a voltage $V(T)$ proportional to the
25 temperature of the device; the voltage $V(T)$ is produced by a device 2 that is sensitive to the temperature. When the temperature of the device increases and the voltage $V(T)$ becomes the same as the voltage V_{ref2} , the amplifier PA1 acts commanding a decrease of the current I_{ref} . Consequently the
30 current I_{30} and the charge current that flows in the transistor M10 are also decreased. Consequently the power dissipated in the transistor M10 decreases and this also makes the temperature of the device decrease; the intervention of the amplifier PA1 occurs until the balance between the

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temperature of the device and the current in transistor M10 that produces this temperature is reached.

The drain terminals of the transistors M10 and M20 are connected to the non-inverting and inverting input terminals of an operational error
5 amplifier CA1 belonging to the drive circuit 100. The output of the amplifier CA1 converges with the output of an operational error amplifier VA1 on a circuit block CVA whose output signal is suitable for driving the transistors M10 and M20. The amplifier VA1 has in input on the inverting terminal a reference voltage V_{ref1} and on the non-inverting terminal the voltage V_{out}
10 at the terminals of the battery LOAD. The non-inverting input of the amplifier CA1 is connected to the terminal to regulate, that is the drain terminal of the transistor M10: in this manner the loop constituted by the amplifier CA1, by the circuit block CVA and by the transistors M10 and M20 being in equilibrium, maintains the voltages on the drain terminals of
15 the transistors M10 and M20 at the same value for the whole time in which the voltage V_{out} grows towards its steady state value V_{ref} , without the need to provide a further amplification stage. The regulated current is thus exactly the same as the reference current I_{ref} multiplied by the ratio of the areas of the transistors MOS M10 and M20. The circuit block CVA is equivalent to
20 an adder node whose output signal coincides with the output signal from the amplifier CA1 or with the output signal from the amplifier VA1 when one or the other are active. The amplifier CA1 has a bias current I_{pol} controlled by the output signal of the amplifier VA1.

During the current regulation, the voltage V_{out} increases until it
25 reaches the reference value V_{ref1} . When this comes about, the system gradually reduces the bias current I_{pol} of the stage CA1 to zero so that the active regulation loop becomes that of voltage, constituted by the amplifier VA1, by the block CVA and by the MOS transistors M10 and M20.

A circuit implementation of the device of Figure 2 is shown in Figure
30 3. When the battery LOAD is discharged, the voltage V_{out} is less than the

reference voltage V_{ref} , the amplifier VA1 is unbalanced and the error amplifier CA1 is biased by the current I_{pol} by means of the mirrors formed by the PMOS transistors M41-M42 and by the NMOS transistors M43-M44. This current is also mirrored in the NMOS transistor M49, at the output of the stage CVA, by means of NMOS transistor mirrors M44-M45, PMOS transistor mirrors M46-M47 and NMOS transistor mirrors M48-M49.

The differential stage of the amplifier CA1, constituted by the PMOS transistors M51-M52 whose gate terminals are connected to the drain terminals of the transistors M20 and M10, sees to regulating the charge current in the battery LOAD by means of transistor mirror M53-M54 which, sending the signal to the output stage CVA, generates in the transistor M55, by means of the current mirror M60-M55, a current that balances the current of the transistor M49; in this manner the equilibrium of the currents is obtained. The drain terminal of the transistor M51 is connected to a transistor M61 in diode connection, connected in turn to ground.

The amplifier VA1 comprises a differential stage with PMOS transistor M62-M63; on the gate terminals of said transistors there are respectively a part of the voltage V_{out} given by $\frac{V_{out} \times R2}{R1 + R2}$ and the reference voltage V_{ref1} . The source terminals of the transistors M62 and M63 are connected to a generator of the bias current I_{pol} and the drain terminals are connected respectively to the drain terminals of the transistors M44 and M56.

It should be noted that, in current regulation, the amplifier VA1 has no effect because of its unbalance that prevents the passage of current in the current mirror formed by the NMOS transistors M56-M57.

The amplifier PA1 comprises a differential stage with PMOS transistor M64 and M65 and a current mirror of NMOS transistor M66-M67. The source terminals of the transistors M64 and M65 are connected to a generator of the bias current I_{pol2} and the drain terminals are connected

respectively to the drain terminals of the transistors M66 and M67. The gate terminals of the transistors M64 and M65 are connected to a reference voltage Vref2 and to the voltage V(T) and the drain terminal of the transistor M64 is connected to the gate terminal of the transistor M58.

5 If the temperature of the system is such that the signal $V(T) = K \times T$ is less than Vref2, the amplifier PA1 is unbalanced and turns off the transistor M58. Thus the reference current Iref is entirely mirrored in the transistor M20 and, during the entire charging phase of the battery, the regulated current is exactly a multiple of the current Iref, as the amplifier CA1 sees to
10 equalling the drain-source voltages of the transistors M10 and M20.

If the temperature of the system is such that V(T) reaches Vref2, the stage PA1 tends to subtract a part of the current Iref at the mirror M30-M31. Consequently the charge current is less than its nominal value and it will settle itself at a value that balances the temperature of the device Tj
15 according to the formula:

$$Tj = Tamb + (Vin - Vout) \times Iout \times \theta$$

where Tamb is the temperature outside the system, Iout is the charge current and θ is the thermal resistor of the package of the device.

The temperature loop, being dynamically slow because of the reaction
20 times of the package, has a dominating pole almost at the origin and has no need for compensation.

When the voltage Vout reaches the reference voltage Vref1, the amplifier VA1 balances itself and the NMOS mirror transistor M56-M59 tends to subtract the bias current Ipol of the amplifier CA1 which then turns
25 off. In this manner the stage VA carries out the voltage regulation of the output.

The compensation of the regulation loop current/voltage has been carried out by means of a Miller capacitor connected between the gate and the drain terminals of the transistor M20.

30 Figure 4 shows time graphs of the voltage Vout, of the output current

I_{out} and of the temperature T_p in the charging phase of the battery, with an input voltage V_{in}=5V and an external temperature of 25° C. The charge current is programmed at 0.5A. The maximum junction temperature set by specification is T_j=120° C. In this case it can be seen that the temperature of the system is lower and thus the charge current is equal to that programmed. In voltage regulation the charge current decreases until it annuls itself and the regulated voltage on the battery is 4.1V, as per specification.

Figure 5 shows an enlargement of the charge current of the battery I_{out} during the current regulation. The excellent precision, which is 0.2%, is highlighted.

Figure 6 shows time graphs of the voltage V_{out}, of the output current I_{out} and of the temperature T_p in the charging phase of the battery when V_{in}=12V at an external temperature of 25° C. As before, the current is programmed at 0.5A. In this case the temperature of the device is regulated at 120° C, lowering the charge current to approximately 0,24A.

CLAIMS

1. Device suitable for charging a battery comprising at least a first (M10) and a second (M20) transistor, said transistors (M10, M20) being connected to an input voltage (V_{in}) and having output terminals, the output terminal of said first transistor (M10) being connected to said battery (LOAD), said device comprising a circuit (100) for driving said transistors (M10, M20), said drive circuit (100) comprising first means (CA1) suitable for regulating the current (I_{out}) in said battery during the charging phase of said battery (LOAD), characterised in that said first means (CA1) are suitable for keeping the voltage on the output terminals of said transistors (M10, M20) the same during the charging phase of said battery (LOAD).
2. Device according to claim 1, characterised in that said first means (CA1) comprise an operational amplifier having the inverting and non-inverting input terminals connected to the output terminals of said transistors (M10, M20), said operational amplifier being suitable for driving said transistors (M10, M20) to provide a constant current to said battery (LOAD).
3. Device according to any of the previous claims, characterised in that said drive circuit (100) comprises further means (VA1) suitable for regulating the voltage (V_{out}) of said battery when the voltage of said battery has reached a reference voltage (V_{ref}).
4. Device according to any of the previous claims, characterised in that said further means (VA1) are suitable for turning off said first means (CA1) when the voltage (V_{out}) of the battery has reached said reference voltage (V_{ref}).
5. Device according to any of the previous claims, characterised in that said drive circuit (100) comprises second means (M30-M31, I_{ref} , PA1) connected to the output terminal of said second transistor (M20) and suitable for setting the current that flows through said second switch means.
6. Device according to claim 5, characterised in that said second

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means (M30-M31, Iref, PA1) comprise means (PA1) suitable for varying the current (I30) on said second transistor (M20) in function of the temperature of the device.

- 5 7. Device according to claim 6, characterised in that said second means (M30-M31, Iref, PA1) comprise a current generator (Iref), means (2) sensitive to the temperature and suitable for producing a voltage (V(T)) in function of the temperature of the device and means (PA1) suitable for comparing the voltage (V(T)) produced by said sensitive means with a further reference voltage (Vref2) and varying the current (I30) on said
10 second transistor (M20) in function of said comparison.