AUDIO POWER CONVERSION SYSTEM

Technical Field

This invention relates to AC-AC and DC-AC conversion for Audio where the inverter stage (DC-AC) is a Single-Ended class D stage (switching amplifier).

The AC-DC stage is preferable a Switch Mode Power Supply but the invention also relates to an Audio power conversion system using linear power supply techniques.

Technical Background

The two predominant topologies used for class D amplifiers are the full-bridge- and the half-bridge topology. A prior art setup of these two topologies including power supply is shown in Fig. 2 and Fig. 3.

For low cost consumer products the half-bridge topology has a distinct advantage over the full-bridge since only half the number of power switches, drivers and output inductors is needed. Even though the voltage rating of the power switches is doubled in the half-bridge topology, there is still a manufacturing and cost benefit of the reduction. Since the speaker output terminals are referenced to ground, overload protection and output sensing becomes easier compared to the full-bridge topology.

The drawback of the half-bridge class D topology is the need for a dual rail supply and the fact that this topology will pump current back to the opposite supply rail from where the power is being drained. As shown in fig. 4 the negative rail capacitor C2 will be charged by the output inductor current during the interval $t \in [DT;T]$.

The charge delivered to back to the rail is dependent on load impedance, audio frequency, power level and rail voltage. These dependencies can be expressed as:

$$\Delta Q = \int_0^{t_{Audio}} \frac{V_{Peak} \cdot \sin(2 \cdot \pi \cdot f_{Audio} \cdot t)}{2 \cdot R_{Load}} - \frac{(V_{Peak} \cdot \sin(2 \cdot \pi \cdot f_{Audio} \cdot t))^2}{2 \cdot R_{Load} \cdot V_{Rail}} \cdot dt \qquad (1)$$

$$\Delta Q = \frac{2 \cdot V_{Audio} - \frac{\pi \cdot V_{Audio}^2}{2 \cdot V_{Rail}}}{4 \cdot \pi \cdot f_{Audio} \cdot R_{Load}} \qquad (2)$$

The worst case pumping can be found by solving dQ/dVAudio=0 for (2):

$$\frac{dQ}{dV_{Audio}} = \frac{2 \cdot V_{Rail} - \pi \cdot V_{Audio}}{2 \cdot \pi \cdot f \cdot V_{Rail}} = 0 \Leftrightarrow V_{Audio} = \frac{2}{\pi} \cdot V_{Rail} \quad (3)$$

The worst case charge can then be found by inserting (3) into (2):

$$\Delta Q_{Max} = \frac{V_{Rail}}{2 \cdot \pi^2 \cdot f_{Audio} \cdot R_{Load}} \quad (4)$$

Capacitor minimum size for a given rail voltage rise (a fraction of nominal rail voltage) can then be found as:

$$C_{Min} = \frac{1}{2 \cdot \pi^2 \cdot f_{Audio} \cdot \Delta V_{relative}} \quad (5)$$

Figure 5 shows an example with a 20Hz audio signal and an 4ohm load impedance where the minimum rail capacitance is determined as a function of the allowable rail perturbation. If we allow for a 20% increase in rail voltage the minimum capacitance/channel/rail is approximately 3000uF. For a stereo setup with a single-ended class D amplifier, the requirement will be 4pcs 3300uF capacitors to keep rail voltages within 20%. The resulting rail variation for the above example is shown in Fig. 5. The nominal rail voltage is 40VDC and the perturbed rail is increased with approximately 8V (20%). The audio signal is equal to $2/\pi$ of the nominal rail voltage which is the worst case situation.

Also performance of the amplifier will be affected by the rail pumping especially non-feedback class D amplifiers where the asymmetrical rail perturbation will be modulated directly onto the audio signal dramatically increasing the distortion. Because of the dual supply with asymmetrical perturbation, any feed-forward system implemented will have little or no effect.

The benefits in terms of component count and complexity of using the single-ended class D amplifier compared to the full-bridge class D amplifier are quickly disappearing when taking into account the problems introduced by the rail pumping phenomena discussed above. These drawbacks can be summarized as:

- Excessive use of rail capacitors => higher cost and larger physical size
- Higher voltage-rated devices in terms of rail Capacitors and amplifier MOSFETs => higher cost and larger physical size

- Unacceptable audio performance for non-feedback class D amplifiers and degraded audio performance for feedback class D amplifiers => reduced product value

A voltage equalization scheme for a single-ended class D amplifier is suggested in WO 2005/091497. This circuit suffers from several disadvantages not encountered in the invention. Some of the disadvantages are:

1) The circuit redistributes the pumping energy in a 2 step operation. In the first step energy is stored in an inductor to be released in the second step.

2) The circuit uses two separate control systems.

3) The circuit will only limit the rail pumping – not cancel it.

4) The circuit will not help utilizing rail capacitance on both rails.

5) The circuit is based on a "buck-boost" topology renowned for its poor conversion efficiency.

If the rail pumping is to be effectively cancelled, a not insignificant amount of power has to be recycled between the rails. From (4) we can calculate the worst case average power that has to be converted from one rail to the other:

$$P_{Av_Pumping} = \frac{V_{Rail}^2}{\pi^2 \cdot R_{Load}} \qquad (6)$$

Introducing the maximum modulation index, MMax, as the fraction of maximum output voltage to rail voltage, the relation between average pumping power and maximum output power can be found as:

$$\frac{P_{Av_Pumping}}{P_{Max_Rload}} = \frac{2}{\pi^2 \cdot M_{Max}^2} \qquad (7)$$

In a stereo setup of 2x125W in 4ohm with rail voltages of +/-40V and a maximum modulation index of 0.85, the average power to be redistributed in the worst case situation is approximately 81W which accounts for 32% of the power delivered to the load!

To benefit from the advantages of using the single-ended class D amplifier the rail pumping problem needs to be addressed in an intelligent manner adding minimum complexity and cost to the audio power conversion system.

Objects of the invention

It is the objective of the invention to provide an audio power conversion system with:

1) Improved system performance, by eliminating or reducing the supply pumping thus improving supply quality leading to better audio performance.

2) Reduced complexity, since the invention enables all the benefits of the single-ended structure without introducing the classical problems that arises with the rail pumping phenomena.

Furthermore, in some embodiments the invention will also provide:

3) Improved system efficiency, by a combination of reducing the rail pumping thus reducing the peak-to-average power ratio of the power supply, and the single-ended structure of the class D amplifier (only 1 semiconductor in the power path).

4) Improved EMI performance, since the invention enables use of soft-switching techniques (ZVS, ZVC) which have a beneficial impact on the generated high frequency noise.

Summary of the invention

The objects of the invention are achieved by an audio power conversion system comprising a power supply having a positive supply rail and a negative supply rail for supplying power to a single ended class D amplifier. The system further comprises a supply pump reduction circuit connected to the supply rails, adapted to redistribute a pumping charge from said power supply by forcing a current-flow from a rail with a higher voltage to a rail with a lower voltage.

The core engine in the invention is the supply pump reduction circuit. The circuit works as a Supply Rail Mirror (SRM) which basically mirrors the voltage of the numerical smallest value to the other rail at any given time. In case of rail pumping, the SRM circuit will mirror the supply rails by redistributing the pumping charge in such a manner that supply rails will become essential equal numerically.

In the prior art, rail pumping is effected during two cycles, where the first cycle only can redistribute charge from the positive rail to the negative rail and the second cycle only can redistribute charge from the negative rail to the positive rail. For practical circuits this means that only the first or the second cycle is effective in redistributing the charge.

According to the current invention, the redistribution circuit is arranges to always distribute charge from the rail with the higher voltage. This means that for practical circuits the pump canceling occurs continuously and is not confined to every other cycle as for the prior art.

This also relates to how efficient the pump cancel circuits are: if the same amount of charge is to be redistributed by the invention and the prior art, the prior art will have to move twice the pumping charge in every cycle since only every second cycle is active. This corresponds to significant higher rms-currents in the prior art compared to the invention with loss of efficiency as a result.

Another advantages with the present invention is the simplicity of the circuit and the control. Because of the SRM topology and the self adjusting property of this approach, no control circuits are needed and any pumping resulting in rail voltage changes are corrected in an autonomous way.

The supply pump reduction circuit preferably comprises a high frequency transformer having a first and a second winding alternatingly connectable during a first and second cycle to said positive and negative supply rails, so as to cause a current to migrate from the rail with the highest voltage to the rail with the lowest voltage, while balancing said transformer. A transformer is a convenient way to realize a self adjusting redistribution circuit according to the present invention. The transformer windings will be connected differently during the two cycles so as to balance the transformer.

The supply pump reduction circuit can further comprise switching means for connecting, during said first cycle, said first winding between said positive supply rail and ground, and said second winding between said negative supply rail and ground, and, during said second cycle, said second winding between said positive supply rail and ground, and said first winding between said negative supply rail and ground.

Such switching will effectively mirror the two supply rails onto each other. This has two distinct advantages. Firstly, any variation in the two rail voltages is equalized (pump canceling). Secondly, this circuit effectively utilizes the capacity of both rails which means that dynamic power delivered from the rail capacitors becomes equal to that utilized in a single rail supply with the same amount of capacity.

The switching means can comprise controlled switches, such as MOSFETs. The simple drive pattern of the MOSFETs also enables a simple way to implement soft-switching techniques of the transistors. The circuit can then comprise a switch control system for providing two pulse trains with equally spaced, non-overlapping pulses of equal length, for controlling the controlled switches

Further more, the circuit may include a separation filter that enables the SRM unit to be coupled to any dual rail supply while maintaining the soft-switching characteristics.

The switching means can also comprise uncontrolled switches like diodes, to reduce complexity. This version also enables soft-switching techniques.

The supply pump reduction circuit can be integrated in the main power supply for the single-ended class D amplifier. Such an integrated circuit will both supply the power to the amplifier while redistributing the pumping energy. The soft-switching characteristics can be maintained in this circuit by adapting the simple control scheme of the basic SRM converters.

Brief description of the drawings

The preferred embodiment of the present invention will be further described in the following, with reference to the appended drawings.

Fig. 1 shows a prior art audio power conversion system using a single-ended class D amplifier

Fig. 2 shows a prior art combination of a single rail power supply and a bridged class D amplifier

Fig. 3 shows a prior art combination of a dual rail power supply and a single-ended class D amplifier.

Fig. 4 shows the mechanism behind the supply pumping effect

Fig. 5 is a graph of rail capacitance as a function of voltage rail excursion for a 4 ohm load 20Hz worst case audio signal.

Fig. 6 is a simulation of the rail pumping in case of a 20Hz worst case audio signal in a 4 ohm load with 3300uF on each rail.

Fig. 7 shows an audio power conversion system with a supply pump canceling circuit attached to the supply rails (SRM).

Fig. 8 shows a preferred embodiment of the invention.

Fig. 9 same as Fig. 8 but with a rail separation filter added.

Fig. 10 shows another preferred embodiment of the invention.

Fig. 11 shows a block diagram of the pump canceling converter integrated in the main power supply.

Fig. 12-14 shows preferred embodiment of the invention as shown in Fig. 11.

Fig. 15 shows the timing of the control signals for the switches in the preferred embodiments.

Fig. 16 shows the effect of adding a pump canceling circuit to a system wit a 2x125W in 4 ohm with no (or little) output capacitors.

Detailed description of a preferred embodiment

A block schematic of an audio power conversion system is shown in Fig. 1. The power supply (1) can be a switched mode supply or a linear type. Depending on the type of amplifier the supply is sourcing the output will be either a single rail or a dual rail supply. The class D amplifier (2) will typically be a half-bridge (single-ended) or a full-bridge topology. The number of channels in (2) can vary from 1 to multiple channels. The load (3) is typically an electro dynamic loudspeaker but can be any kind of transducer transforming the electrical signal from the amplifier to an acoustic signal. The power source (4) can be an AC-source, e.g. the utility net, or it could be a battery (e.g. automotive, portable equipment). The output of the power source (4) is a DC-voltage (or almost) which means that in case of an AC-source input, means to rectify and stabilize the voltage is included in (4). The electrical part of the audio power conversion system is defined as (3).

Given that the class D amplifier (2) is a single-ended type, the power supply (1) to support this topology will be a dual rail supply. The key object of the invention is to overcome the rail pumping problem discussed previously in an intelligent way such that the single-ended class D amplifier structure becomes more attractive. In a preferred embodiment of the invention the SRM (6) (Supply Rail Mirror) converter operates in parallel with the power supply (2).

A preferred implementation of the invention is shown in Fig. 8. The positive supply rail is connected to the junction between a first capacitor (15) and the drain-terminal of a first pair of MOSFETs (8) and (9). The source terminal of (8) is connected to a first terminal on a first transformer winding (12), and the source terminal of (9) is connected to a first terminal on a second transformer winding (13). The second terminal of the two transformer windings, (12) and (13), are connected to a common point (0). The two windings are coupled to each other through a transformer core of magnetic material (14). The negative supply rail is connected to the junction between a second capacitor (15) and the source-terminal of a second pair of MOSFETs (10) and (11). The drain terminal of (10) is connected to the junction between the transformer winding (12), and the source terminal of (8). The drain terminal of (11) is connected to the junction between the transformer winding (13), and the source terminal of (9). The two capacitors are connected to the two transformer windings in a common point (0).

When operational and the transistors 8-11 is turned ON/OFF according to Fig. 15, the circuit will cancel the supply pumping by mirroring the two supply rails on to each other. In a first cycle, the transistors 8 and 11 will be turned ON. The positive supply rail across the capacitor 15 will then be put across the transformer winding 12.

Likewise, the negative supply voltage on the capacitor 16 will be put across the transformer winding 13. Since the two windings are coupled to each other in a 1:1 ratio, any difference in the magnitude of the positive and negative rail voltage will cause a load current to migrate from the rail with the largest magnitude to the other rail. In the next cycle the same operation is performed but now with transistor 9 and 10 turned ON. This action secures the balancing of the transformer 14.

In a preferred embodiment of the invention the transistors 8-11 is turned ON and OFF under Zero Voltage Switching (ZVS) condition. By switching the transistors under this condition, losses associated with the ON and OFF transitions can be omitted. It is possible to achieve Zero Voltage Switching of the transistors by adjusting the magnetizing inductance of the transformer configuration (14) in such a way that the voltage across the transistors is fully reversed before the next transition occurs. To allow the ZVS to be completed it is necessary to have a small dead time between the transistor turn ON signals as shown in Fig. 15.

The magnetizing current needed to fully reverse the voltage across the transistors within the dead time window is given by:

$$I_{Magnetizing} \geq C_{Node} \cdot \frac{V_{DS}}{t_{Dead_time}} \qquad (8)$$

, where C_{Node} is the accumulated capacitive load of the circuit node and V_{DS} is the magnitude of the voltage in this particular node that has to be reversed within the dead time. Equation (8) is an approximation and is only valid as long as the dead time is much smaller than the switch on-time. One should also keep in mind that the C_{Node} capacitance can be highly voltage dependent (e.g. output capacitance of MOSFETs and Anode-cathode capacitance of diodes)

The magnetizing current translates into a magnetizing inductance of:

$$L_{Magnetizing} \leq \frac{V_{DS} \cdot t_{ON}}{2 \cdot I_{Magnetizing}} \qquad (9)$$

Substituting (8) into (9):

$$L_{Magnetizing} \leq \frac{t_{Dead_time} \cdot t_{ON}}{2 \cdot C_{Node}} \qquad (10)$$

The magnetizing inductance of the non-ideal transformer (14) can then be used to facilitate the ZVS transition. Since practical transformer also exhibits non-ideal coupling between windings, this uncoupled transformer flux can be regarded as a parasitic inductance in series with the transformer windings. This inductance is normally referred to as leakage inductance.

According to the invention it is also possible to shape the current in the SRM so that Zero Current Switching (ZCS) is possible (disregarding transformer magnetizing current). The ZCS is possible by creating a resonant tank using the transformer leakage inductance and the capacitors 15 and 16. The current resonance must go through a full-wave oscillation which means that the ideal current shape will be that of a squared sinusoidal. The resonant tank must obey:

$$t_{ON} \cong 2 \cdot \pi \cdot \sqrt{L_{Leakage} \cdot (C_{15} + C_{16})} \quad (11)$$

In some applications it is not possible to control the values of the capacitors 15 and 16 to accommodate the resonant current transition. In such a case one can according to the invention apply a filter that separates the capacitors 15 and 16 from the power supply rails in terms of high frequency influence (Fig. 9). The separation is done by adding the inductor 17 between the capacitor 15 and the positive supply rail and adding the inductor 18 between the capacitor 16 and the negative supply rail. In this way the HF behaviour of the circuit and thereby the resonance frequency between the capacitors 15 and 16 and the leakage inductance can be controlled.

Another preferred embodiment of the invention is shown in Fig. 10. The transistors 30 and 31 form a half-bridge configuration with the capacitors 28 and 29. The transformer winding 23 is connected between the junction of transistor 30, 31 and capacitors 28, 29. The first terminal of transformer winding 21 is connected to the anode of diode 26 and the cathode of diode 25. The second terminal of transformer winding 22 is connected to the anode of diode 27 and the cathode of diode 24. The second terminal of transformer windings 21 and the first terminal of transformer winding 22 are connected together and to the common point 0. The cathodes of diodes 26 and 27 are connected to the junction of capacitor 28, transistor 31 and capacitor 33 which again is connected to the positive supply rail. The anodes of diodes 24 and 25 are connected to the junction of capacitor 29, transistor 30 and capacitor 32 which again is connected to the negative supply rail. The junction of capacitor 33 and 32 is connected to the common point 0.

The transistors are operated according to Fig. 15 with non-overlapping near 50% duty-cycle. In case of supply pumping either the voltage across capacitor 33 or

32 will increase. This voltage increase will also be found on capacitors 28 and 29 but because of the circuit configuration the voltage increase will be split between the two of them. Turning ON the transistor 30 will put the capacitor 29 voltage across the transformer winding 23. If the capacitor 33 is being pumped, current from capacitor 29 will be transformed through winding 23 to winding 22 and charge capacitor 32 through the diode 24. In the next cycle, transistor 31 will put the capacitor 28 voltage across the transformer winding 23. Assuming that the capacitor 33 is being pumped, current from capacitor 28 will be transformed through winding 23 to winding 21 and charge capacitor 32 through the diode 25. Pumping of the capacitor 32 will result in similar operation as described above but with the diodes 26 and 27 being active instead of diodes 24 and 25.

As for the previous implementation of the invention, this circuit also facilitates ZVS of the transistors in a similar manner.

ZCS operation of the circuit shown in Fig. 10 is also possible. The resonant tank in this circuit is formed by the capacitors 28 and 29 together with the leakage inductance of transformer 14. The resonant current is a half-wave sinusoidal and will result in a Zero Current Switching (ZCS) transition if:

$$t_{ON} \cong \pi \cdot \sqrt{L_{Leakage} \cdot (C_{28} + C_{29})} \qquad (12)$$

Another preferred embodiment of the invention is shown in Fig. 11. In this implementation, the SRM and the power supply is integrated into one stage. All of the implementations of the invention presented until now can be changed into a power supply with integrated SRM. The transformation is quite simple and is done by adding a winding (or windings) to the transformer configuration (14).

A preferred embodiment of the invention where the power supply and the SRM has been integrated can be seen in Fig. 12. The additional circuitry compared to the stand alone SRM shown in Fig. 9 can easily be identified as two additional transformer windings 34 and 35 and a push-pull configuration implemented by the transistors 36 and 36. The invention is not limited to use push-pull primary circuits but can be implemented as any primary-side referenced circuits like the half-bridge configuration shown in Fig. 13 and the full-bridge configuration shown in Fig 14.

As discussed previously Fig. 6 shows the rail voltage variation for a stereo setup with 2x125W in 4 ohm. The rail capacitance in this example was 2x3300uF on each rail (4x3300uF total). By adding the pump cancelling circuit shown in Fig. 9 and removing the rail capacitors (2x22uF remaining) the voltage variations have practical

disappeared as shown in Fig. 16. The slight variation that can be seen is caused by resistive voltage drops in the non-ideal switches, inductors and transformer windings.

CLAIMS

1. An audio power conversion system (3) comprising:

a power supply (1) having a positive supply rail (100) and a negative supply rail (200) for supplying power to a single ended class D amplifier (2),

characterized by

a supply pump reduction circuit (6) connected to the supply rails (100, 200) and adapted to redistribute a pumping charge from said power supply by forcing a current-flow from a rail with a higher voltage to a rail with a lower voltage.

2. The system according to claim 1, wherein said supply pump reduction circuit comprises a high frequency transformer having a first and a second winding alternatingly connectable during a first and second cycle to said positive and negative supply rails (100, 200), so as to cause a current to migrate from the rail with the highest voltage to the rail with the lowest voltage, while balancing said transformer.

3. The system according to claim 2, wherein said supply pump reduction circuit further comprises switching means for connecting, during said first cycle, said first winding between said positive supply rail and ground, and said second winding between said negative supply rail and ground, and, during said second cycle, said second winding between said positive supply rail and ground, and said first winding between said negative supply rail and ground.

4. The system according to claim 2 or 3, further comprising capacitors (15, 16) connected in parallel with said first and second transformer windings.

5. The system according to claim 3, said switching means comprises controlled switches (8, 9, 10, 11).

6. The system according to claim 5, further comprising a switch control system for providing two pulse trains with equally spaced, non-overlapping pulses of equal length, for controlling said controlled switches.

7. The system according to claim 6, wherein the control pulses are PWM modulated

8. The system according to any one of claims 3 - 7, said switching means further comprises uncontrolled switches (24, 25, 26, 27).

9. The system according to claim 1, wherein said supply pump reduction circuit (6) comprises:

a transformer having a first and a second transformer winding (12, 13),

a first capacitor (15) connected between a first common point (0) and a second

common point (100),

a first switch connected between said second common point (100) and a first terminal of the first transformer winding (12),

a second switch connected between said second common point (100) and a second terminal of the second transformer winding (13),

a second capacitor (16) connected between said first common point (0) and a third common point(200),

a third switch (10) connected between said third common point (200) and said first terminal on said first transformer winding (12),

a fourth switch (11) connected between said third common point (200) and said second terminal on said second transformer winding (13) and

wherein a second terminal of said first transformer winding (12) and a first terminal of said second transformer winding (13) are connected to said first common point (0).

10. (FIG 9) The system according to claim 9, wherein said supply pump reduction circuit (6) further comprises:

a first separation filter inductor (17) connected between a first common point (100) and the positive supply rail and

a second separation filter inductor (18) connected between a second common point (200) and the negative supply rail.

11. (FIG 10) The system according to claim 1, wherein said supply pump reduction circuit (6) comprises:

a transformer having a first, a second and a third transformer winding (21, 22, 23),

a first capacitor connected between a first common point (0) and a second common point (100),

a first diode (26) having a cathode connected to said second common point (100) and an anode connected to a first terminal of said first transformer winding (21),

a second diode (27) having a cathode connected to said second common point (100) and an anode connected to a second terminal of a second transformer winding (22),

a second capacitor connected between said first common point (0) and a third common point (200),

a third diode (24) having an anode connected to said third common point (200) and a cathode connected to said second terminal of said second transformer winding (22),

a fourth diode (25) having an anode connected to said third common point (200) and a cathode connected to said fist terminal of said first transformer winding (21),

wherein a second terminal of said first transformer winding (21) and a first terminal of said second transformer winding (22) are connected to said first common point (0),

a third capacitor (28) connected between said second common point (100) and a first terminal of said third transformer winding (23),

a fourth capacitor (29) connected between said first terminal of said third transformer winding and said third common point (200),

a first switch (31) connected between said second common point (100) and a second terminal of said third transformer winding (23), and

a second switch (30) connected between said second terminal of said third transformer winding and said third common point (200).

12. The system according to any one of the preceding claims, wherein said supply pump reduction circuit (6) is integrated in the power supply (7).

13. The system according to claim 9, wherein said transformer has a third and a fourth transformer winding (34, 35), and wherein said supply pump reduction circuit (6) further comprises:

a fifth switch (36) having a first terminal connected to said third transformed winding (34) and a second terminal connected to a power source (4),

a sixth switch (37) having a first terminal connected to said fourth transformer winding (35) and a second terminal connected to said power source (4).

14. The system according to claim 9, wherein said transformer has a third transformer winding (38), and wherein said supply pump reduction circuit (6) further comprises:

a third capacitor (39) connected between a first terminal of said third winding (38) and a power supply (4),

a fifth switch (41) connected between a second terminal of said third winding (38) and said power supply (4),

a fourth capacitor (40) connected between said first terminal of said third winding (38) and said power supply (4),

a sixth switch (42) connected between said second terminal of said third winding (38) and said power supply (4).

15. The system according to claim 9, wherein said transformer has a third transformer winding (43), and wherein said supply pump reduction circuit (6) further comprises:

a fifth switch (44) connected between a first terminal of said third winding (38) and a power supply (4),

a sixth switch (46) connected between a second terminal of said third winding (38) and said power supply (4),

a seventh switch (45) connected between said first terminal of said third winding (38) and said power supply (4),

an eighth switch (47) connected between said second terminal of said third winding (38) and said power supply (4).

16. The system according to any one of claims 2-15, wherein said transformer windings are magnetically coupled to each other in a transformer core (14) of a magnetic material