

The object of the present invention is an electric binary logic level detector. It is used in the field of information technology and, more specifically within this, in the field of smart cards equipped with microprocessors and memory circuits, made using MOS technology, of the non-volatile type (EPROM or EEPROM). The invention also relates to amplifiers for reading information contained in random access dynamic or static electronic memories.

The use of smart cards is increasing greatly. They are used most widely in the banking field where smart cards incorporating an integrated circuit are intended eventually to replace cheque books and to act as a universal means of transaction between the various people working in the financial field. Whatever the financial operations performed with such a card may be, the latter must contain two kinds of information. A first kind of information relates to bank balances. This information supplies the amount of the balance before and after each operation. This information about the balance should be available to the user. The information is confidential but nevertheless has to be ascertainable. On the contrary, other information should remain secret except to the owner of the card. This is the case for his secret code for validating an operation performed with the card. Other information should remain secret from the view of everyone, including the owner of the card. In general these are data items used for producing the secret code which is known only by the owner and which cannot therefore be reconstituted by electrical manipulations of the card. Unfortunately, the ingenuity of fraudsters is unlimited and it is necessary to guard against any attempts to decipher the secret information contained in the cards.

Thus it is realised that an intelligent fraudster could attempt to measure the electrical consumption of a polarisation circuit of the system for reading information contained in a card in order to determine, by measuring the variation in the electrical consumption, the sequence of the logic levels supplied by the card so as to deduce from this the secret codes written in it. In practice, the memory cells of integrated circuit smart cards are often of the type comprising a transistor

with two gates: a control gate and a floating gate. Charge stored in the floating gate can oppose the switching into a conductive state of the transistor in response to a command applied to the control gate and in this way show their presence, whereas their absence would make the transistor conductive and would cause in a measurement circuit connected in series with the said transistor a change in the signal introduced into it. The programming of such a memory, therefore, is performed by storing or not storing such charges in the floating gates of the said transistors. However, the electrical energy employed to change from one situation to the other is low. In order to be able to transmit the information correctly to a reading device or a device for performing a financial transaction it has to be amplified.

In practice these amplifiers are simply produced in CMOS technology by using two transistors having inverse conductivities, one of type P and one of type N, connected in series and polarised between the supply voltage V_{cc} of the circuit and ground. The gates of these transistors are connected together and receive the signal to be amplified. The output is taken from the midpoint of the said transistors. This amplifier assembly is an inverter. The disadvantage of using such an inverter as an amplifier is that there is a large difference in consumption depending on whether it has to transmit a logic state 1 or a logic state 0. The current which passes through the amplifier thus shows, by its value, the logic state read. In practice when it consumes a larger current the internal impedance of the polarisation generator gives rise to a drop in the supply voltage which can be made use of in this sense. Whatever the improvements made to these generators may be, the circuits for connecting the supply to the cards are contact circuits and consequently highly resistive, and they act as an internal resistance of this kind and cause the revealing drop in voltage.

A solution to the problem described in European patent application EP-A-279 712, cited in accordance with Art. 54(3) EPC, is specifically mentioned in the preambles of claims 1, 2, 3 and 4. The present invention proposes improvements to this.

In practice, in dynamic memory circuits the information relating to the logic level to be detected is transient. The determination of a given logic level can be more reliably obtained the more this fleeting information can be transformed into information which is maintained at least for some time. Moreover it is necessary that such a detector, outside the periods when it has to perform its detection function, should have as small a static consumption as possible. In practice it is necessary not to increase too much the temperature of the integrated circuit of which this detector may form part. Lastly, the detector thus produced should be a rapid detector: it should have an operating speed as fast as that of a logic gate.

The aim of the invention is to provide a solution to these problems by proposing a detector equipped substantially with two detection circuits which are connected in parallel between the electricity supply and ground and are complementary to one another. Depending on the logic level introduced, one of the two circuits switches over and causes an electrical consumption equal to the electrical consumption caused by the other circuit when the latter switches over at a different binary logic level. Preferably, in order to avoid untimely consumptions of electricity outside the detection periods these two circuits are activated and then deactivated at the time of reception of each logic level detected. The deactivating signal of the detector may also be used to reset the detector to zero and to make it ready for a further detection.

Consequently the invention relates to:

- an electric binary logic level detector comprising a first and a second circuit connected in parallel which receive the same signal to be detected, these two circuits having complementary electrical consumptions so that the detector always has the same total consumption whether it is detecting a binary logic level "0" or a binary logic level "1", characterized in that each circuit comprises an activating command for being activated when a level is to be detected and to be deactivated outside these periods, the deactivating command serving to reset the detector to zero.

- an electric binary logic level detector comprising a first and a second circuit connected in parallel which receive the same signal to be detected, these two circuits having complementary electrical consumptions so that the detector always has the same total consumption whether it is detecting a binary logic level "0" or a binary logic level "1", characterized in that it comprises a circuit for maintaining the logic level supplied in order to improve the detection of transient logic levels received.

- an electric binary logic level detector comprising a first and a second circuit connected in parallel which receive the same signal to be detected, these two circuits having complementary electrical consumptions so that the detector always has the same total consumption whether it is detecting a binary logic level "0" or a binary logic level "1", characterized in that the two circuits comprise means in order to be coupled and mutually to maintain themselves in their respective states.

- an electric binary logic level detector comprising a first and a second circuit connected in parallel which receive the same signal to be detected, these two circuits having complementary electrical consumptions so that the detector always has the same total consumption whether it is detecting a binary logic level "0" or a binary logic level "1", characterized in that between Vcc and a terminal supplying an inverse bias signal, each circuit comprises in series a first, P type transistor, a second, P type transistor and a third, N type transistor, the first transistors having their gates connected to a bias signal, the outputs of the first and of the second circuits being taken taken at the respective midpoints between the first and second transistors, the gates of the second and the third transistors of the first circuit being respectively connected to the signal to be detected and to Vcc, and the gates of the second and the third transistors of the second circuit being respectively connected to ground and to the signal to be detected.

The invention will be better understood on reading the following description with reference to the accompanying Figures. These are given solely by way of non-limiting example of the invention.

Figure 1 shows a diagrammatic representation of a detector in accordance with the invention.

Figure 2 shows timing diagrams of synchronization signals occurring in the device in accordance with the invention.

Figure 1 shows an electric binary logic level detector 50 in accordance with the invention. It comprises an input 1 for receiving a signal with a given logic level and, in the embodiment shown, two outputs 2 and 3 for supplying at least one signal with a logic level corresponding to the logic level received. In the present case the two signals supplied are also complementary to one another. As an essential characteristic feature, the detector in accordance with the invention comprises means for making its consumption independent of the logic levels supplied. In the particular embodiment shown, the means for making the consumption independent of the logic levels supplied substantially comprises two circuits 4 and 5, polarised to V_{cc} , in parallel with one another and both receiving through an input, 6 and 7 respectively, the signal to be detected.

A particular feature of the two circuits 4 and 5 is that they have complementary electrical consumptions with respect to the binary logic levels to be detected. In the particular, and preferred, embodiment example shown, the two circuits 4 and 5 are completely identical and this ensures that the electrical consumptions are complementary. They are differentiated only by the manner in which the components which they comprise are connected.

Thus the circuit 4 comprises three transistors connected in series, namely the transistors 8 to 10, whereas the circuit 5 comprises three other transistors connected in series, namely the transistors 11 to 13. The transistors 8, 9, 11 and 12 are P channel transistors (their gates are shown with a small circular symbol). They have the characteristic feature, when supplied with a positive supply voltage V_{cc} , of being conductive when they receive a zero electric level (ground) on

their gate and, on the other hand, of being blocked when they receive an electric level 1 (V_{cc}) there. The transistors 10 and 13 are N channel transistors. They operate in the inverse manner to the transistors just mentioned. In the circuits 4 and 5 the three transistors are connected in series between the supply voltage V_{cc} and a common terminal receiving a signal CHEPR complementary to a signal PRECH which is itself applied to the gates of the transistors 8 and 11. In a particular embodiment, the gate of the transistor 10 is connected to the supply voltage V_{cc} whereas the gate of the transistor 12 is connected to ground. The gates of the other transistors, 9 and 13, are connected together to the input 1 of the detector. The output 2 of the detector is taken from the midpoint of the transistors 8 and 9 whereas the output 3 is taken from the midpoint of the transistors 11 and 12.

The signal PRECH is a precharge signal. It is complementary to the signal CHEPR and it is usually zero whereas the latter has the value V_{cc} . At the time of detection, after a signal for precharging a bit line PRBL of a memory (for example comprised by a memory card) has been applied to the output of a decoder 14, in dependence on an address signal ADR, a bit line BLi of order number "i" is selected. The simultaneous selection of a word line then allows a specific word line WLj to send to the decoder 14 the data contained in a memory point "ij". This data is sent to the detector. The change in the supply current is produced in a plurality of word lines simultaneously so that its exploitation for fraudulent decoding purposes becomes impossible. Subsequently when the detector receives the command for validation of detection, it switches over in a manner which differs depending on the nature of the data available at its input 1.

Before the signal SD to be detected occurs, the precharge signal PRECH has the value zero and the signal CHEPR has the value V_{cc} (Figure 2). In this case the two signals S2 and S3 available at the outputs 2 and 3 have the value V_{cc} . In fact the transistors 8 and 11 conduct because, being P channel transistors, they receive a zero voltage on their gates. The voltage V_{cc} is therefore transmitted to the outputs 2 and 3. All the

transistors 8 to 12 are then conductive and only the transistor 13 is blocked. After the application of the signal PRBL, which biases the input of the detector and the bit lines to the value 1, reading of the cell takes place. The signal SD either remains at 1 or discharges to zero. Once the level has stabilised, the signal PRECH switches to Vcc and the signal CHEPR switches to zero. In a first case the signal SD available at the input 1 has the value zero. In this case the transistor 13 remains blocked whereas the transistor 9 becomes conductive. The transistor 8 becomes blocked and the transistor 10 becomes conductive. Under these conditions the output 2 changes to the zero state. In contrast, the blocking of the transistor 11, the switching on of the transistor 12 and the blocking of the transistor 13 maintains the output 3 at the level 1. On the contrary, if the input signal is at the level 1 and has the value Vcc, the transistors 12 and 13 become conductive and the output 3 switches to zero whereas the output 2 remains at Vcc.

Whatever the situation may be, the transistors 10 and 12 are permanently conductive. Their function is solely to make the two identical branches of the circuit symmetrical. In this manner identical discharge rates are obtained in the two branches. Because of this fact it is no longer possible to use the discharge rate, as reflected in the supply circuit, as information which can be used to disclose the logic levels transmitted. At the end of the transmission the signal PRECH falls back again to zero and the signal CHEPR changes in a complementary manner. The detector then returns to its initial state: the transistors 8, 9, 10, 11 and 12 are conductive, the transistor 13 is blocked and the two outputs 2 and 3 are at the level Vcc. In this condition the detector does not consume any current since the conductive transistors are connected on either side to equal potentials and because the other transistor is blocked.

When the detector detects, at the time of switch over, one of the two outputs 2 and 3 remains in the Vcc state whereas the other returns to zero. The one which remains in the Vcc state is in fact in an unstable state at this voltage. In fact this voltage is taken between two blocked

transistors in series: transistors 8 and 9 when a zero state is available at the input 1, transistors 11 and 12 when V_{cc} is available at the input 1. In order to maintain the outputs 2 and 3 at this significant level a bistable circuit is used in series with each of the two outputs, for example the circuit 15. The circuit 15 substantially comprises an inverter 16 in series with the output 2 and a P channel transistor 17 connected in parallel between the voltage supply V_{cc} and the input of the inverter 16. The output of the inverter 16 is fed back to the gate of the transistor 17. If a "1" level (V_{cc}) is available at the input of the inverter 16, a zero level is available at its output. Under these conditions the transistor 17 becomes conductive and transmits, maintaining the potential, the voltage V_{cc} to the input of the inverter 16. On the contrary, if the potential at the output 2 is zero the output of the inverter 16 is brought to V_{cc} , blocking the transistor 17 and efficiently maintaining the input of the inverter 16 at zero.

In a preferred alternative embodiment, the two circuits 4 and 5 are both coupled to one another through the intermediary of their respective bistable circuits 15 and 18. For this purpose the output of the circuit 15, that is to say the output of the inverter 16, is connected through a connection 19 to the gate of the transistor 12 and the connection to ground of the said gate of the transistor 12 is cut. For the same purpose the input of the bistable circuit 18, that is to say in short the output 3 of the detector, is connected through a connection 20 to the gate of the transistor 10 and the connection to the voltage supply V_{cc} of the gate of the transistor 10 is cut. These two latter connections are shown in dashed lines in Figure 1. This type of connection constitutes for the detector unit an assembly which has three stable states. Outside the detection periods the outputs 2 and 3 are at V_{cc} , the output of the bistable circuit 15 is therefore at zero and the new connections 19 and 20 maintain the gates of the transistors 12 and 10, respectively, in the same states as described until now. During a detection one of the two outputs is brought to V_{cc} whereas the other is brought to zero. When the output 2 is only brought to V_{cc} (a logic level 1 is available at its input 1) the transistor 12 receives a zero

potential: nothing is changed so far as it is concerned. On the other hand, the transistor 10 also receives a zero potential and as a result it also tends to become blocked. Consequently, if there is a parasitic change tending to cause the input 1 to change to the level zero (for example a decrease in the voltage supplied by the memory) the transistor 9 will be able to become conductive without changing the level of the voltage available at the output 2 because the blocking of the transistor 10 ensures that the value of this voltage at the output 2 is V_{cc} .

In the other case, when a logic level zero is detected at the input of the detector, the output 3 is brought to a voltage V_{cc} whereas the output 2 is brought to zero. Consequently the transistor 10 receives a voltage V_{cc} on its gate. Nothing is changed so far as it is concerned relative to its previously described connection layout. On the contrary, the transistor 12 now receives on its gate a signal biased to V_{cc} . Because the transistor 12 is a P channel transistor it becomes blocked. Consequently the output 3 taken between two blocked transistors, the transistors 11 and 12, remains at its existing potential, namely the potential V_{cc} . It remains at this value even if there is a parasitic change. When the precharge signals PRECH and CHEPR return to their resting values, the outputs of the circuits 15 and 18 both fall back to zero.

The connection arrangement obtained in this manner therefore has the advantage of comprising three stable states - a stable resting state, and two stable states which depend on the logic level detected. In the two stable states which depend on the logic level detected, the circuit is able to take into account transient effects and to maintain the state of the information no matter what the random changes to which the information is subsequently subjected may be. In particular this method of operation is of particular interest when, before reading other memory cells, the precaution is taken of discharging the word lines WL_j with a voltage V_{ss} (negative) after a preceding reading operation. This precaution, which improves the reliability of reading the data contained in a memory cell, until now made it difficult to take the information read into account. Moreover the bistable circuits 15 and 18 being

complementary, the consumption is the same whatever the logic level detected.

In the logic circuits located downstream it is possible to use one of the signals supplied by the bistable circuits or even both of them. In these logic circuits located downstream the treatment received by the signals makes it impossible to decode them fraudulently. Preferably the detector in accordance with the invention is incorporated in the integrated circuit comprised by a smart card. It is not very bulky and its production does not involve any special steps in the manufacture of the integrated circuit. Only one detector is used per card.

CLAIMS

1. An electric binary logic level detector (50) comprising a first and a second circuit (4 and 5) connected in parallel which receive the same signal to be detected (1), these two circuits (4 and 5) having complementary electrical consumptions so that the detector (50) always has the same total consumption whether it is detecting a binary logic level "0" or a binary logic level "1", characterized in that each circuit comprises an activating command (PRECH and CHEPR) for being activated when a level is to be detected and to be deactivated outside these periods, the deactivating command serving to reset the detector to zero.
2. An electric binary logic level detector (50) comprising a first and a second circuit (4 and 5) connected in parallel which receive the same signal to be detected (1), these two circuits (4 and 5) having complementary electrical consumptions so that the detector (50) always has the same total consumption whether it is detecting a binary logic level "0" or a binary logic level "1", characterized in that it comprises a hold circuit (15 and 18) for maintaining the logic level supplied in order to improve the detection of transient logic levels received.
3. An electric binary logic level detector (50) comprising a first and a second circuit (4 and 5) connected in parallel which receive the same signal to be detected (1), these two circuits (4 and 5) having complementary electrical consumptions so that the detector (50) always has the same total consumption whether it is detecting a binary logic level "0" or a binary logic level "1", characterized in that the two circuits comprise means (19 and 20) in order to be coupled and to mutually maintain themselves in their respective states.
4. An electric binary logic level detector (50) comprising a first and a second circuit (4 and 5) connected in parallel which receive the same signal to be detected (1), these two circuits (4 and 5) having complementary electrical consumptions so that the detector (50) always



has the same total consumption whether it is detecting a binary logic level "0" or a binary logic level "1", characterized in that, between Vcc and a terminal supplying an inverse bias signal (CHEPR), each circuit comprises in series a first, P type transistor, a second, P type transistor and a third, N type transistor, the first transistors having their gates connected to a bias signal (PRECH), the outputs (2 and 3) of the first and of the second circuits (4 and 5) being taken at the respective midpoints between the first and second transistors, the gates of the second and the third transistors of the first circuit being respectively connected to the signal to be detected (1) and to Vcc, and the gates of the second and the third transistors of the second circuit (5) being respectively connected to ground and to the signal to be detected (1).

5. Use of a detector as claimed in any one of claims 1 to 4 as a read amplifier in a system for reading information contained in a memory circuit of a smart card of the type comprising an integrated circuit memory.

6. Use as claimed in claim 5, characterized in that the detector constitutes an integral part of the integrated circuits in the smart card.

