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BRANCH TRANSMISSION LINE, DRIVER CIRCUIT, AND
SEMICONDUCTOR TEST SYSTEM USING SAME

Field of the Invention

This invention relates to a signal transmission line having two branch lines to be used in a semiconductor test system, and more particularly, a transmission line connected to at least two branch lines and having means for minimizing unwanted ringing or vibration on a signal transmitted to receiving points, and a signal driver circuit for driving such a transmission line, and a semiconductor test system using such transmission lines and driver circuits.

Background of the Invention

Figure 6 is a schematic block diagram showing an example of semiconductor test system in the conventional technology for testing a semiconductor integrated circuit (hereafter may also be referred to as "device under test" or "DUT"). In this example, the semiconductor test system includes a test handler 24 for handling semiconductor devices 19 to be tested so that the semiconductor devices 19 are positioned on appropriate test positions to receive test signals. The example of Figure 6 shows only one test pin (test channel) of the test system, although a large number of test pins are provided in an actual semiconductor test system.

In the example of Figure 6, a test processor 11 is a dedicated processor provided within the semiconductor test system for controlling the operation of the test system through a tester bus. Based on pattern data from the test processor 11, a pattern generator 12 provides timing data and waveform data to a timing generator 13 and a wave formatter 14, respectively. A test pattern (test signal) is produced by the wave formatter 14 with use of the waveform data from the pattern generator 12 and the timing data from the timing generator 13. The test pattern is supplied to the devices under test (DUT) 19 in the test handler 24 through a driver

15 and a test fixture and performance board 22.

A response output from the DUT 19 resulted from the test pattern is converted to a logic signal by an analog comparator 16 with reference to predetermined threshold voltages. The logic signal is compared with expected value data from the pattern generator 12 by a logic comparator 17. The result of the logic comparison is stored in a Failure memory 18 corresponding to the address of the DUT 19. The driver 15, the analog comparator 16 and switches (not shown) for changing pins of the device under test, are provided in a pin electronics 20.

To increase the test efficiency, one of approaches is to test two devices 19 by using one test pin. As shown in Figure 6, the test handler 24 provides the two devices to be tested to the test positions to receive the same test signal from the driver 15 via branch lines. The present invention is directed to a signal transmission line having such branch lines to transmit the test signal to two receiving points without decreasing the signal quality.

The conventional technology regarding such a transmission line is explained with reference to the schematic diagram of Figure 4 which shows two branch lines used in a driver circuit of semiconductor test system. As shown in Figure 4, the signal transmission line from the driver is branched into two lines. There are basically two termination modes in such a transmission line, one is a parallel termination mode using a parallel termination resistor, and the other is a series termination mode using a series termination resistor. The example of Figure 4 is directed to the series termination mode where a series resistor is incorporated at a transmission side.

The major components in the configuration of Figure 4 includes a pulse signal source 100, a driver DR1, a series resistor TR2, a first transmission line CB1, a second transmission line CB2, a third transmission line CB3, and two

devices under test (DUT). The pulse signal source 100 in Figure 4 corresponds to the pattern generator and wave formatter in the semiconductor test system of Figure 6, and the driver DR1 in Figure 4 corresponds to the driver 15 in the pin electronics in the test system of Figure 6.

The driver DR1 converts an incoming logic signal to a driver signal (test signal) having specified high voltage V_{IH} and low voltage V_{IL} and sends the drive signal (test signal) to the series resistor TR2. Within the context of this disclosure, the output terminal of the driver is hereafter referred to as a driver terminal. The rising edges (leading edges) and falling edges (trailing edges) of the drive signal are calibrated in advance to have accurate predetermined timings.

In testing semiconductor devices, it is desired that the waveforms at first and second receiving points (receiver terminals) are accurate duplicates of the drive signal at the driver terminal, and that rising and falling edges at the receiver terminals are within an acceptable range of the timing. If the waveforms of the drive signal are distorted or the edge timings are outside of the acceptable range, accurate test results are unavailable.

The series termination resistor TR2 is a resistor connected in series with the third transmission line to terminate reflected signals from the far end of the third transmission line. The series termination resistor TR2 has a resistance value of 50 ohms is used when the third transmission line CB3 has a characteristic impedance of 50 ohms. In practice, since the driver DR1 has certain output resistance, such as several ohms, the resistance value of the resistor TR2 is several ohms smaller than 50 ohms.

The third transmission line CB3 is a coaxial cable of several ten centimeters and has the characteristic impedance of, for example, 50 ohms. In a semiconductor test system, the third transmission line CB3 runs through a test fixture

and a performance board which interface the test system and the devices under test. The test fixture is a contact block having a large number of flexible contact pins such as pogo-pins to electrically connect the drivers in the pin electronics (Figure 6) to the performance board. The performance board has a circuit arrangement which is unique to the type of device under test.

The first transmission line CB1 and the second transmission line CB2 have an identical length and a characteristic impedance that is two times the characteristic impedance of the third transmission line CB3. Thus, in the above example, the characteristic impedance of the first and second transmission lines is 100 ohms. The first and second transmission lines are coaxial cables or microstrip lines with a length of, for example about 10cm (centimeters). Each end of the first and second transmission lines is connected to the third transmission line CB3 at a connection point CP. A suitable connection is made so that the characteristic impedance at this connection point CP is not affected.

Two devices to be tested by the same test signal are identical to one another, and are mounted on IC sockets (not shown) in the test handler during the test. Although the distance between the two devices varies depending on the structure of the test system, a typical example is about 10cm. Within the context of this disclosure, a pin terminal connected to the first device under test is referred to as a first receiver terminal RT1, and a pin terminal connected to the second device under test is referred to as a second receiver terminal RT2. At both receiver terminals (connected to devices under test), stray capacitance Cs1 and Cs2 of several pico-farad exist including input capacitance of the devices under test and IC sockets.

Waveform distortion involved in the conventional technology is explained with reference to Figure 3. In the arrangement of Figure 4, a forward path from the connection

point CP to the first receiver terminal RT1 is denoted by PASS1f, and a return path from the first receiver terminal RT1 to the connection point CP is denoted by PASS1r, a forward path from the connection point CP to the second receiver terminal RT2 is denoted by PASS2f, and a return path from the second receiver terminal RT2 to the connection point CP is denoted by PASS2r.

In Figure 3, waveforms A and B show distortions in the signals at the receiver terminals RT1 and RT2. The waveform C in Figure 3 shows the signals at both of the receiver terminals RT1 and RT2 when the transmission delays Td1 and Td2 from the connection point CP to the receiver terminals RT1 and RT2 are the same. In this case, since the receiver waveforms are the same at the two receiver terminals RT1 and RT2, there is no problem in the device testing. The waveforms are reflected from the receiver terminals RT1 and RT2 and returned to the connection point CP with the same phase and voltage. Thus, the reflected signals are terminated by the series termination resistor TR2 after transmitting through the third transmission line CB3.

The waveforms A and B in Figure 3 show the case where a transmission delay Td1 in the first transmission line CB1 and a transmission delay Td2 in the second transmission line CB2 are slightly different. The waveform A shows a signal at one receiver terminal and the waveform B shows a signal at the other receiver terminal in such a situation. The difference between the transmission delays can be caused by various factors even when the length of the two transmission lines is the same. Such factors include differences in soldering tips of the transmission lines, differences in stray capacitance at IC socket terminals, differences in input capacitance of the devices under test, and etc.

Reference is also made here regarding the ringing in the waveforms of Figure 3. At the connection point CP, the drive signal from the driver splits into two and propagates forward

to the two receiver terminals RT1 and RT2 and returns therefrom. In this case, the waveforms returned to the connection point CP have different phases (timings) from one another. Hence, a part of the returned signals are terminated by the series termination resistor TR2 after passing through the third transmission line CB3, while the remaining signals travel through the other transmission line (first transmission line CB1 and second transmission line CB2). By repeating this process, the ringing waveforms shown in Figure 3 are generated. The ringing (vibration) amplitude D corresponds to the phase difference and a slew rate of the drive signal. The ringing period E (oscillation frequency) corresponds to the time difference in the signal transmission time in the forward path PASS1f and the return path PASS1r and the signal transmission time in the forward path PASS2f and the return path PASS2r.

In order to test recent high speed devices operating at frequencies higher than several hundred HMz, a drive signal (test signal) with higher frequency and smaller slew rate (for example, 0.2ns/V) must be applied to the device under test. Hence, a small phase difference in the transmission lines results in a large vibration (ringing) amplitude.

Further, in such high speed device testing, since an interval between the signal edges becomes small, the next edge arrives before the ringing is attenuated. Thus, even though predetermined timings are set, the waveform changes by the effect of ringing waveform of rising and/or falling edge of the prior pulse as denoted by F in Figure 3. As a result, the timing of rising and falling edges of succeeding pulse will change as denoted by H and J in Figure 3. This change is not acceptable for a semiconductor test system requiring test results with high timing accuracy. The ringing or vibration described in the foregoing poses difficulty in applying accurate predetermined test signal waveforms to the devices under test, resulting in difficulty in achieving the

accurate device testing.

As described in the foregoing, in the conventional technology where a high speed test signal is transmitted through a transmission line and is branched into two transmission lines to be supplied to receiver terminals, unwanted ringing or vibration tend to be produced on the test signals.

Summary of the Invention

Therefore, it is an object of the present invention to provide a branch transmission line for transmitting a test signal to two devices under test which is capable of minimizing unwanted ringing or vibration in the test signal at receiving terminals of the devices under test.

It is another object of the present invention to provide a driver circuit using the branch transmission line of the present invention to transmit the test signal having a predetermined amplitude and slew rate to the two devices under test for testing the two devices by the same test signal at the same time.

It is a further object of the present invention to provide a semiconductor test system using the branch transmission line of the present invention to transmit the test signal having a predetermined amplitude and slew rate to the two devices under test for testing the two devices by the same test signal at the same time.

It is a further object of the present invention to provide various types of configuration of a waveform improvement means to be incorporated in the branch transmission line.

In the present invention, a waveform improvement means is provided between a first receiver terminal and a second receiver terminal, thereby creating a closed loop. A signal from the signal source is split into two signals at a connection point, one signal travels through the closed loop in a clockwise direction while the other signal travels

through the closed loop in a counterclockwise direction. Thus, the two signals return to the connection point with the same timing (phase) even when there is a difference in the signal propagation delay times between the first and second transmission lines.

The branch transmission line of the present invention is formed of a first transmission line where one end of which is connected to a first receiver terminal and the other end of which is connected to a connection point, a second transmission line where one end of which is connected to a second receiver terminal and the other end of which is connected to the connection point, a third transmission line where one end of which is connected to a signal source through a series termination resistor and the other end of which is connected to the connection point, a waveform improvement means connected to the first and second receiver terminals for forming a closed loop including the first and second transmission lines and the waveform improvement means, wherein characteristic impedance of the first and second transmission lines is twice as much as that of the third transmission line.

The waveform improvement means is a transmission line having characteristic impedance identical to that of the first and second transmission lines and is formed of either a coaxial cable or a microstrip line. In another aspect, the waveform improvement means is a transmission line having a series connected resistor whose impedance is smaller than the characteristic impedance of the first and second transmission lines by several times. In a further aspect, the waveform improvement means is a transmission line having a series connected capacitor whose impedance is smaller than the characteristic impedance of the first and second transmission lines by several times.

In the present invention, the signal from the signal source propagating through the third transmission line splits

into two signals, one travels through the closed loop in a clockwise direction while the other travels through the closed loop in a counterclockwise direction, and both signals return to the connection point with the same timing. Since there is no phase difference between the two returned signals, ringing or vibration is not induced at the first and second receiver terminals. This is true even when there is a difference in the signal propagation delay times between the first transmission line and the second transmission line. The returned signals are terminated by the series termination resistor. As a consequence, unwanted waveform distortion will not be produced. Thus, the branch transmission line of the present invention is able to achieve ideal waveforms at the receiver terminals for testing the two semiconductor devices at the same time by the same test signal.

Brief Description of the Drawings

Figure 1 is a schematic diagram showing a basic concept of the branch transmission line of the present invention.

Figure 2 is a schematic diagram showing a basic concept of a driver circuit using the branch transmission line of the present invention.

Figure 3 is a diagram for explaining waveform distortions at receiver terminals in the driver circuit using the branch transmission line.

Figure 4 is a schematic diagram showing a basic structure in the conventional driver circuit using a branch transmission line in a semiconductor test system.

Figure 5 is a diagram showing an example of waveform improvement means in the present invention.

Figure 6 is a block diagram showing an example of structure in the semiconductor test system having a branch transmission line for testing two devices at the same time by the same test signal.

Detailed Description of the Preferred Embodiments

The present invention is explained with reference to the

drawings. Figure 1 shows a basic concept of a branch transmission line of the present invention, Figure 2 shows a basic concept of a driver circuit using the branch transmission line of the present invention, and Figure 5 shows an example of various means for minimizing waveform distortions in the present invention. Figure 3 is to explain the waveform improvement in the driver circuit of the present invention. In the drawings above, identical labels and reference numerals are used for the components corresponding to those in the conventional technology of Figure 4.

The branch transmission line of Figure 1 includes a pulse signal source 100, a series termination resistor TR2, a first transmission line CB1, a second transmission line CB2, a third transmission line CB3, and a waveform improvement means 10. The pulse signal source 100 in Figure 4 corresponds to the pattern generator and wave formatter in the semiconductor test system of Figure 6. A pulse signal (test signal) is transmitted to the first and second receiver terminals RT1 and RT2. The present invention is intended to transmit the pulse signal to the two receiver terminals RT1 and RT2 with the waveforms identical to the original waveform from the pulse signal source 100. The example of Figure 1 includes the waveform improvement means 10. The other components are identical to those in the conventional configuration of Figure 4.

With respect to the first and second receiver terminals RT1 and RT2, it is assumed that distributed capacitance (stray capacitance) Cs1 and Cs2 exist at the inputs of the test system (handler) and devices under test. Load resistors may be included at the receiver terminals, the resistance of which is large enough, for example 10K ohms, relative to the characteristic impedance of 100-ohm of the first and second transmission lines CB1 and CB2.

The waveform improvement means 10 is connected between the first and second receiver terminals RT1 and RT2. Thus,

the both ends of the first transmission line CB1 and second transmission line CB2 are connected to one another through the waveform improvement means 10.

An example of the waveform improvement means 10 is a transmission line having characteristics impedance that is identical to that of the first and second transmission lines CB1 and CB2. Namely, as shown in Figure 1, a fourth transmission line CB4 having characteristic impedance 100 ohms is incorporated between the first and second receiver terminals RT1 and RT2. There is no requirements regarding a signal propagation delay time for the fourth transmission line CB4. It is only necessary that the fourth transmission line CB4 is able to connect two receiver terminals RT1 and RT1. A coaxial cable, a microstrip line or other high frequency transmission line may be used for the fourth transmission line CB4.

The waveform improvement by the configuration of the present invention described in the foregoing is explained with reference to Figures 1 and 3. It is assumed that there exists a difference in the transmission delay times between the first transmission line CB1 and second transmission line CB2. As shown in Figure 1, a clockwise route LP1 is a closed loop for a signal traveling from the connection point CP, first transmission line CB1, fourth transmission line CB4, second transmission line CB2, and to the connection point CP. A counterclockwise route LP2 is a closed loop for a signal traveling from the connection point CP, second transmission line CB2, fourth transmission line CB4, first transmission line CB1, and to the connection point CP.

By adding the fourth transmission line CB4, signals will not directly return to the connection point CP from the receiver terminals, but will return to the connection point CP by travelling through the closed loops, i.e., the clockwise route LP1 or the counterclockwise route LP2. It should be noted that the signals in either routes LP1 or LP2

pass through the identical transmission lines in the end. Hence, the signals traveling through the routes LP1 and LP2 experience the same propagation delay time.

Thus, in the present invention, even when there is a difference in the transmission delay times between the first transmission line CB1 and second transmission line CB2, drive signals (test signals) separated at the connection point CP will return to the connection point CP at the same timing (phase). As a consequence, unwanted vibration or ringing such as shown in Figure 3 will not be produced. Thus, the branch transmission line of the present invention is able to achieve an ideal waveform C in Figure 3 at both receiver terminals RT1 and RT2.

Preferably, the connection points of the fourth transmission line CB4 are at the very points of the first receiver terminal and second receiver terminal. However, the positions of the connection points can be slightly apart, such as several millimeters, from the ideal receiver terminals since the ringing or vibration in such a situation will be significantly small.

An example of other possible configurations in the waveform improvement means 10 is shown in Figure 5. Figure 5(a) is a schematic diagram showing a basic structure in the closed loop formed by incorporating the waveform improvement means 10. Figures 5(b), 5(b) and 5(c) respectively show equivalent circuits of various modifications of the waveform improvement means 10.

Figure 5(b) shows an example when the waveform improvement means 10 is a single transmission line. As noted above, the transmission line can be configured by a coaxial cable, microstrip line or other high frequency cables. As described above, one drive signal propagates in the clockwise direction of the closed loop of Figure 5(a) while the drive signal propagates in the counterclockwise direction of the closed loop, thereby returning to the connection point CP at

the same timing.

An example of Figure 5(c) includes capacitor C1 between two transmission lines CB5. The capacitor C1 is effective to allow only high frequency components to pass therethrough and cut DC or low frequency components in the drive signals. Because only high frequency components affect the quality of the waveforms of the drive signals, it is unnecessary for the DC or low frequency components to pass through the waveform improvement means. The value of the capacitor C1 is determined by the slew rates and frequency of the drive signals, which is in the order of 1,000 pico-farad.

In the configuration of Figure 5(d), a resistor R1 is provided between the two transmission lines CB5. An example of resistance value is less than 10 ohms (less than 1/5 of the characteristic impedance) when the characteristic impedance of the transmission lines CB5 is 100 ohms. The resistor R1 is effective in slightly attenuating the signal propagating through the waveform improvement means, thereby improving the stability of operation. Although not shown, a further example of configuration in the waveform improvement means 10 is a combination of the capacitor C1 and resistor R1 series connected with one another between the transmission cables CB5.

In the example of Figure 5(b), 5(c) and 5(d), when the receiver terminals RT1 and RT2 are located close to each other such as several centimeters and a relatively low level of waveform quality is sufficient, a simple wire may be used as the waveform improvement means.

The branch transmission line of Figure 1 is advantageously applied to the driver circuit of Figure 2 in the semiconductor test system. Also referring to Figure 6, the branch transmission line is provided between the driver 15 in the pin electronics 20 and the devices under test in the test handler or wafer prober through the performance board and the test fixture 22. In the configuration of

Figure 2, the drive signal (test signal) at the output of the driver DR1 is transmitted and applied to the two devices under test with substantially the same waveform.

In the present invention, the signal from the signal source propagating through the third transmission line splits into two signals, one travels through the closed loop in a clockwise direction while the other travels through the closed loop in a counterclockwise direction, and both signals return to the connection point with the same timing. Since there is no phase difference between the two returned signals, ringing or vibration is not induced at the first and second receiver terminals. This is true even when there is a difference in the signal propagation delay times between the first transmission line and the second transmission line. The returned signals are terminated by the series termination resistor. As a consequence, unwanted waveform distortion will not be produced. Thus, the branch transmission line of the present invention is able to achieve an ideal waveform at the receiver terminals for testing the two semiconductor devices at the same time by the same test signal.

Although only a preferred embodiment is specifically illustrated and described herein, it will be appreciated that many modifications and variations of the present invention are possible in light of the above teachings and within the purview of the appended claims without departing the spirit and intended scope of the invention.

WHAT IS CLAIMED IS:

1. A branch transmission line for transmitting a signal to two receiver terminals, comprising:

a first transmission line, one end of which is connected to a first receiver terminal and the other end of which is connected to a connection point;

a second transmission line, one end of which is connected to a second receiver terminal and the other end of which is connected to the connection point;

a third transmission line, one end of which is connected to a signal source through a series termination resistor and the other end of which is connected to the connection point;

a waveform improvement means connected to the first and second receiver terminals for forming a closed loop including the first and second transmission lines and the waveform improvement means;

wherein characteristic impedance of the first and second transmission lines is twice as much as that of the third transmission line.

2. A branch transmission line as defined in Claim 1, wherein a signal from the signal source propagating through the third transmission line is split into a first signal and a second signal at the connection point, wherein the first signal travels through the closed loop in a clockwise direction thereof while the second signal travels through the closed loop in a counterclockwise direction thereof, and wherein the first and second signals return to the connection point with the same timing.

3. A branch transmission line as defined in Claim 1, wherein the waveform improvement means is a transmission line having characteristic impedance identical to that of the first and second transmission lines and is formed of either a coaxial cable or a microstrip line.

4. A branch transmission line as defined in Claim 1,



wherein the waveform improvement means is a transmission line having a series connected resistor whose impedance is smaller than the characteristic impedance of the first and second transmission lines by several times.

5. A branch transmission line as defined in Claim 1, wherein the waveform improvement means is a transmission line having a series connected capacitor whose impedance is smaller than the characteristic impedance of the first and second transmission lines by several times.

6. A branch transmission line as defined in Claim 1, wherein the waveform improvement means is a transmission line having characteristic impedance identical to that of the first and second transmission lines and having a series connected resistor whose impedance is smaller than the characteristic impedance of the first and second transmission lines by several times.

7. A branch transmission line as defined in Claim 1, wherein the waveform improvement means is a transmission line having characteristic impedance identical to that of the first and second transmission lines and having a series connected capacitor whose impedance is smaller than the characteristic impedance of the first and second transmission lines by several times.

8. A driver circuit having a branch transmission line for transmitting a signal to two receiver terminals, comprising:

- a driver for generating a drive signal having a predetermined amplitude and slew rate;

- a first transmission line, one end of which is connected to a first receiver terminal and the other end of which is connected to a connection point;

- a second transmission line, one end of which is connected to a second receiver terminal and the other end of which is connected to the connection point;

- a third transmission line, one end of which is



connected to an output of the driver through a series termination resistor and the other end of which is connected to the connection point;

a waveform improvement means connected to the first and second receiver terminals for forming a closed loop including the first and second transmission lines and the waveform improvement means;

wherein characteristic impedance of the first and second transmission lines is twice as much as that of the third transmission line.

9. A driver circuit as defined in Claim 8, wherein the drive signal from the driver propagating through the third transmission line is split into a first drive signal and a second drive signal at the connection point, wherein the first drive signal travels through the closed loop in a clockwise direction thereof while the second drive signal travels through the closed loop in a counterclockwise direction thereof, and wherein the first and second drive signals return to the connection point with the same timing.

10. A driver circuit as defined in Claim 8, wherein the waveform improvement means is a transmission line having characteristic impedance identical to that of the first and second transmission lines and is formed of either a coaxial cable or a microstrip line.

11. A driver circuit as defined in Claim 8, wherein the waveform improvement means is a transmission line having a series connected resistor whose impedance is smaller than the characteristic impedance of the first and second transmission lines by several times.

12. A driver circuit as defined in Claim 8, wherein the waveform improvement means is a transmission line having a series connected capacitor whose impedance is smaller than the characteristic impedance of the first and second transmission lines by several times.

13. A driver circuit as defined in Claim 8, wherein the



waveform improvement means is a transmission line having characteristic impedance identical to that of the first and second transmission lines and having a series connected resistor whose impedance is smaller than the characteristic impedance of the first and second transmission lines by several times.

14. A driver circuit as defined in Claim 8, wherein the waveform improvement means is a transmission line having characteristic impedance identical to that of the first and second transmission lines and having a series connected capacitor whose impedance is smaller than the characteristic impedance of the first and second transmission lines by several times.

15. A semiconductor test system for testing semiconductor devices, comprising:

- a test signal generator for generating a test signal to be provided to semiconductor devices under test;

- a comparator for comparing output signals from the semiconductor devices under test resultant from the test signal with an expected signal;

- a driver circuit having a branch transmission line for transmitting a signal to first and second receiver terminals, wherein the driver circuit comprising:

- a driver for generating a drive signal having a predetermined amplitude and slew rate;

- a first transmission line, one end of which is connected to the first receiver terminal and the other end of which is connected to a connection point;

- a second transmission line, one end of which is connected to the second receiver terminal and the other end of which is connected to the connection point;

- a third transmission line, one end of which is connected to an output of the driver through a series termination resistor and the other end of which is connected to the connection point;



a waveform improvement means connected to the first and second receiver terminals for forming a closed loop including the first and second transmission lines and the waveform improvement means;

wherein characteristic impedance of the first and second transmission lines is twice as much as that of the third transmission line.

16. A semiconductor test system as defined in Claim 15, wherein the waveform improvement means is a transmission line having characteristic impedance identical to that of the first and second transmission lines and is formed of either a coaxial cable or a microstrip line.

17. A semiconductor test system as defined in Claim 15, wherein the waveform improvement means is a transmission line having a series connected resistor whose impedance is smaller than the characteristic impedance of the first and second transmission lines by several times.

18. A semiconductor test system as defined in Claim 15, wherein the waveform improvement means is a transmission line having a series connected capacitor whose impedance is smaller than the characteristic impedance of the first and second transmission lines by several times.

19. A semiconductor test system as defined in Claim 15, wherein the first receiver terminal is a first contact point between the semiconductor test system and a first semiconductor device under test, and the second receiver terminal is a second contact point between the semiconductor test system and a second semiconductor device under, and wherein the waveform improvement means is connected between the first and second contact points.