

DRAM MEMORY CELL HAVING A VERTICAL BIPOLAR INJECTOR

ABSTRACT

According to a first aspect, the invention relates to a memory cell comprising:

- an FET transistor having a source (S), a drain (D) and a floating body (FB) between the source and the drain,
- an injector that can be controlled to inject a charge into the floating body of the FET transistor, the injector consisting of a bipolar transistor having an emitter, a base and a collector formed by the body of the FET transistor,

the cell being characterized in that the emitter of the bipolar transistor is arranged so that the source of the FET transistor serves as the base for the bipolar transistor.

The invention also extends to a memory array comprising a plurality of memory cells according to the first aspect of the invention, and to a method of controlling such a memory cell.

FIGURE 2a