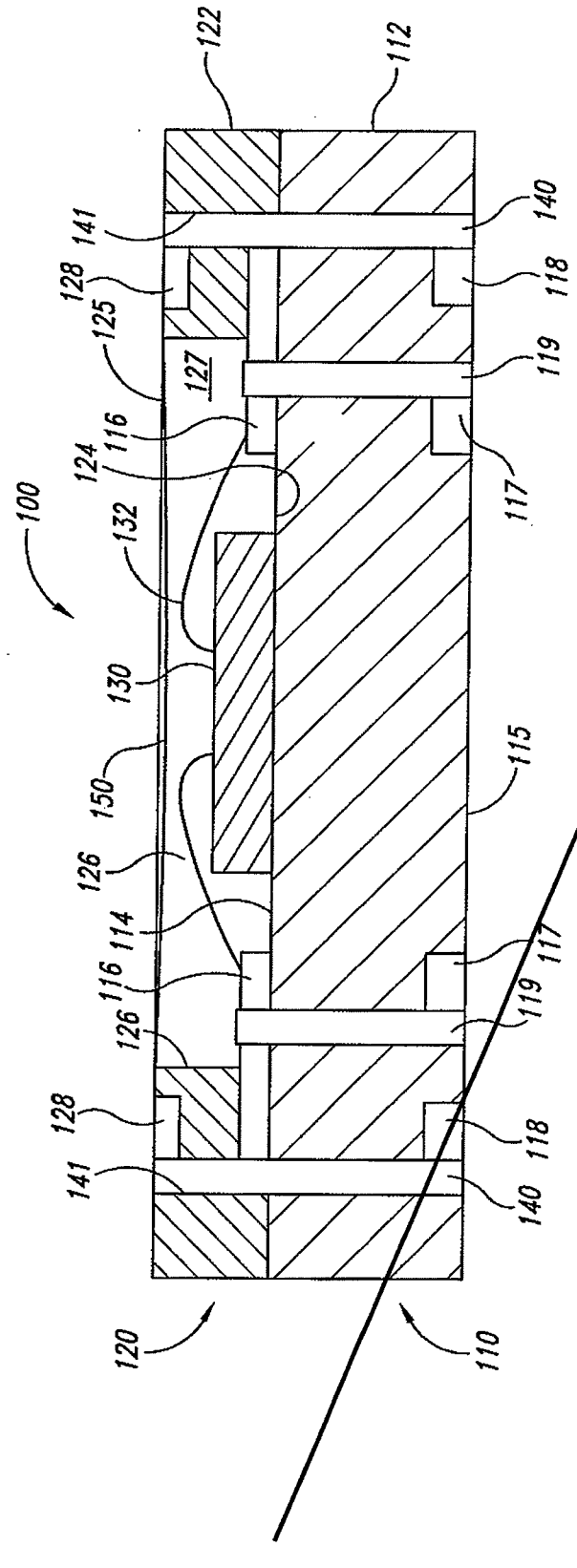

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Fig. 1

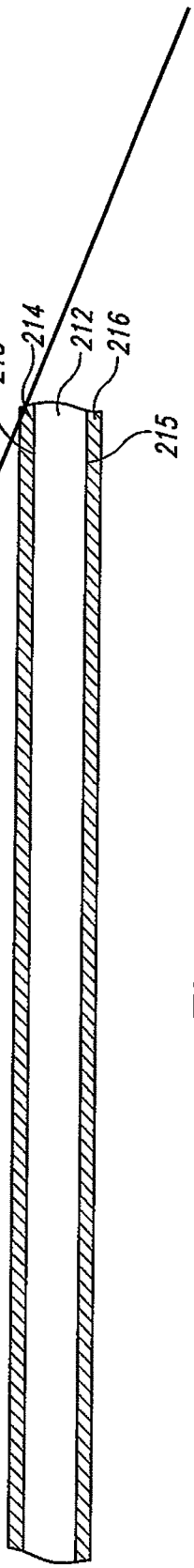

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Fig. 2A

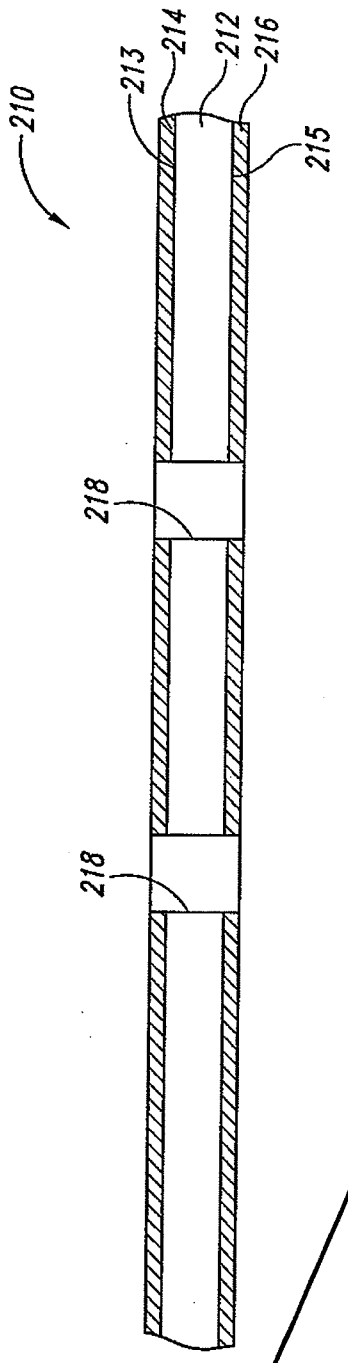

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Fig. 2B

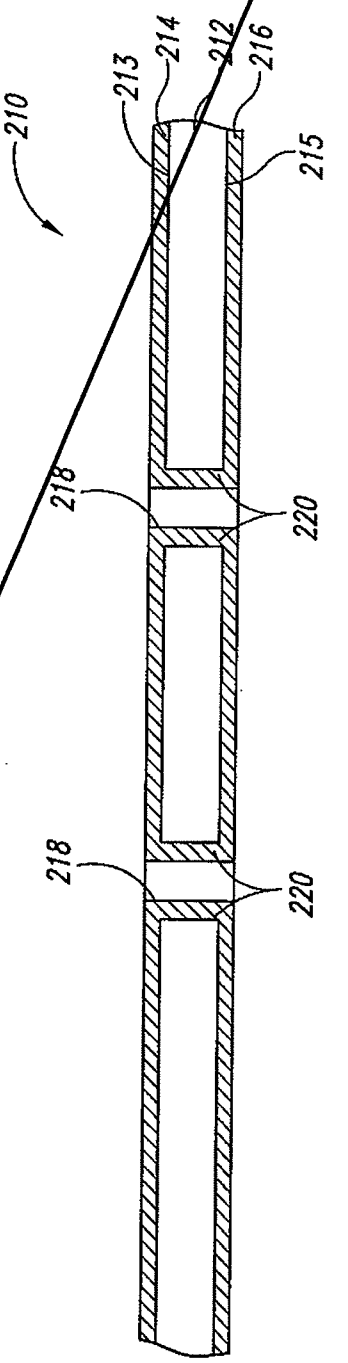

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Fig. 2C

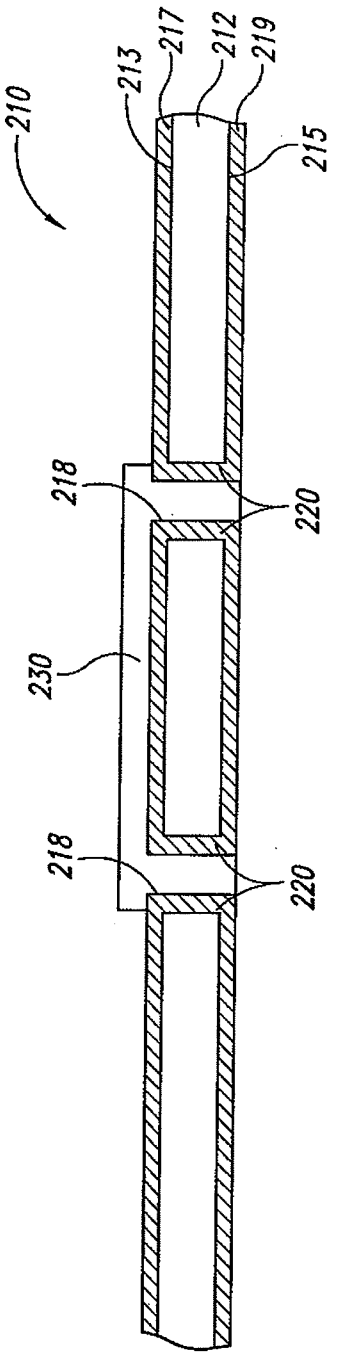

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Fig. 2D

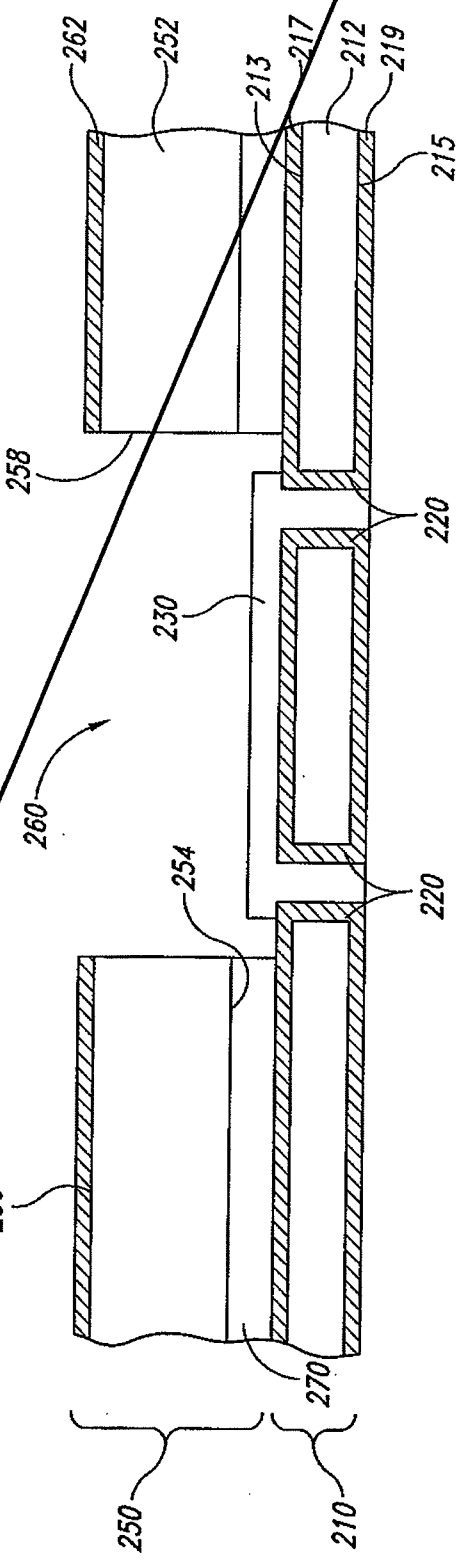

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Fig. 2E

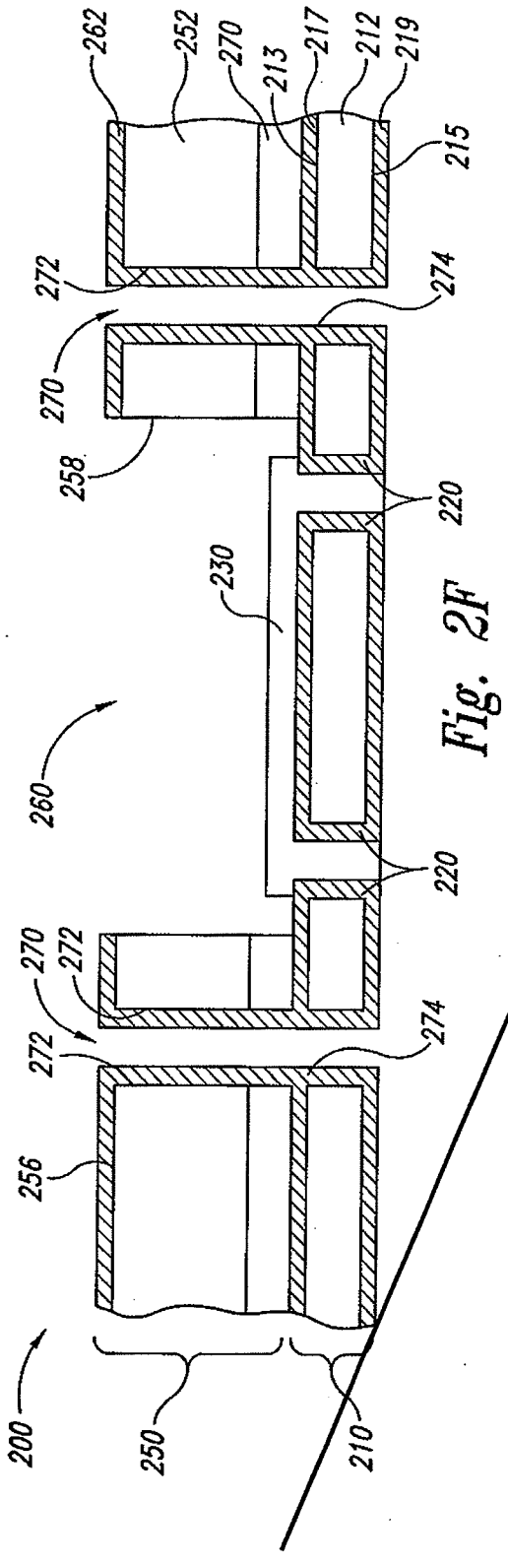

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Fig. 2F

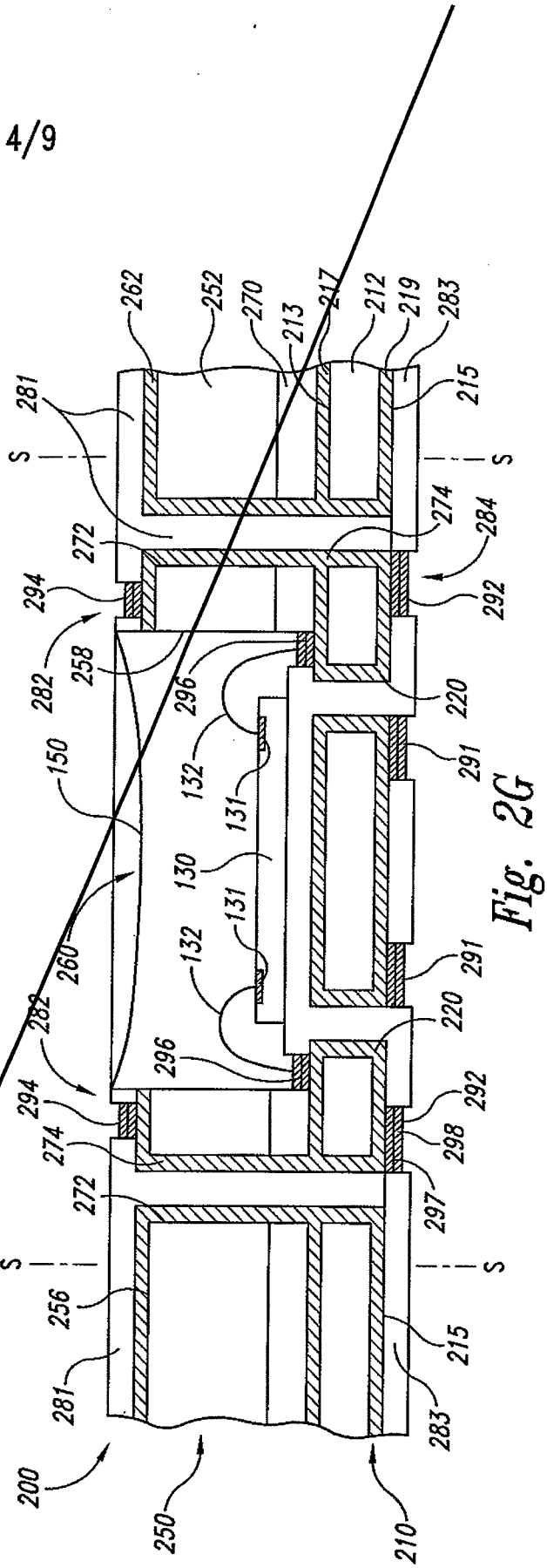

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Fig. 2G

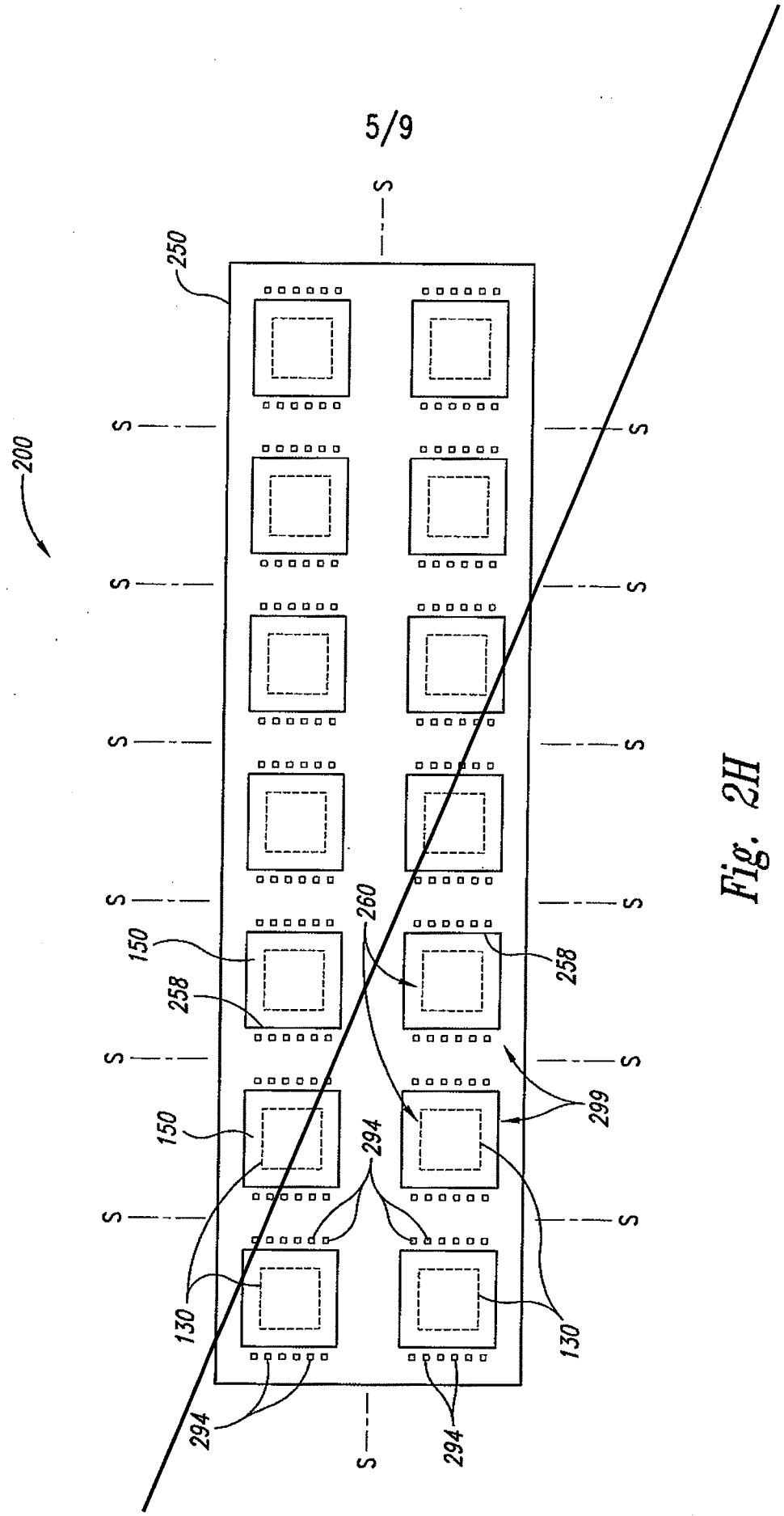


Fig. 2H

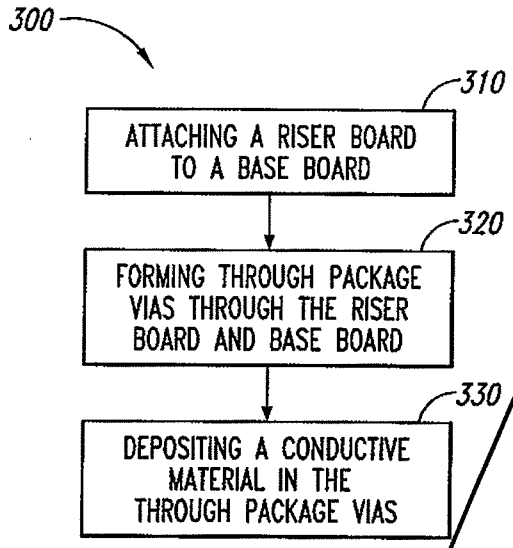

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ATTACHING A RISER BOARD TO A BASE BOARD
320
FORMING THROUGH PACKAGE VIAS THROUGH THE RISER BOARD AND BASE BOARD
330
DEPOSITING A CONDUCTIVE MATERIAL IN THE THROUGH PACKAGE VIAS

Fig. 3A

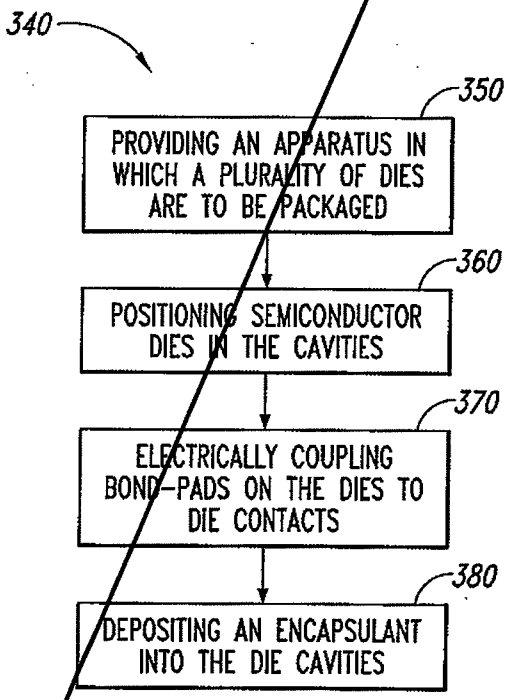

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350
PROVIDING AN APPARATUS IN WHICH A PLURALITY OF DIES ARE TO BE PACKAGED
360
POSITIONING SEMICONDUCTOR DIES IN THE CAVITIES
370
ELECTRICALLY COUPLING BOND-PADS ON THE DIES TO DIE CONTACTS
380
DEPOSITING AN ENCAPSULANT INTO THE DIE CAVITIES

Fig. 3B

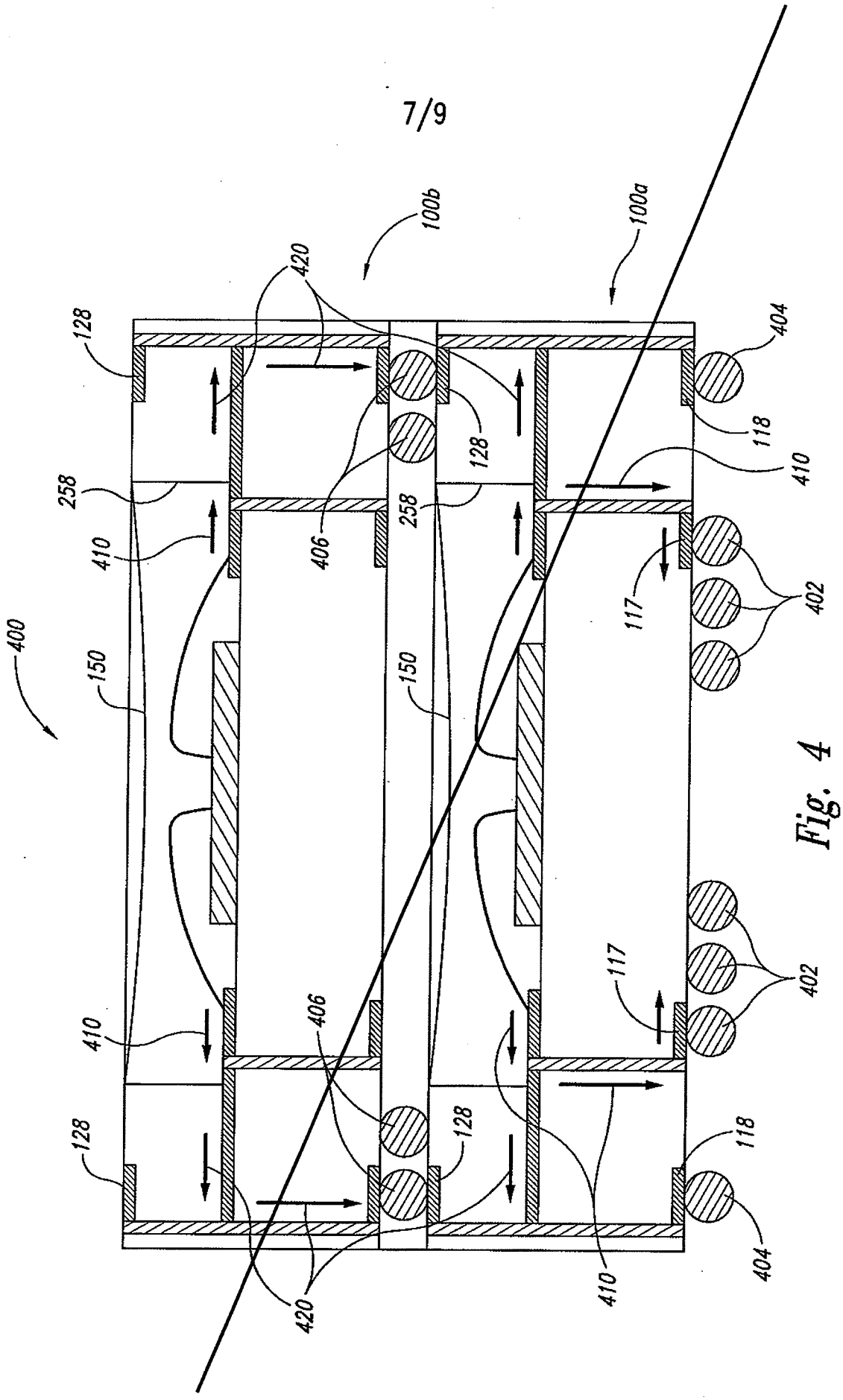

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Fig. 4

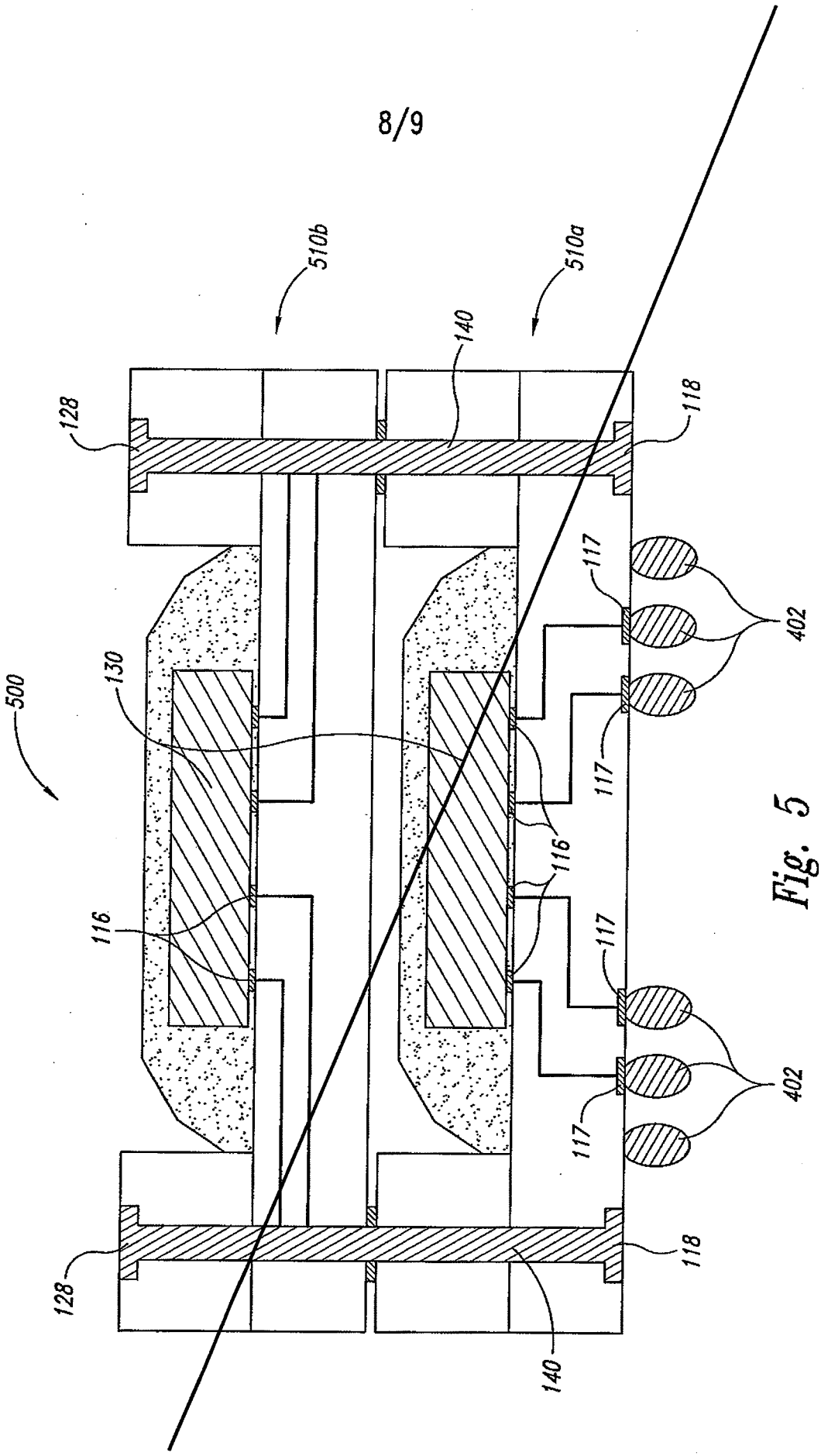

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Fig. 5

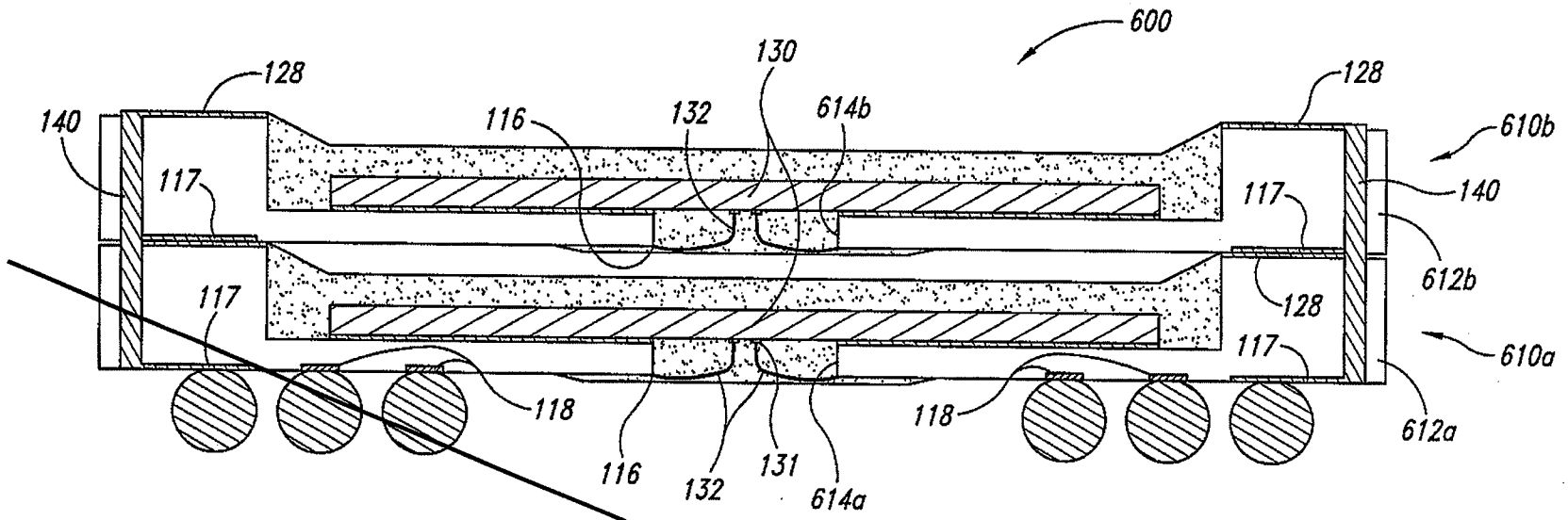

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Fig. 6

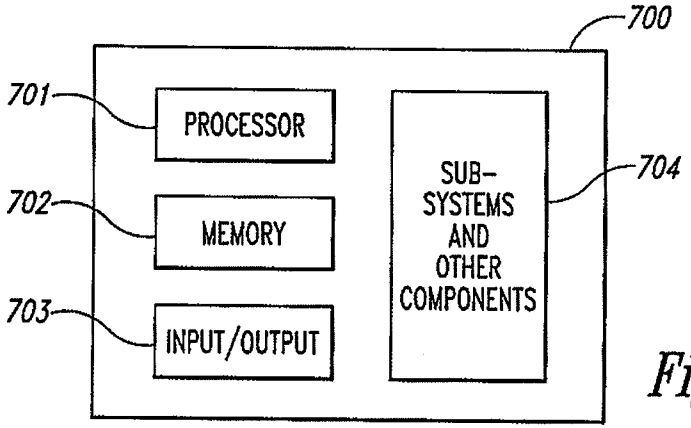

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PROCESSOR
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MEMORY
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INPUT/OUTPUT
SUB-
SYSTEMS
AND
OTHER
COMPONENTS
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Fig. 7

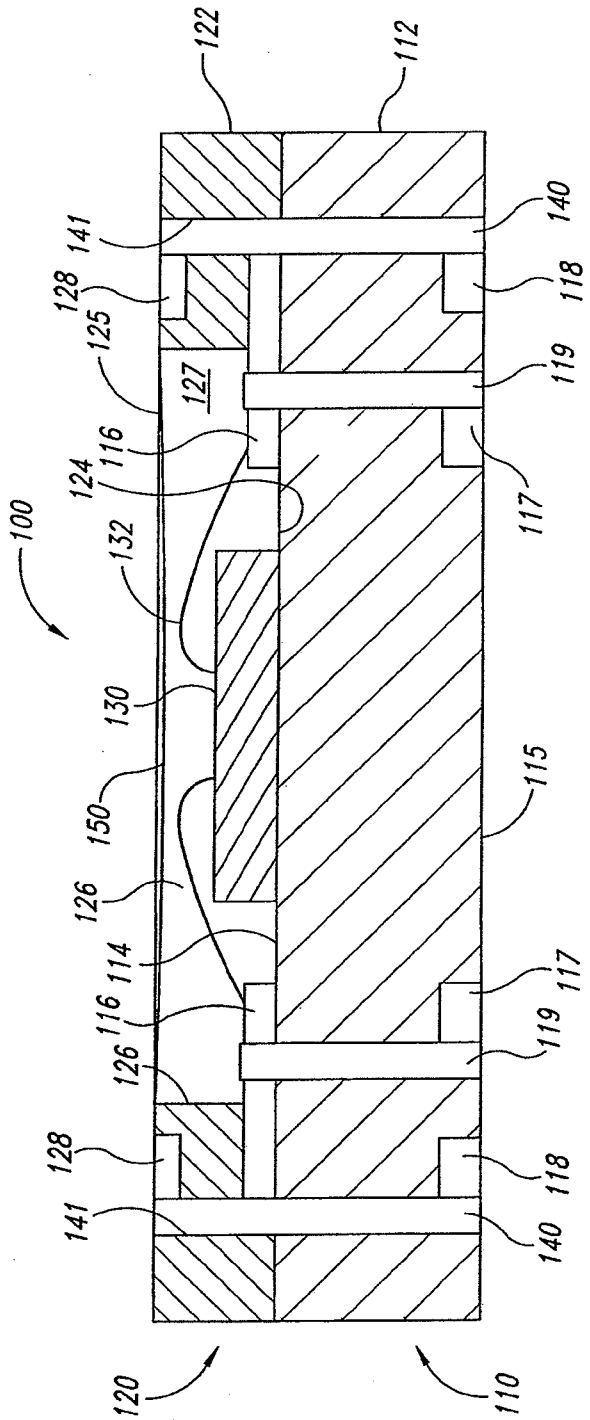

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Fig. 1

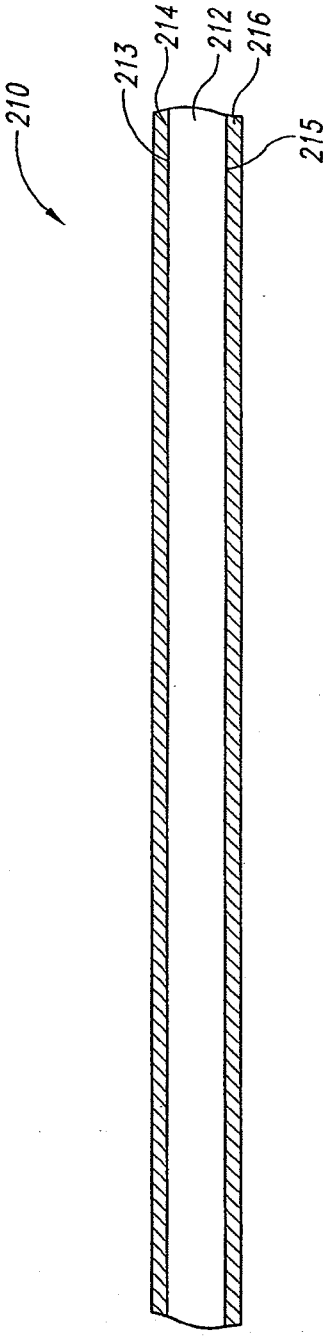

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Fig. 2A

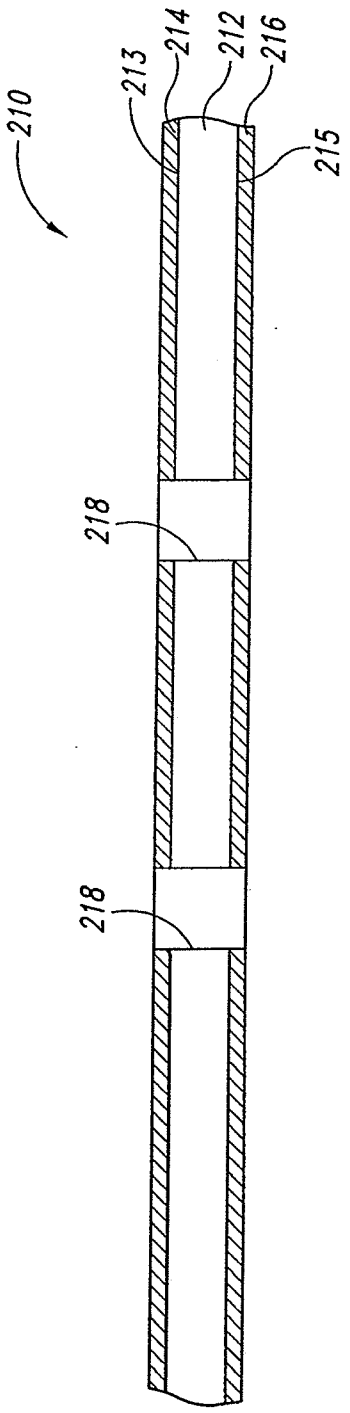

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Fig. 2B

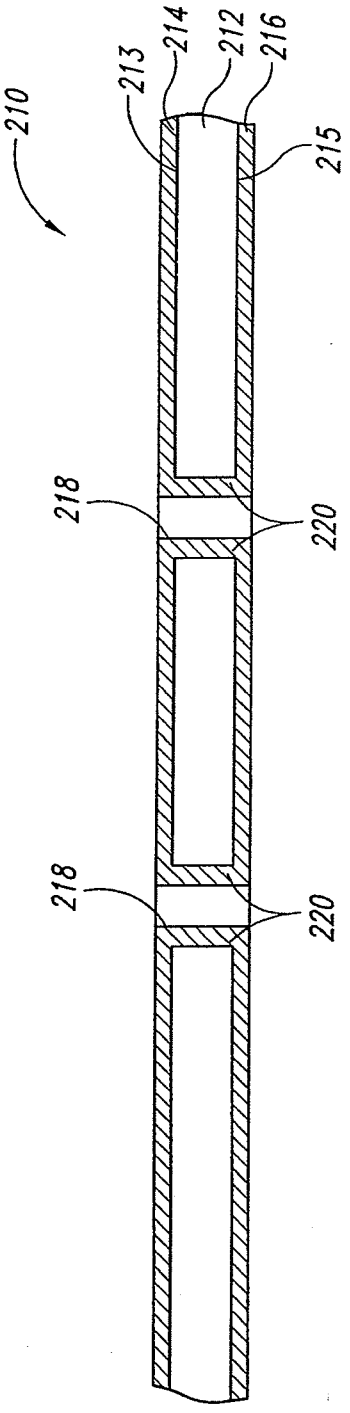

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Fig. 2C

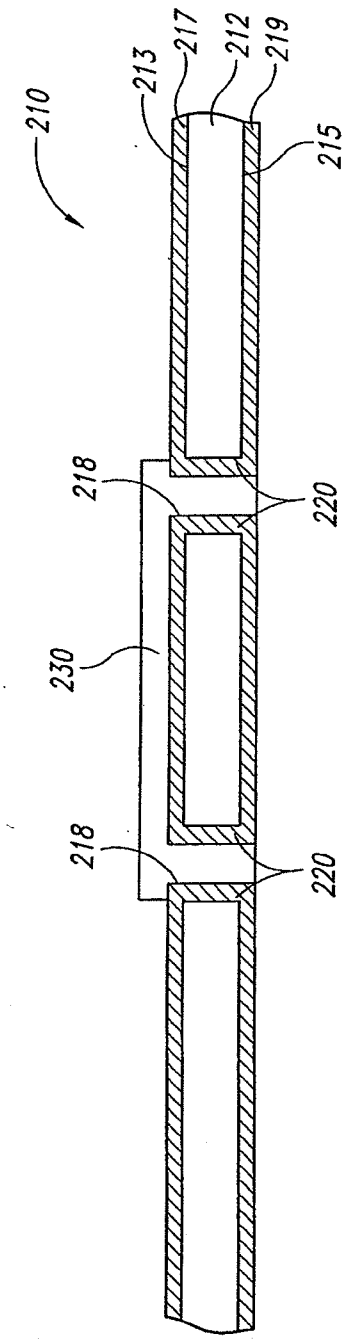

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Fig. 2D

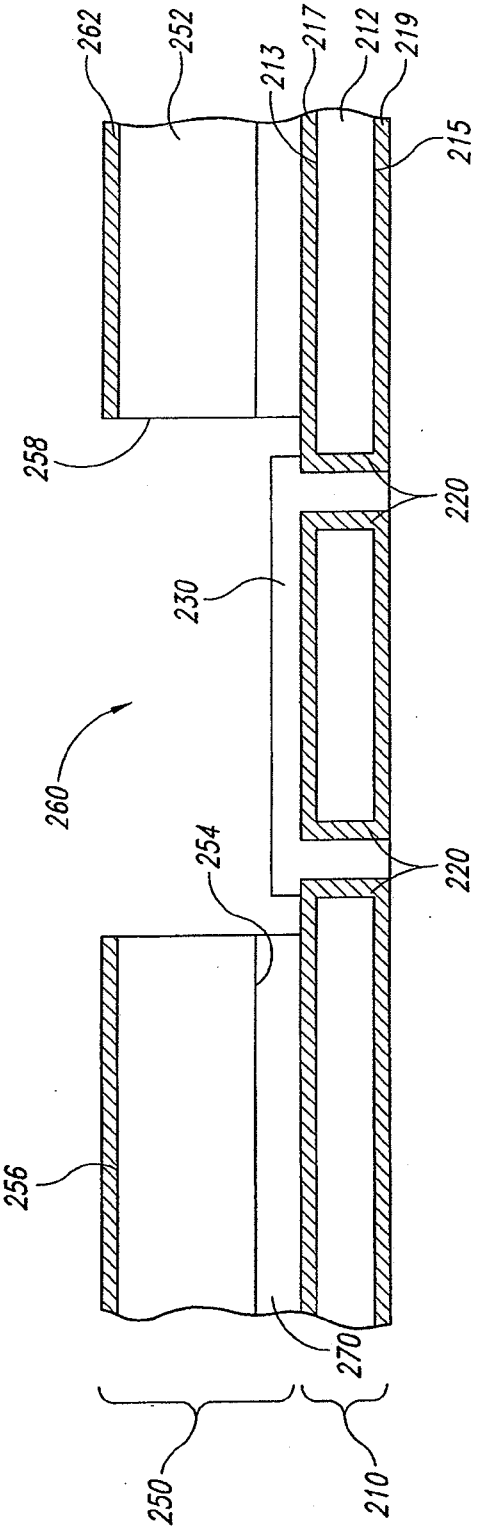

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Fig. 2E

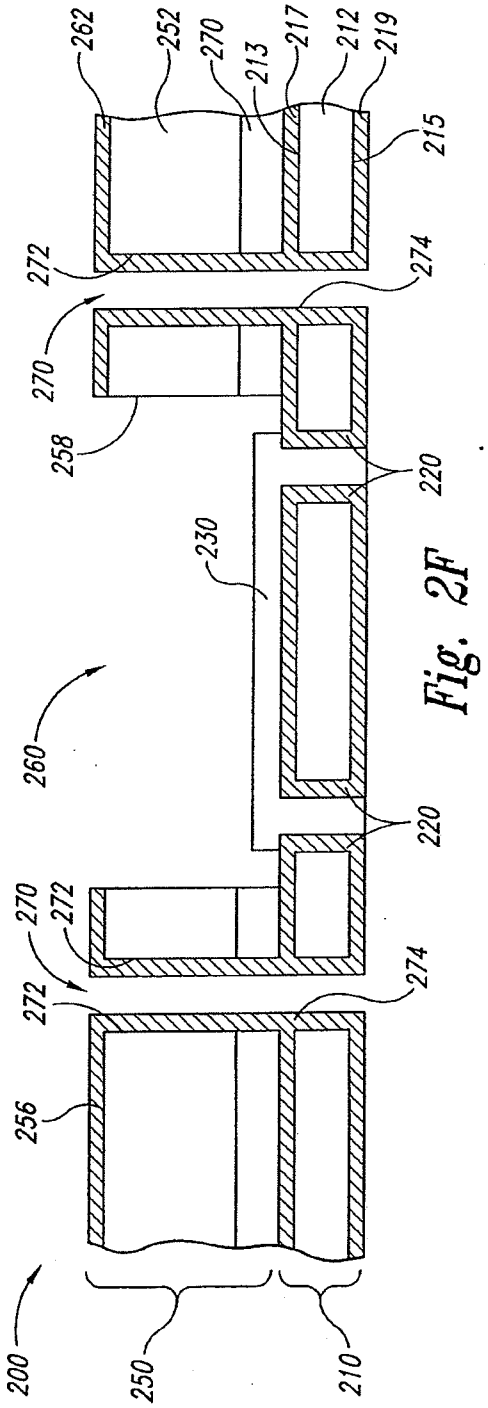

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Fig. 2F

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Fig. 2G

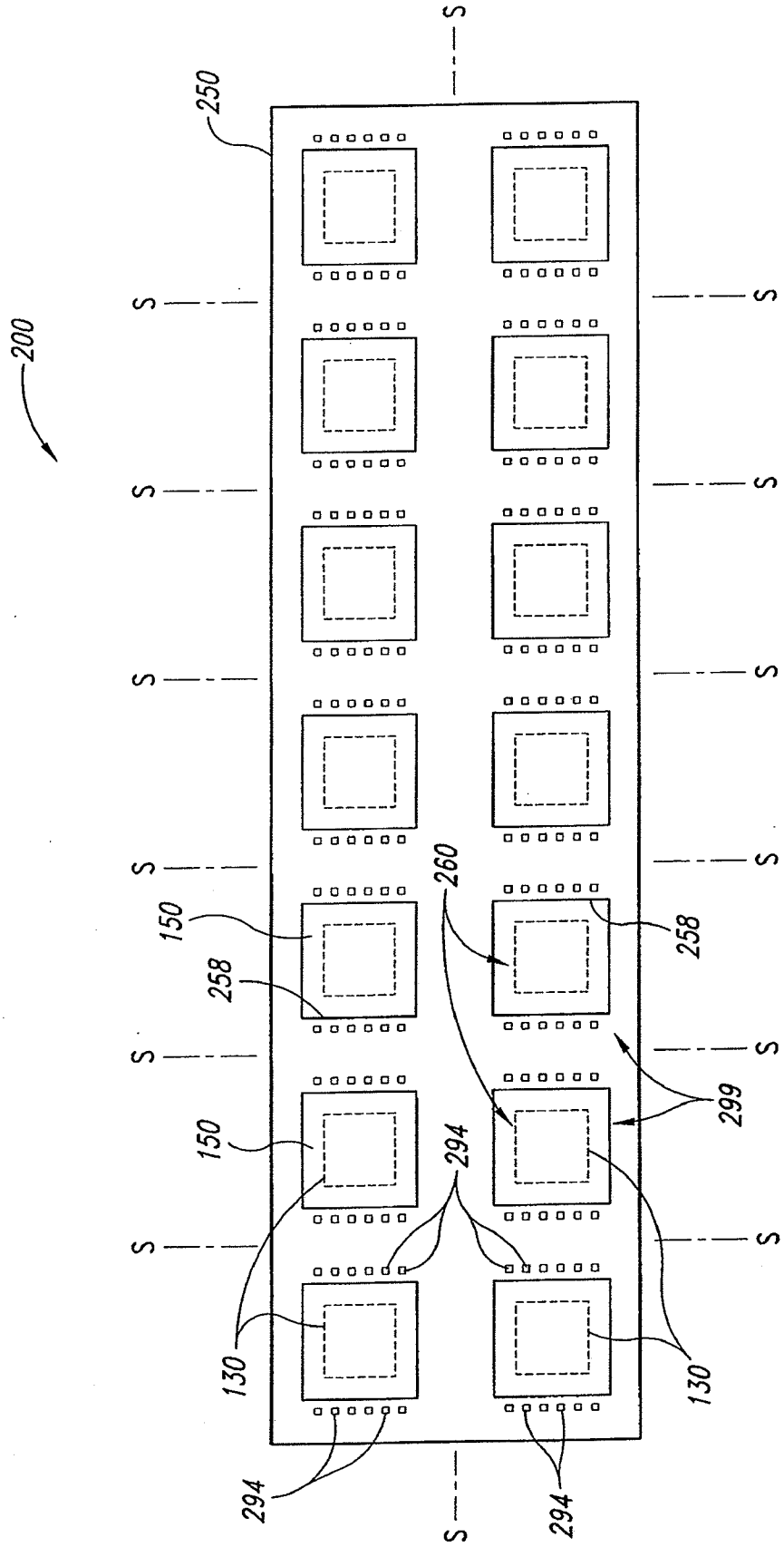


Fig. 2H

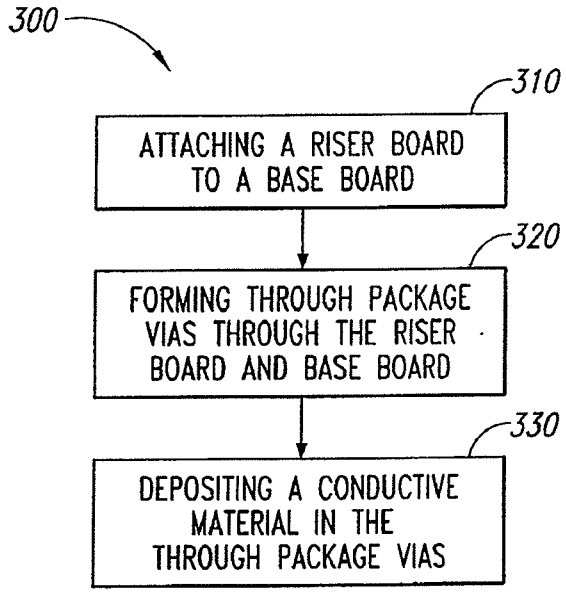

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DEPOSITING A CONDUCTIVE MATERIAL IN THE THROUGH PACKAGE VIAS

Fig. 3A

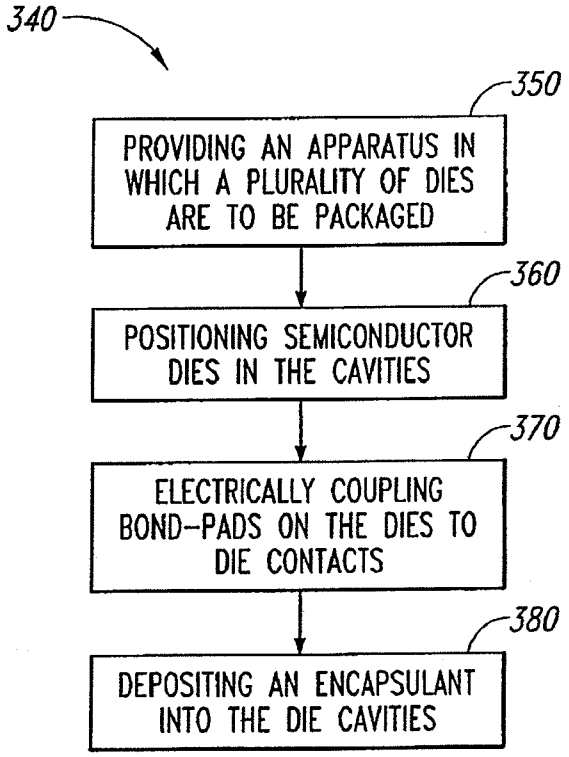

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Fig. 3B

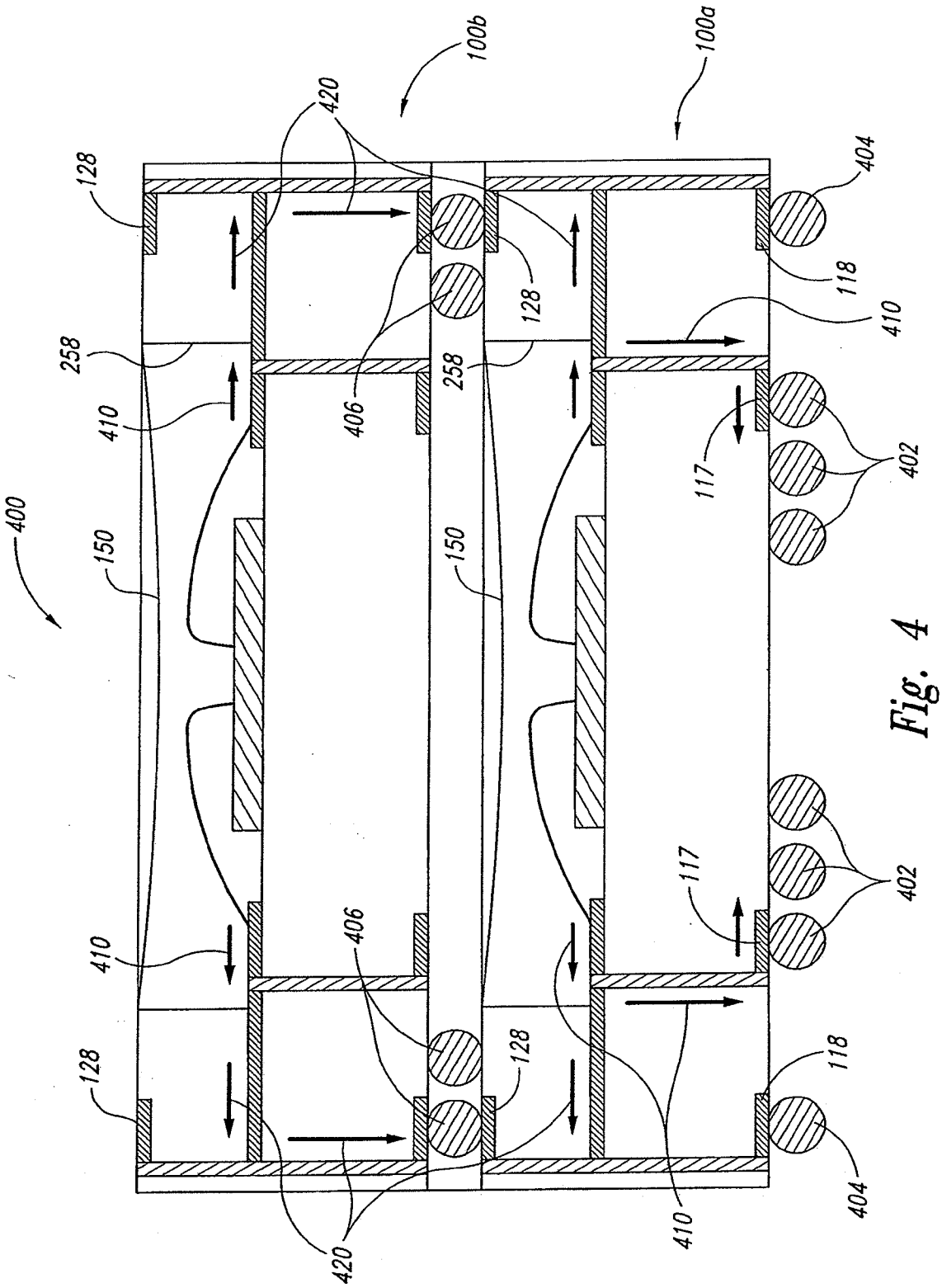

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Fig. 4

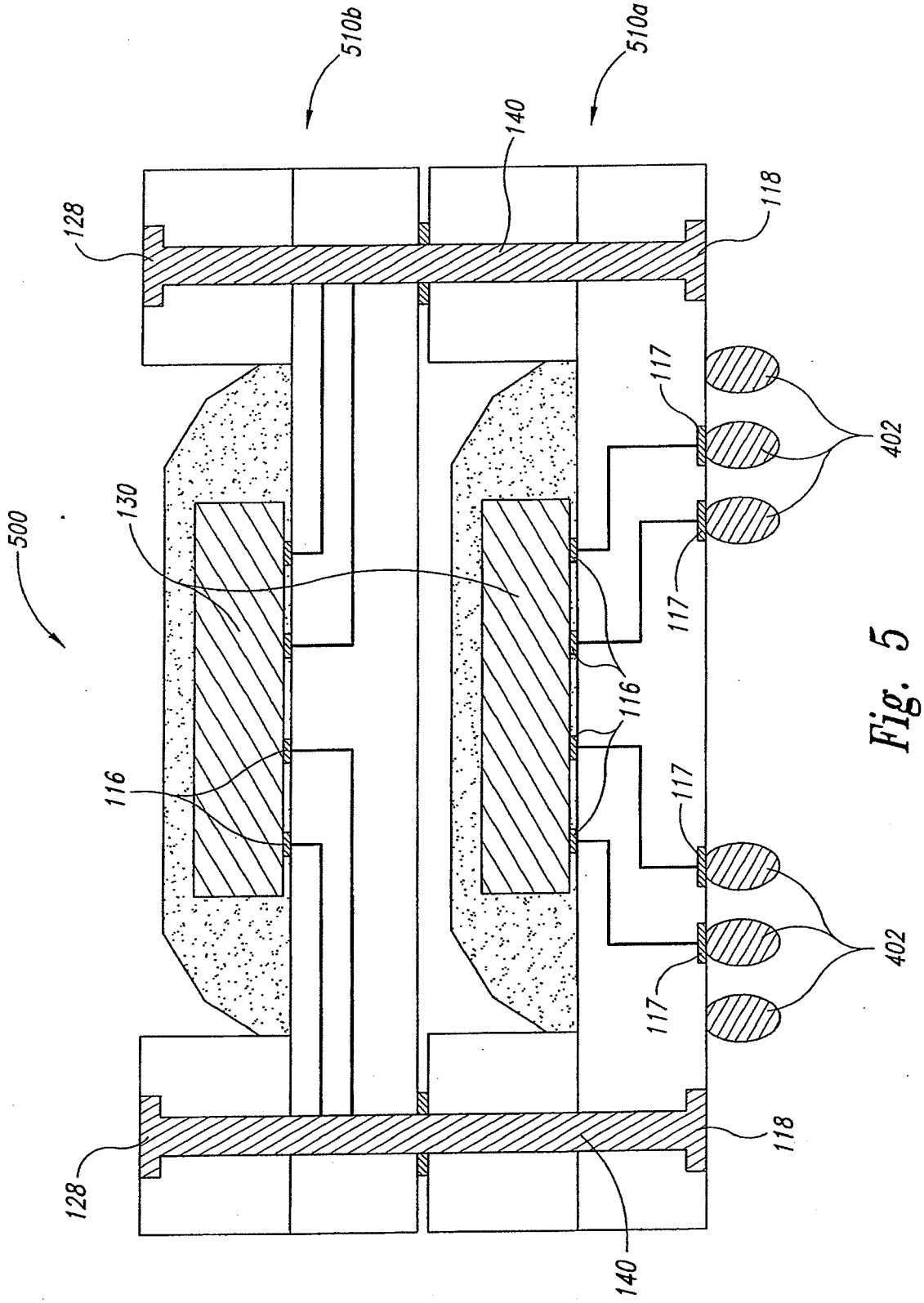

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Fig. 5

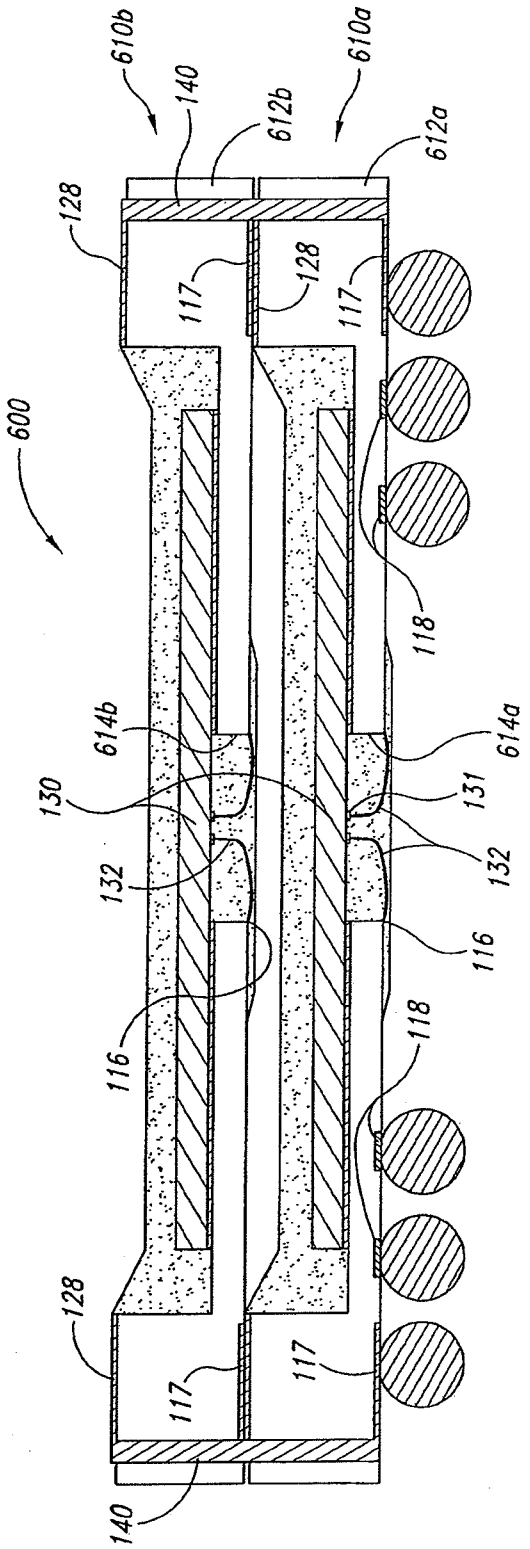

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Fig. 6

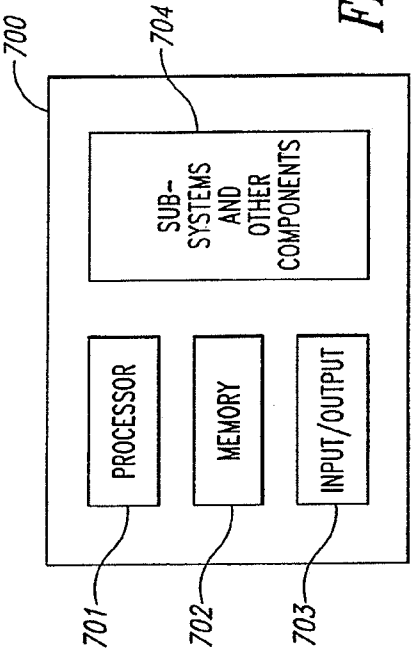

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SUB-SYSTEMS AND OTHER COMPONENTS
PROCESSOR
MEMORY
INPUT/OUTPUT
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Fig. 7