

WIRE BONDING APPARATUS

Field of the Invention

The present invention relates to a wire bonding
5 apparatus, more particularly a wire bonding apparatus
capable of detecting bonding failures of a low-capacity
device.

Background of the Invention

10 A wire bonding apparatus is an apparatus for
connecting an electrode on a semiconductor chip, which
is a first bonding point, and a lead, which is a second
bonding point, using a wire made of gold, aluminum and
the like.

15 A bonding arm is oscillated upwardly and downwardly
by a linear motor of a bonding head placed on a XY table
movable in the X and Y directions or a cam coupled to a
motor shaft of the linear motor, and a wire is led out
from a capillary mounted on a tip of an ultrasonic horn
20 of the bonding arm. And, applying a high voltage between
a tip of the wire and a discharge electrode will
generate an electric discharge. The generated discharge
energy melts the tip of the wire to form a ball at its
end. Then, the ball supported by the tip of the
25 capillary is thermocompression-bonded onto an electrode
on a semiconductor chip, which is a first bonding point,
by using an ultrasonic means and a heating means

together while being pressed thereto with mechanical pressurization force owing to an oscillation of the bonding arm, resulting in connecting the wire to the first bonding point.

5 Figs.6A to 6D are views showing processes for performing wire bonding using the wire bonding apparatus.

As shown in Fig.6A and Fig.6B, causing an electric discharge between a tip of a wire 1 led from a tip of a capillary 2 and a discharge electrode 4 for a certain period allows melting the tip of the wire 1 whereby a ball 20 is formed at the tip. Then, the capillary 2 supporting the ball 20 at the tip thereof is positioned over an electrode 12 of a semiconductor chip 13, which is a first bonding point 15.

Next, as shown in Fig.6C, ultrasonic wave oscillations are applied to the tip of the capillary 2 via an ultrasonic horn of the bonding arm at the same time as the capillary 2 is moved downwardly, the ball 20 being pressed onto the electrode 12. As a result, the wire 1 is connected to the electrode.

Then, as shown in Fig.6D, the capillary 2 is moved upward according to a predetermined loop control so as to be displaced to a lead 14, which is a second bonding point 16.

And, ultrasonic wave oscillations are applied to the tip of the capillary 2 via the ultrasonic horn at

the same time as the capillary 2 is moved downwardly, the wire 1 being pressed onto the lead 14, resulting in connecting the wire 1 to the lead 14. Then, after moving the capillary 2 upward to a predetermined height, a wire
5 cut clamp 3 is operated to cut the wire over the lead 14. Thus, one wire bonding work is finished.

In a conventional wire bonding apparatus, under a state that the ball 20 is crushed onto the electrode 12 of the semiconductor chip 13, a bonding failure
10 detection device discriminates whether or not the bonding work is completely finished, in other words, whether or not the wire bonding is successful or unsuccessful. The bonding failure detection device detects bonding failures in the following manner.

15 Fig.7 is a flowchart showing a conventional method for detecting bonding failures.

Before a bonding work, a detection zone, a starting point and a threshold value are set together (ST1, ST2). Note that it is impossible to set a detection zone, a
20 starting point and a threshold level for each wire.

Then, a wire bonding for connecting an electrode on a semiconductor chip to a lead using a wire is carried out (ST3). And, a bonding failure detecting for discriminating whether or not the wire is completely
25 bonded to the electrode on the semiconductor chip is performed (ST4). In the step, when it is discriminated that the wire bonding is unsuccessful, an error handling

for stopping the operation of the wire bonding apparatus will be performed. On the other hand, when it is discriminated that the wire bonding is successful, a subsequent wire bonding work is carried out and the bonding failure detecting will be carried out in the same manner (ST3, ST4). After all of the wire bonding work is carried out, the wire bonding work is finished (ST5).

Next, a bonding failure detection apparatus for detecting bonding failures will be explained.

Fig.8 is a block diagram showing a DC dedicated bonding failure detection apparatus of a conventionally used wire bonding apparatus. The DC dedicated bonding failure detection apparatus is for detecting bonding failures of a semiconductor chip having DC characteristics.

The DC dedicated bonding failure detection apparatus is provided with a bonding failure detection board 44 for DC and a bonding CPU board 18. The bonding CPU board 18 has an I/O port 32. The bonding failure detection board 44 for DC has an I/O port 33, a CPU 30, an A/D converter 35, an amplifier (AMP) 37, a DC generator 45 and a resistor 46.

An output 38 is connected to the wire 1 of the wire bonding apparatus shown in Fig.6. A ground (GND) 39 is connected to a bonding stage, on which the semiconductor chip 13 is placed, via the output 38.

When a bonding failure detection is carried out using the DC dedicated failure detection apparatus, voltage is applied to the electrode 12 of the semiconductor chip 13 through the resistor 46, the output 38 and the wire 1 from the DC generator 45 at wire bonding. Then, the detected signal output from the electrode 12 of the semiconductor chip 13 is input to the amplifier 37 through the wire 1 and the output signal output from the amplifier 37 is analog-digitally converted by the A/D converter 35 and then input to the CPU 30. The CPU 30 discriminates that the bonding is successful when the detected signal is within the threshold value or that the bonding is abnormal (unsuccessful) when the detected signal is out of the threshold value. Then, the signal showing whether the bonding is successful or unsuccessful is input to the bonding CPU board 18 via the I/O ports 33 and 32 for determining bonding failures.

Fig.9 is a circuit diagram showing a specific structure of an AC dedicated bonding failure detection apparatus of a conventional wire bonding apparatus (referred to Japanese Published Unexamined Application 2000-260808, p4 to 5, Fig.1). The AC dedicated bonding failure detection apparatus is for detecting failures of a semiconductor chip having AC characteristics.

A wire 1 led from a wire spool 21 passes through a space between supporting surfaces of the wire cut clamp

3 capable of supporting and releasing the wire 1 and is inserted into the capillary 2 positioned directly under the wire cut clamp 3. Between an end 22 of the wire 1 spooled around the spool 21 and a bonding stage 17, 5 which is a reference potential point, where a lead frame 11 as a frame is placed, an AC bridge circuit 5 is connected.

The AC bridge circuit 5 has an AC generator 5a including a sine-wave generator oscillating at a 10 predetermined frequency. The AC bridge circuit 5 forms a closed loop of the AC generator 5a, a first series circuit 5c1 comprising a variable resistor R1 receiving an output signal output from the AC generator 5a and a condenser C1, and a second series circuit 5c2 comprising 15 a fixed resistor R2 receiving an AC signal output from the AC generator 5a and an electric pathway from the end 22 of the wire to the bonding stage 17, which is a reference potential point.

A first connection point X of the variable resistor 20 R1 and the condenser C1 is connected to one input of a differential amplifier 6 and a second connection point Y of the fixed resistor R2 and the end 22 of the wire is connected to the other input of the differential amplifier 6.

25 Between the fixed resistor R2 and the end 22 of the wire, a coaxial cable 5b is connected for preventing exogenous noise. Thus, the coaxial cable 5b generates

capacitance C2 between a core wire and an exterior coat of the coaxial cable 5b. As a result, the capacitance C2 is equivalently connected between the fixed resistor R2 and the bonding stage 17.

5 The differential amplifier 6 comprises an operational amplifier A1, an operational amplifier A2, a resistor R3, a resistor R4 and a resistor R5. The differential amplifier 6 detects and outputs a difference in input signals to both input terminals from
10 the first connection point X and the second connection point Y. To an output terminal of the differential amplifier 6, a condenser C and a primary input terminal of a transformer 7 are connected serially.

A secondary output terminal of the transformer 7 is
15 connected to an absolute value inverter 8 which converts positive or negative AC voltage output from the transformer 7 to positive absolute voltage. A first level discriminator 9 is connected to an output terminal of the absolute value inverter 8. An output of the first
20 level discriminator 9 is input to a bonding determination circuit 26 for detecting bonding failures.

A low-pass filter 23 is connected to an output from the low-pass filter 23 is input to a secondary level discriminator 24 to an output terminal of the
25 operational amplifier A1 of the differential amplifier 6 connected to the second connection point Y of the AC bridge circuit 5. The secondary level discriminator 24

compares an output from the low-pass filter 23 with a standard signal level set beforehand. When the output from the low-pass filter 23 is larger than the standard signal level, a signal showing a logical value "0" is
5 output to an AND circuit 25. When the output from the low-pass filter 23 is smaller than the standard signal level, a signal showing a logical value "1" is output to the AND circuit 25.

A bonding detection switch 27 outputs a signal
10 showing a logical value "0" to the AND circuit 25 at a first bonding (a chip bonding) and a signal showing a logical value "1" to the AND circuit 25 at a secondary bonding (a lead bonding). The AND circuit 25 performs an AND operation of an output signal from the bonding
15 detection switch 27 and an output from the secondary level discriminator 24, and outputs a logical value "1" or "0" to a bonding determination circuit 26 at the first bonding (a chip bonding) and a logical value "0" thereto at a secondary bonding (a lead bonding).

20 The bonding determination circuit 26 is operated to detect bonding failures by reading an output signal from the AND circuit 25 at a bonding failure detection timing, in other words, at a bonding failure detection mode according to a command from the bonding apparatus,
25 when a wire is bonded to the electrode 12 on the semiconductor chip 13, which is a first bonding point, or the lead 14 of the lead frame 11, which is a second

bonding point.

Summary of Invention

The bonding failure detection apparatus of the
5 conventional wire bonding apparatus discriminates
whether the bonding is successful or unsuccessful by
judging a difference between an AC or DC output voltage
and a voltage detected at the AC or DC dedicated bonding
failure detection apparatus. In this method, the
10 detected voltage is specified as a voltage of which a
waveform becomes steady state in both the DC and AC
dedicated bonding failure detection apparatuses.
Accordingly, if the semiconductor chip and the lead
frame to be detected do not have a certain level of
15 capacitance (for example, about 100PF), a necessary
difference between an output voltage and a detected
voltage for discriminating whether the bonding is
successful or unsuccessful is hardly generated. In other
words, such a conventional failure detection apparatus
20 cannot detect bonding failures of a low-capacity object
of several PF to several dozen PF. In addition,
recently, objects to be detected tends to have low
capacitance.

An object of the present invention is to provide a
25 wire bonding apparatus capable of detecting bonding
failures of a low-capacity device.

In order to achieve above mentioned object, a wire

bonding apparatus according to the present invention for connecting an electrode of a semiconductor chip to a lead of a lead frame using a wire or bonding a bump to a pad of a semiconductor chip comprises:

5 DC pulse applying means for applying DC pulse to the wire or the bump,

 detection means for detecting a response waveform from the wire or the bump applied with the DC pulse, and

 discrimination means for discriminating whether or
10 not the wire or the bump is successfully bonding-connected by comparing the response waveform with an unsuccessful bonding response waveform obtained by applying DC pulse to an unsuccessfully bonded wire or bump.

15 According to the wire bonding apparatus, the apparatus comprises a DC pulse applying means, and a response waveform obtained by applying DC pulse from the DC pulse applying means is compared with an unsuccessful bonding response waveform, whereby a step response
20 characteristic can be detected comparing with AC sine waveform. As a result, it becomes possible to detect a difference between successful bonding and unsuccessful bonding of a low-capacity device and therefore to detect bonding failures of the device.

25 In a wire bonding apparatus according to the present invention, the DC pulse applying means is designed to apply DC pulse to a condenser via a variable

resistor as well as to the wire or the bump via a resistor, the detection means is designed to detect a response waveform from the condenser as well as a response waveform from the wire or the bump, and the
5 variable resistor is adjusted to make a product of a capacitance obtained by subtracting a capacitance of an object to be detected from a capacitance of a side of the wire or the bump and a resistance of the resistor nearly equal to a product of a capacitance of the
10 condenser and a resistance of the variable resistor.

Preferably, in a wire bonding apparatus according to the present invention, the detection means contains a circuit for shaping or processing the response waveform.

Preferably, in a wire bonding apparatus according
15 to the present invention, the waveform shaping or processing circuit contains a circuit in which the response waveform may be amplified by a differential amplifier after differential processing, and the amplified waveform may be filtered and converted into a
20 rectangular waveform or a triangular waveform.

Preferably, in a wire bonding apparatus according to the present invention, the discrimination means performs discrimination by comparing a threshold value, obtained by multiplying the unsuccessful bonding
25 response waveform by a threshold coefficient, with the response waveform.

A wire bonding apparatus according to the present

invention for connecting an electrode of a semiconductor chip to a lead of a lead frame using a wire or bonding a bump to a pad of a semiconductor chip comprises:

DC pulse applying means for applying DC pulse to
5 the wire or the bump,

detection means for detecting a response waveform from the wire or the bump applied with the DC pulse, and

discrimination means for discriminating whether or not the wire or the bump is successfully bonded,

10 wherein the discrimination means comprises the steps of:

applying DC pulse to the wire or the bump by the DC pulse applying means before the wire or the bump contacts the electrode of the semiconductor chip to
15 detect an unsuccessful bonding response waveform from the wire or the bump by the detection means;

applying DC pulse to the wire or the bump by the DC pulse applying means when the wire or the bump contacts the electrode of the semiconductor chip to detect a
20 successful bonding response waveform from the wire or the bump by the detection means;

calculating a threshold coefficient using the unsuccessful bonding response waveform and the successful bonding response waveform;

25 applying DC pulse to the wire or the bump by the DC pulse applying means after the wire or the bump are bonded to the electrode of the semiconductor chip to

detect a response waveform from the wire or the bump by the detection means; and

comparing the response waveform with a threshold value obtained by multiplying the unsuccessful bonding response waveform by the threshold coefficient.

According to a wire bonding apparatus according to the present invention, it becomes possible to detect a difference between successful bonding and unsuccessful bonding of a low-capacity device and to set a threshold coefficient and a threshold value automatically by software control.

As described above, according to the present invention, a wire bonding apparatus capable of detecting bonding failures of a low-capacity device can be provided.

Brief Description of the Drawings

Fig.1 is a block diagram schematically showing a structure of a bonding failure detection apparatus according to one embodiment of the present invention.

Fig.2 is a detail view showing a detection circuit shown in Fig.1.

Fig.3 is a view schematically showing a connection diagram between a low capacitance detection circuit and the wire bonding apparatus shown in Fig.1 and showing a successful bonding response waveform and an unsuccessful bonding (open) response waveform.

Fig.4A is a flowchart showing a method for detecting bonding failures using the bonding failure detection apparatus shown in Fig.1 while automatically setting a threshold value for a first chip and Fig.4B is
5 a flowchart showing a method for detecting bonding failures using the bonding failure detection apparatus shown in Fig.1 while automatically setting a threshold value for the subsequent chips.

Fig.5 is a graph showing a change in a detected
10 voltage V_c to a period T after applying output voltage E to a wire when bonding failure detection is performed using the bonding failure detection apparatus shown in Fig.1.

Figs.6A to 6D are views showing processes for
15 performing wire bonding using the wire bonding apparatus.

Fig.7 is a flowchart showing a conventional method for detecting bonding failures.

Fig.8 is a block diagram showing a DC dedicated
20 bonding failure detection apparatus of a conventionally used wire bonding apparatus.

Fig.9 is a circuit diagram showing a specific structure of an AC dedicated bonding failure detection apparatus of a conventional wire bonding apparatus.

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Detailed Description of Embodiment of the Invention

Referring to the attached drawings, details of the

embodiments of the present invention will be set forth.

Fig.1 is a block diagram schematically showing a structure of a bonding failure detection apparatus according to one embodiment of the present invention.

5 Fig.2 is a detail view showing a detection circuit shown in Fig.1. Fig.3 is a view schematically showing a connection diagram between a low capacitance detection circuit and the wire bonding apparatus shown in Fig.1 and showing a successful bonding response waveform and
10 an unsuccessful bonding (open) response waveform.

Fig.3 schematically shows waveforms in both cases in which a wire is successfully bonded to a semiconductor chip and a case in which a wire is unsuccessfully bonded (open) to a semiconductor chip
15 normally. When DC pulse voltage is applied to a semiconductor chip stepwise, a successful bonding waveform 48 or an unsuccessful bonding (open) waveform 49 is detected. Only the main points are explained about the part having the same structure and function as a
20 conventional apparatus, and detailed descriptions thereof are omitted.

A bonding failure detection apparatus according to this embodiment utilizes a step response using a DC pulse method. And, the bonding failure detection
25 apparatus allows various parameters, such as a detection zone and a detection starting point, to be specified for each wire. In addition, the apparatus makes it possible

to detect failures of a device having a mixture of AC characteristic and DC characteristic.

As shown in Fig.1, the bonding failure detection apparatus comprises a bonding failure detection board 10, a low capacitance detection circuit 40 and a bonding head control board 19. The bonding head control board 19 has a CPU control circuit 29 and a data communication circuit 32. The CPU control circuit 29 is connected to a touch panel (not shown) for inputting parameters, such as a detection zone, a detection starting point and a detection level (a threshold value), for each wire. The CPU control circuit 29 is connected to the data communication circuit 32.

The bonding failure detection board 10 comprises a data communication circuit 33, a CPU control circuit 30, a memory 34, a comparative circuit (not shown), an A/D converter 35, a D/A converter 36 and a pulse generator 28. The low capacitance detection circuit 40 comprises a current-limit circuit 31, a detection circuit 41 and a waveform shaping and processing circuit 42.

An input side of the data communication circuit 33 is connected to the CPU control circuit 30, and an output side of the data communication circuit 33 is connected to the data communication circuit 32. The CPU control circuit 30 is connected to the comparative circuit. The CPU control circuit 30 is connected to each of the memory 34, the A/D converter 35 and the D/A

converter 36. The D/A converter 36 is connected to the pulse generator 28. The pulse generator 28 is connected to the current-limit circuit 31, and the current-limit circuit 31 is connected to a semiconductor chip (CHIP) 43 via a wire (represented by reference number 1 in Fig.3). The A/D converter 35 is connected to the waveform shaping and processing circuit 42, and the waveform shaping and processing circuit 42 is connected to the detection circuit 41. The detection circuit 41 is connected to the semiconductor chip (CHIP) 43 via the wire (represented by reference number 1 in Fig.3).

As shown in Fig.2, the detection circuit contains a resistor R1, a variable resistor VR1, a balance condenser C1 and a resistor R2. The detection circuit is connected to a capacitive portion W/F of the capillary, a capacitive portion W/C of the wire cut clamp and a capacitive portion EFO of a discharge unit via the wire 1. When the wire 1 is bonding-connected to a pad of the semiconductor chip 43, the detection circuit is also connected to the semiconductor chip 43 via the wire 1.

That is, in a case where the wire is open with the semiconductor chip 43, the current-limit circuit 31 is connected to a terminal TP1 via the variable resistor VR1, the balance condenser C1 and the resistor R2, and connected to a terminal TP2 via the resistor R1, the capacitive portion W/F of the capillary, the capacitive portion W/C of the wire cut clamp, and the capacitive

portion EFO of the discharge unit and the resistor R2. And, in a case where the wire is bonding-connected to the pad of the semiconductor chip 43, the current-limit circuit 31 is connected to a terminal TP1 via the
5 variable resistor VR1, the balance condenser C1 and the resistor R2, and connected to a terminal TP2 via the resistor R1, the semiconductor chip 43, the capacitive portion W/F of the capillary, the capacitive portion W/C of the wire cut clamp, and the capacitive portion EFO of
10 the discharge unit and the resistor R2. The difference between the open case and the case where the wire is bonding-connected to the semiconductor chip 43 depends on only a difference whether or not the semiconductor chip 43 is connected between the current-limit circuit
15 31 and the terminal TP2. The bonding failure detection apparatus according to this embodiment utilizes the difference for detecting whether the bonding is successful or unsuccessful.

The balance condenser C1 has capacitance
20 approximately equal to a sum of capacitances of the capacitive portions of the capillary, the wire cut clamp, the discharge unit and the wiring (W/F capacitance + W/C capacitance + EFO capacitance + wiring capacitance). And, the variable resistor VR1 is adjusted
25 such that $VR1 \times C1 = R1 \times (W/F \text{ capacitance} + W/C \text{ capacitance} + EFO \text{ capacitance} + \text{wiring capacitance})$. That is, the current limit circuit 31 is designed to coincide a

product ($VR1 \times C1$) of a resistance of the variable resistor VR1 and the condenser C1 between the current-limit circuit 31 and the terminal TP1 with a product ($R1 \times (W/F \text{ capacitance} + W/C \text{ capacitance} + EFO \text{ capacitance} + \text{wiring capacitance})$) of a resistance of the resistor R1 and a sum of capacitances of the capacitive portion W/F of the capillary, the capacitive portion W/C of the wire cut clamp, the capacitive portion EFO of the discharge unit and the capacitive portion of the wiring) between the current-limit circuit 31 and the terminal TP2.

As shown in Fig.3, each of an output and a detection of the low capacitance detection circuit 40 is connected to the wire (gold wire) 1. And, a ground (GND) is connected to a bonding stage on which the semiconductor chip 43 is placed.

A method for detecting bonding failures using the aforesaid bonding failure detection apparatus will be explained referring to Fig.1 to Fig.5.

Fig.4A is a flowchart showing a method for detecting bonding failures using the bonding failure detection apparatus shown in Fig.1 while automatically setting a threshold value for a first chip. Fig.4B is a flowchart showing a method for detecting bonding failures using the bonding failure detection apparatus shown in Fig.1 while automatically setting a threshold value for the subsequent chips.

Fig.5 is a graph showing a change in a detected voltage V_c to a period T after applying output voltage E to a wire when bonding failure detection is performed using the bonding failure detection apparatus shown in Fig.1. Reference number 49 represents an unsuccessful bonding (open) waveform and reference number 48 represents a successful bonding waveform. And, reference number 47 represents an applied DC pulse waveform stepwise.

Before bonding for connecting a semiconductor chip to a lead, parameters, such as a detection zone, a detection starting point and DC pulse, are input from the touch panel for each wire which is connected to the semiconductor chip 43. Thus, the parameters are input to the CPU control circuit 29 of the bonding head control board 19.

Then, a software control sends the parameters to the CPU control circuit 30 of the bonding failure detection board 10 from the CPU control circuit 29 of the bonding head control board 19 via the data communication circuits 32 and 33 and then stores in the memory 34.

Next, as shown in Fig.4A, a wire open waveform is read into (ST11). Specifically, a tip of the wire (gold line) 1 shown in Fig.3 is melted to form a ball. Then, the capillary 2 with the ball being supported at its tip is positioned directly over the electrode of the

semiconductor chip 43, which is the first bonding point, or the capillary 2 moves downwardly. At this time, the DC pulse 47 at voltage E shown in Fig.5 is applied to the wire from the current-limit circuit 31. As shown in
5 Fig.2, the DC pulse 47 is applied to the balance condenser C1 via the variable resistor VR1 and a response output from the condenser C1 is detected at the terminal TP1 via the resistor R2. At the same time, the DC pulse 47 is applied to the capacitive portion W/F of
10 the capillary, the capacitive portion W/C of the wire cut clamp, a capacitive portion EFO of the discharge unit via the resistor R1 and a response from each capacitive portion is detected at the terminal TP2 via the resistor R2. In this case, since the wire 1 is in an
15 open state in which the wire 1 is not connected to the semiconductor chip 43, the step response waveform detected at the terminal TP2 has a form of the waveform 49 of Fig.5. The applied DC pulse 47 is variable within 1KHz to 20KHz.

20 The wire open waveform 49 detected at the detection circuit 41 is shaped and processed at the waveform shaping and processing circuit 42. Specifically, the wire open waveform 49 is amplified at the differential amplifier after HPF (differential processing), and then
25 the amplified waveform is filtered (for example, denoizing) and converted into a rectangular waveform (for example, peak-hold or sample-hold) or a triangular

waveform (for example, integral processing). The converted wire open waveform is analog-digitally converted at the A/D converter 35. The converted values are read into the CPU control circuit 30 and stored in the memory 34. And, the converted values are set to the comparative circuit from the memory 34.

The variable resistor VR1 is adjusted to coincide a product $(VR1 \times C1)$ of a resistance of the variable resistor VR1 and a capacitance of the condenser C1 between the current limit circuit 31 and the terminal TP1 with a product $(R1 \times (W/F \text{ capacitance} + W/C \text{ capacitance} + EFO \text{ capacitance} + \text{wiring capacitance}))$ of a resistance of the resistor R1 and a sum of capacitances of the capacitive portion W/F of the capillary, the capacitive portion W/C of the wire cut clamp, the capacitive portion EFO of the discharge unit and the wiring between the current-limit circuit 31 and the terminal TP2.

A relationship between a voltage Vc1 detected at the terminal TP1 and a detection period T1 is shown in Equation (1) and a relationship between a voltage Vc1 detected at the terminal TP2 and a detection period T2 is shown in Equation (2).

$$T1 = -VR1 \times C1 \times \ln\{1 - (Vc1/E)\} \quad (1)$$

$$T2 = -R1 \times C(W/C + W/F + EFO + \text{wiring}) \times \ln\{1 - (Vc1/E)\} \quad (2)$$

At an open state, since the detection circuit 41 is balanced, $T1 = T2$. On the contrary, at a successful

bonding state in which the wire is connected to the electrode of the semiconductor chip 43, since the circuit is off balance by the semiconductor chip, $T1 \neq T2$. And, the successful bonding waveform 48 shown in Fig.3
5 has larger amplitude than the unsuccessful bonding waveform 49 because of $T1 \neq T2$; the unsuccessful bonding (open) waveform 49 has smaller amplitude than the successful bonding waveform 48 because of $T1 = T2$.

Then, one wire bonding is performed and a
10 successful bonding waveform is read into (ST12). Specifically, the capillary 2 is moved downwardly while the ball being pressed to the electrode and ultrasonic oscillations are applied to the tip of the capillary 2 from the ultrasonic horn of the bonding arm, whereby the
15 wire 1 is connected to the electrode. At the same time, the DC pulse 47 at voltage E shown in Fig.5 is applied to the wire stepwise from the current-limit circuit 31 and then a successful bonding waveform is detected at the terminal TP2. As shown in Fig.2, the DC pulse 47 is
20 applied to the electrode of the semiconductor chip 43, the capacitive portion W/F of the capillary, the capacitive portion W/C of the wire cut clamp, a capacitive portion EFO of the discharge unit via the resistor R1. And, a response from each capacitive
25 portion is detected at the terminal TP2 via the resistor R2. In this case, since the wire 1 is in a successful bonding state in which the wire 1 is connected to the

semiconductor chip 43, the step response waveform detected at the terminal TP2 has a form of the waveform 48 of Fig.5. In addition, at the terminal TP1, a same waveform as the unsuccessful bonding (open) waveform is
5 detected.

The successful bonding waveform 48 detected at the detection circuit 41 is shaped and processed at the waveform shaping and processing circuit 42. Specifically, the successful bonding waveform 48 is
10 amplified at the differential amplifier after HPF (differential processing), and the amplified waveform is filtered (for example, denoizing) and then converted into a rectangular waveform (for example, peak-hold or sample-hold) or a triangular waveform (for example,
15 integral processing). The converted successful bonding waveform is analog-digitally converted at the A/D converter 35. The converted values are read into the CPU control circuit 30 and stored in the memory 34. And, the converted values are set to the comparative circuit from
20 the memory 34.

At the comparative circuit, by using the unsuccessful bonding (open) waveform 49 and the successful bonding waveform 49, a threshold coefficient is calculated and stored in the memory 34 (ST13).

25 Then, the capillary 2 is moved upwardly according to a predetermined loop control toward the lead, which is the second bonding point. At this time, DC pulse 47

at voltage E shown in Fig.5 is applied stepwise to the wire from the current-limit circuit 31 and a step response waveform is detected at the terminal TP2. In addition, at the terminal TP1, a same waveform as the
5 unsuccessful bonding (open) waveform is detected.

Each of the step response waveform and the unsuccessful bonding (open) waveform detected at the detection circuit 41 is shaped and processed at the waveform shaping and processing circuit 42.
10 Specifically, each of the step response waveform and the unsuccessful bonding (open) waveform is amplified at the differential amplifier after HPF (differential processing), and then each amplified waveform is filtered (for example, denoizing) and converted into a
15 rectangular waveform (for example, peak-hold or sample-hold) or a triangular waveform (for example, integral processing). Each of the converted step response waveform and the unsuccessful bonding (open) waveform is analog-digitally converted at the A/D converter 35. Each
20 converted values are read into the CPU control circuit 30 and stored in the memory 34. And, each converted values are set to the comparative circuit from the memory 34.

At the comparative circuit, by using the
25 unsuccessful bonding (open) waveform and the threshold coefficient, a threshold value is introduced. And, the threshold value is compared with the step response

waveform. If the threshold value is equal to the step response waveform, it is discriminated that the bonding is unsuccessful; if the threshold value is not equal to the response waveform, it is discriminated that the bonding is successful (ST14). Thus, wire bonding failures are detected. These processing is controlled by software.

The unsuccessful bonding state (wire open state) differs from the successful bonding state (normally bonding state) in the step response waveform for the capacitance of the semiconductor chip 43, resulting in difference between the successful bonding waveform 48 and the unsuccessful bonding (open) waveform 49, as shown in Fig.5. The difference is proportional to the capacitance of the semiconductor chip, as shown in Equation (2). Accordingly, even if an object (semiconductor chip) to be detected has very low capacitance, it becomes possible to detect such difference. Detecting the difference allows discrimination of a successful wire bonding or an unsuccessful wire bonding. Amplifying the difference by HPF, filtering and converting into a rectangular waveform or a triangular waveform facilitates the discrimination of the successful wire bonding or the unsuccessful wire bonding.

A result of the successful bonding or the unsuccessful bonding is sent to the CPU control circuit

29 of the bonding head control board 19 via the data communication circuits 33 and 32. When the unsuccessful bonding is sent thereto, error handling such as stopping the wire bonding apparatus will be carried out. When the
5 successful bonding is sent thereto, subsequent bonding will be performed.

When it is discriminated that the wire is perfectly bonded, parameters for the subsequent wire bonding are set by software control. And, a bonding failure
10 detection (ST12 to ST14) is performed at wire bonding. The detection work is repeated until all of the wires on the chip are bonded. And, when all of the wires on the chip are bonded, a wire bonding work is finished (ST15).

Then, a subsequent chip is subjected to a wire
15 bonding and a bonding failure detecting. Since the detecting work for the subsequent chip uses the threshold coefficient set at the first chip, a step for setting a threshold value is omitted. Hereinafter, a bonding failure detecting method for subsequent chips
20 will be explained referring to Fig.4B.

As shown in Fig.4B, a wire open waveform is read into (ST21). The step ST21 is the same as the step ST11, so its detail description is omitted.

The wire open waveform detected at the detection
25 circuit 41 is shaped and processed at the waveform shaping and processing circuit 42. Then, the shaped and processed wire open waveform is analog-digitally

converted at the A/D converter 35. The converted values are read into the CPU control circuit 30 and stored in the memory 34. And, the converted values are set to the comparative circuit from the memory 34. And, the
5 variable resistor VR1 is adjusted for balancing in the same manner of the first chip.

Then, after the wire is connected to the electrode of the semiconductor chip, the capillary 2 is moved upwardly according to a predetermined loop control
10 toward the lead, which is the second bonding point. At this time, DC pulse 47 at voltage E shown in Fig.5 is applied stepwise to the wire from the current-limit circuit 31 and a step response waveform is detected at the terminal TP2 (ST22). In addition, at the terminal
15 TP1, a same waveform as the unsuccessful bonding (open) waveform is detected.

Each of the step response waveform and the unsuccessful bonding (open) waveform detected at the detection circuit 41 is shaped and processed at the
20 waveform shaping and processing circuit 42. Then, each of the shaped and processed step response waveform and unsuccessful bonding (open) waveform is analog-digitally converted at the A/D converter 35. The converted values are read into the CPU control circuit 30 and stored in
25 the memory 34. And, the converted values are set to the comparative circuit from the memory 34.

At the comparative circuit, by using the

unsuccessful bonding (open) waveform and the threshold coefficient, a threshold value is introduced. And, the threshold value is compared with the step response waveform. If the threshold value is equal to the step
5 response waveform, it is discriminated that the bonding is unsuccessful; if the threshold value is not equal to the response waveform, it is discriminated that the bonding is successful (ST24). Thus, bonding failures are detected. These processings are controlled by software.

10 A result of the successful bonding or the unsuccessful bonding is sent to the CPU control circuit 29 of the bonding head control board 19 via the data communication circuits 33 and 32. When the unsuccessful bonding is sent thereto, error handling such as stopping
15 the wire bonding apparatus will be carried out. When the successful bonding is sent thereto, subsequent bonding will be performed.

When it is discriminated that the wire is perfectly bonded, parameters for the subsequent wire bonding are
20 set by software control. And, a bonding failure detection (ST22, ST14) is performed at wire bonding. The detection work is repeated until all of the wires on the chip are bonded. And, when all of the wires on the chip are bonded, a wire bonding work is finished (ST25).

25 The aforesaid wire bonding method and bonding failure detecting method will be applied to a wire bonding for connecting the wire to the lead, which is a

second bonding point 16, shown in Fig.6, in addition to the wire bonding for connecting the wire to the electrode of the semiconductor chip, which is a first bonding point 15, shown in Fig.6. In addition, the
5 aforesaid bonding failure detection method may be applicable for a case where the tip of the wire is melted to form a ball at its tip and the ball is connected to an electrode or a pad of a semiconductor chip as a bump.

10 According to this embodiment, as shown in Fig.2, the detection circuit 41 has the resistor R1, the variable resistor VR1, the balance condenser C1 and the resistor R2 and is connected to the capacitive portion W/F of the capillary, the capacitive portion W/C of the
15 wire cut clamp and the capacitive portion EFO of the discharge unit via the wire 1. A relationship between a voltage Vc1 detected at the terminal TP1 and a detecting period T1 is expressed by Equation (1) and a relationship between a voltage Vc1 detected at the
20 terminal TP2 and a detecting period T2 is expressed by Equation (2). In an open state, since the detection circuit 41 is balanced, $T1=T2$; in a successful bonding state in which the wire is connected to the electrode of the semiconductor chip 43, since the detection circuit
25 is off balance by the semiconductor, $T1 \neq T2$. Accordingly, the successful bonding state differs from the unsuccessful bonding state (the wire open state) in the

step response waveform for the capacitance of the semiconductor 43. Since the difference is proportional to the capacitance of the semiconductor chip, as shown in Equation (2), even if an object (semiconductor) to be
5 detected has very low capacitance, it becomes possible to detect the difference. So, even if an object to be detected has very low capacitance impossible of being detected using a conventional bonding failure detection apparatus, bonding failures thereof can be detected.

10 In this embodiment, since DC pulse 47 is applied, a step response characteristic can be detected comparing with AC sine waveform, resulting in facilitating detecting a difference between an open state and a successful bonding state. And, a step response waveform
15 output by applying DC pulse is subjected to the HPF processing (differential processing) to extract only a build up change in the waveform, resulting in facilitating detecting a difference between an unsuccessful bonding and a successful bonding.

20 The present invention is not limited solely to the embodiment specifically exemplified above, and those skilled in the art will appreciate that various changes and modifications can be made therein without departing from the scope of the invention. For example, in this
25 embodiment, parameters such as a detection zone and a starting point are set for each wire; however, uniformed parameters may be used.

In this embodiment, when the capillary 2 is moved to the lead, which is a second bonding point, a step for detecting a step response waveform from the terminal TP2 is performed just one time, that is, DC pulse 47 is applied to the wire and the response waveform is detected just one time. However, it is also possible that DC pulse 47 is applied to the wire several times at one wire bonding and several response waveforms are detected. In this case, each of the response waveforms is compared with a threshold value for determination. Alternatively, an average waveform of the response waveforms is compared with a threshold value. In addition, an average of the maximum response waveform and the minimum response waveform, or the both maximum and minimum response waveforms are compared with a threshold value.

And, in this embodiment, a threshold value is automatically set using the flowchart shown in Fig.4A. However, it is possible that a threshold value is set in such a manner that an operator inputs a predetermined threshold value to the bonding failure detection apparatus and the flowchart shown in Fig.4B, not the flowchart shown in Fig.4A, is used.

For example, the predetermined threshold value may be set in the following manner. By using the bonding failure detection apparatus, shown in Fig.1 and Fig.2, a successful bonding waveform and an unsuccessful bonding

(open) waveform are measured beforehand for each wire for the first bonding point, the second bonding point or a bonding bump, and a value dividing a sum of the successful bonding waveform and the unsuccessful bonding form by two is specified as the threshold value. Alternatively, the successful bonding waveform and the unsuccessful bonding waveform may be measured at several times. In such a case, an average of the several measurements may be specified as to a threshold value.

10 This embodiment is constructed such that the low capacitance detection circuit 40 is separated from the bonding failure detection board 10. However, it is also possible that the low capacitance detection circuit 40 is arranged in the bonding failure detection board.

15

What is claimed is:

1. A wire bonding apparatus for connecting an electrode of a semiconductor chip to a lead of a lead frame using a wire or bonding a bump to a pad of a semiconductor
5 chip comprising:

DC pulse applying means for applying DC pulse to the wire or the bump,

detection means for detecting a response waveform from the wire or the bump applied with the DC pulse, and

- 10 discrimination means for discriminating whether or not the wire or the bump is successfully bonding-connected by comparing the response waveform with an unsuccessful bonding response waveform obtained by applying DC pulse to an unsuccessfully bonded wire or
15 bump.

2. A wire bonding apparatus according to claim 1,

wherein said DC pulse applying means is designed to apply DC pulse to a condenser via a variable resistor as
20 well as to the wire or the bump via a resistor,

said detection means is designed to detect a response waveform from said condenser as well as a response waveform from said wire or said bump, and

said variable resistor is adjusted to make a
25 product of a capacitance obtained by subtracting a capacitance of an object to be detected from a capacitance of a side of said wire or said bump and a

resistance of said resistor nearly equal to a product of a capacitance of said condenser and a resistance of said variable resistor.

5 3. A wire bonding apparatus according to claims 1 or 2,
 wherein said detection means contains a circuit for
shaping or processing said response waveform.

 4. A wire bonding apparatus according to claim 3,
10 wherein said waveform shaping or processing circuit
contains a circuit in which the response waveform is
amplified by a differential amplifier after differential
processing, and the amplified waveform is filtered and
converted into a rectangular waveform or a triangular
15 waveform.

 5. A wire bonding apparatus according to any one of
claims 1 to 4,
 wherein said discrimination means performs
20 discrimination by comparing a threshold value, obtained
by multiplying said unsuccessful bonding response
waveform by a threshold coefficient, with said the
response waveform.

25 6. A wire bonding apparatus for connecting an electrode
of a semiconductor chip to a lead of a lead frame using
a wire or bonding a bump to a pad of a semiconductor

chip comprising:

DC pulse applying means for applying DC pulse to the wire or the bump,

detection means for detecting a response waveform
5 from the wire or the bump applied with the DC pulse, and

discrimination means for discriminating whether or not said wire or said bump is successfully bonded,

wherein said discrimination means comprises the steps of:

10 applying DC pulse to said wire or said bump by said DC pulse applying means before said wire or said bump contacts the electrode of the semiconductor chip to detect an unsuccessful bonding response waveform from said wire or said bump by said detection means;

15 applying DC pulse to said wire or said bump by said DC pulse applying means when said wire or said bump contacts the electrode of the semiconductor chip to detect a successful bonding response waveform from said wire or said bump by said detection means;

20 calculating a threshold coefficient using said unsuccessful bonding response waveform and said successful bonding response waveform;

applying DC pulse to said wire or said bump by said DC pulse applying means after said wire or said bump are
25 bonded to the electrode of the semiconductor chip to detect a response waveform from said wire or said bump by said detection means; and

comparing said response waveform with a threshold value obtained by multiplying said unsuccessful bonding response waveform by said threshold coefficient.