CLAIMS

1. A semiconductor package structure, comprising:

a first package structure, comprising an intermediary layer and a molding compound, wherein a plurality of first connection pads are disposed on the intermediary layer, and the molding compound wraps the intermediary layer and is coplanar to the plurality of first connection pads;

a second package structure, disposed on the intermediary layer and electrically connected to the plurality of first connection pads,

wherein a gap is formed between the first package structure and the second package structure;

wherein the first package structure further comprises:

a base plate;

at least one first chip stack body, disposed on the base plate; and

at least one second chip stack body, disposed on the base plate and spaced apart from the first chip stack body,

wherein the intermediary layer is disposed on the first chip stack body and the second chip stack body;

wherein the first chip stack body and the second chip stack body are connected with each other by means of the intermediary layer.

2. The semiconductor package structure of claim 1, wherein the first chip stack body comprises one first chip, and the second chip stack body comprises one second chip; and

wherein the first chip is electrically connected to the second chip by means of the intermediary layer.

3. The semiconductor package structure of claim 2, wherein the first chip or the second chip is connected to the base plate by means of a lead wire.

4. The semiconductor package structure of claim 1, wherein the first chip stack body comprises a first lower chip and a first upper chip that are stacked onto one another, and the second chip stack body comprises a second lower chip and a second upper chip that are stacked onto one another; and

wherein the intermediary layer is disposed on the first upper chip and the second upper chip, and the first upper chip is electrically connected to the second upper chip by means of the intermediary layer.

5. The semiconductor package structure of claim 4, wherein the first upper chip or the second upper chip is connected to the base plate by means of a lead wire.

6. The semiconductor package structure of claim 5, wherein each of the first lower chip and the second lower chip is connected to the base plate by means of a lead wire respectively.

7. The semiconductor package structure of claim 5, wherein the first lower chip is electrically connected to the first upper chip, and the second lower chip is electrically connected to the second upper chip.

8. The semiconductor package structure of any of claims 1 to 7, wherein the intermediary layer comprises:

a first surface, wherein the plurality of first connection pads are disposed on the first surface;

a second surface, disposed opposite to the first surface, wherein a plurality of second connection pads are disposed on the second surface; and

a plurality of signal channels, configured to connect the plurality of first connection pads and the plurality of second connection pads with each other.

9. The semiconductor package structure of claim 8, wherein the first chip stack body and the second chip stack body comprise a plurality of lead wire pads, and the plurality of lead wire pads are connected to the plurality of second connection pads by means of a re-distribution layer.

10. The semiconductor package structure of claim 8, wherein the plurality of second connection pads connected to the first chip stack body and the second chip stack body are connected to each other by means of a re-distribution layer.

11. The semiconductor package structure of claim 1, wherein the first chip stack body and the second chip stack body are disposed on the base plate by means of a bonding layer.

12. The semiconductor package structure of claim 11, wherein the base plate comprises a virtual channel, the bonding layer is located on the virtual channel, and a heat conductivity coefficient of the virtual channel is greater than a heat conductivity coefficient of the bonding layer.

13. The semiconductor package structure of claim 1, further comprising a filling layer, wherein the gap is fully filled with the filling layer.

14. The semiconductor package structure of claim 13, wherein a heat conductivity coefficient of the filling layer is greater than a heat conductivity coefficient of the molding compound.

15. The semiconductor package structure of claim 13, wherein a volume of a filler in the filling layer is less than a volume of a filler in the molding compound.

16. The semiconductor package structure of claim 11, wherein the bonding layer comprises a first bonding layer and a second bonding layer, the second bonding layer is located on the first bonding layer, and an elastic modulus of the second bonding layer is greater than an elastic modulus of the first bonding layer.

17. A method for manufacturing a semiconductor package structure, comprising:

providing a first package structure, wherein the first package structure comprises an intermediary layer and a molding compound, a plurality of first connection pads are disposed on the intermediary layer, and the molding compound wraps the intermediary layer and is coplanar to the plurality of first connection pads;

providing a second package structure, wherein the second package structure is disposed on the intermediary layer and electrically connected to the plurality of first connection pads,

wherein a gap is formed between the first package structure and the second package structure;

wherein the first package structure further comprises:

a base plate;

at least one first chip stack body, disposed on the base plate; and

at least one second chip stack body, disposed on the base plate and spaced apart from the first chip stack body,

wherein the intermediary layer is disposed on the first chip stack body and the second chip stack body;

wherein the first chip stack body and the second chip stack body are connected with each other by means of the intermediary layer.