

- 1 -

"IMPROVEMENTS IN OR RELATING TO DATA TRANSMISSION AND PROCESSING SYSTEMS"

(H)

This invention relates to data transmitting and processing systems and is especially advantageous for and primarily intended for such systems wherein data is collected from a plurality of terminal units under the control of control data supplied from a
5 central processing unit to said terminal units.

There is a known data transmission system in which data devices such as instruments and detectors, are set up at different positions and transmit items of data to a central processing unit and are controlled by the latter under the control of data delivered
10 from the central processing unit to said devices. The central processing unit, which is installed in a central processing room, is connected to a plurality of terminal units coupled to data devices directly through parallel transmission lines. Data items are transmitted to the central processing unit and control data is
15 supplied to the data devices each time a request is made to the central processing unit.

In order to obtain easier control by the central processing unit in a system of this nature, identifying numbers are allotted to the types of data devices in the system and also to the data
20 devices of each type, each data device being thus given a number, generally known as a "logic device number" which is composed of the aforesaid allotted numbers. The terminals connected to the devices are allotted numbers generally called "physical device numbers". It is necessary to effect device number conversion

in order to bring the logic device numbers and the physical device numbers into mutual correspondence.

Since only requested data is sent and received in the known data transmission system, such data has to be transmitted with a device number attached.

Conventional known device number conversion has the serious disadvantage of being undesirably time consuming because it relies on a conversion index system each time a request is made to the central processing unit for data transmission and reception.

There is the further disadvantage that the device number converter employed has to have an undesirably large storage capacity which makes it expensive. Moreover, if device numbers are required to be altered or added to at any time, doing this involves a complex and time-consuming procedure.

An object of the present invention is to provide an improved data transmission and processing system in which the need to attach a physical device number to each item of data is avoided and accordingly tedious and time-consuming conversion between device numbers is eliminated.

Another object is to provide an improved data transmission and processing system which is such that the central processing unit therein can be made capable of processing data at a higher speed than it could otherwise do.

A further object is to provide an improved data transmission and processing system which is such as to include a device number

converter having a storage capacity which is smaller than it would otherwise have to be.

According to this invention in one aspect, a data transmission and processing system includes a central processing unit; a
5 transmission control unit connected thereto; a plurality of terminal units connected to said transmission control unit and each having an identifying physical number allotted thereto; a plurality of data devices coupled respectively to the terminal units and each having an identifying logic number allotted thereto; a data memory
10 in each terminal unit for storing in predetermined addresses in said memory control data supplied from the central processing unit and data from the data devices coupled to that terminal; a memory in the transmission control unit for storing at predetermined addresses in said memory the content of the data memories in the terminal
15 units; and a device number converter for bringing the physical device numbers into correspondence with the logic device numbers and for storing at addresses corresponding with the logic device numbers those addresses in the transmission control unit memory at which data with said logic device numbers is to be written.

20 According to this invention in another aspect a data transmission and processing system includes a central processing unit; a transmission control unit connected thereto; a plurality of terminal units, to which identifying physical device numbers are allotted, connected to said transmission control unit; a plurality
25 of data devices coupled respectively to said terminal units and

having identifying logic device numbers, respectively allotted thereto; a first data memory in each terminal unit for storing at predetermined addresses therein control data supplied from said central processing unit and collected data from the associated data devices; a second memory in the transmission control unit for storing at predetermined addresses therein the content of said first data memories, and a device number converter also in said transmission control unit for bringing the physical device numbers into correspondence with the logic device numbers and storing at addresses corresponding to the logic device numbers those second memory addresses at which data on said logic device numbers is to be written; and means in said transmission control unit and said terminal units for communicating all stored data therebetween.

The invention is illustrated in and explained in connection with the accompanying drawings, in which:-

Figure 1 is a block diagram of one form of system in which conversion in accordance with this invention is used;

Figure 2 is a block diagram showing the internal arrangement of one form of transmission control unit in the system illustrated by Figure 1;

Figure 3 is a block diagram showing the internal arrangement of one form of terminal unit in the system illustrated by Figure 1;

Figure 4 is a block diagram illustrating principal portions of the transmission control unit of Figure 2 and the terminal unit of Figure 3;

Figure 5 is an explanatory timing diagram relating to data transmission and request processing;

Figure 6 is a diagram typifying the structure of data to be transmitted;

5 Figure 7 is a diagram illustrating the manner in which items of data flow;

Figure 8 is a diagram which is explanatory of the device number conversion effected in accordance with the present invention; and

10 Figure 9, which is provided for purposes of comparison with Figure 8, is a similar diagram explanatory of the device number conversion effected in a known conversion method.

Refer first to Figure 9 which illustrates the conversion effected in a known device number conversion system. When data A with a logic device number A_1 is sent to a processing internal
15 buffer in a central processing unit, the logic device number A_1 is located by the index of a logic device table in a device number converter to determine a corresponding address A_2 . The corresponding address A_2 is then located in a physical device table to find a physical device number A_3 . The data A can now be transmitted with
20 the physical device number A_3 to a data transmission buffer, from which the data will be sent to a terminal unit over a given transmission line. Data B delivered from a data device is supplied from a terminal unit along with a physical device number B_1 to the data transmission buffer. In the central processing unit (CPU), the
25 physical device number B_1 is located by the index of a physical

22

device table to find a corresponding address B_2 , which is then searched for in the logic device table to determine a corresponding logic device number B_3 . The collected data B with the logic device number B_3 can now be written into the processing internal buffer.

5 With this known conversion method, therefore, logic device numbers are converted into physical device numbers or vice versa by means of a device number conversion index each time a request is made by the central processing unit. This process is time-consuming and accordingly severely limits the processing speed of the central
10 processing unit. Since a physical device number is attached to each item of data for its transmission, transmission control is complex. Moreover the device number converter must have a large storage capacity and this involves considerable cost. Furthermore the device number converter has an irregular number and address arrangement,
15 and this involves a complex and time-consuming procedure if, for any reason, additional device numbers are required to be inserted in the tables, as will happen if a new data device is required to be added in an existing installed system or if a device number has to be altered because a data device is moved to a different location.

20 Refer now to Figure 1. This shows a system in which a central processing unit (CPU) 1 is connected through a connector line 3 to a transmission control unit 2 having therein what may be called a second data memory (MEBD) for storing updated control data and collected data through uniform collection of data transmitted at a
25 constant period, all data items being sent and received between



terminal units at a constant period. In accordance with the present invention, the transmission control unit 2 incorporates a device number converter having addresses corresponding to logic device numbers, and MFDB addresses in which data on which logic device numbers are to be written are stored at the addresses of the device number converter. In other words, the addresses of the data items stored in the MFDB themselves correspond to the physical device numbers.

The transmission control unit 2 is connected to a plurality of terminal units 6 (there may be any number but only three LS.1, LS.2, LS.3 are shown) coupled in series by a 1-bit transmission line 7 for bit serial transmission of data. Each terminal unit 6 is connected to one or more data devices 4 by connector lines 5.

Referring now to Figure 2, the transmission control unit 2 has a data memory 8 (hereinafter called an "MFDB") serving as a second data memory and connected to a processor (microprocessor) 9 which is coupled with a request control interface 10 for the central processing unit 1 and with a transmission control interface 11 for the terminal units 6.

In Figure 3, each terminal unit 6 has a data memory 12 (hereinafter called an "LFDB") coupled with a processor (microprocessor) 13 which is connected to a transmission control interface 14 coupled with the transmission control interface 11 and is also connected to a field interface 15 for the devices 4. The connecting or coupling lines are indicated at 5 and 7, one of the lines 7

providing input to 14 from the transmission control unit 2.

The data memory 8 in the transmission control unit 2 and the data memory 12 in each terminal 6 are constructed and arranged as shown in Figure 4. As will be seen, the MFDB has a series of control data memories OUT.1, OUT.2, OUT.3 for delivering control data to the terminal units 6 (LS.1, LS.2, LS.3), respectively, and a series of collected data memories IN.1, IN.2, IN.3 for receiving collected data from the terminal units 6, respectively. The memories have addresses corresponding to the devices connected to the terminal units for storing control data or collected data to or from the data devices. The transmission control unit 2 also has a device number converter 16 constituted for example by a ROM (read-only-memory) and having addresses corresponding to the logic device numbers. An address for a logic device number as selected by the central processing unit 1 stores therein an address of the MFDB at which data for the device corresponding to such a selected logic device number is to be stored. More specifically, when the logic device number of a particular device is selected, the address of the MFDB at which data from a particular device is to be stored is read out of the converter 16 thereby to effect address assignment for the MFDB for access to data. Such device number conversion will be described in detail later on.

In Figure 4, only the LFDB for the terminal unit LS.1 is shown, but the LFDB construction for the other terminal units is similar. Thus, the LFDB has control data memories OUT.1, OUT.2, OUT.3

corresponding to the control data memories OUT.1, OUT.2, OUT.3 in the MFDB, and collected data memories IN.1, IN.2, IN.3 corresponding to the collected data memories IN.1, IN.2, IN.3 in the MFDB.

Therefore, the MFDB corresponds with the LFDB for all the terminal
5 units. Control data from the central processing unit 1 is written into a given address in one of the control data memories OUT.1, OUT.2, OUT.3 of the MFDB, and collected data is read out of a given address in one of the collected data memories IN.1, IN.2, IN.3 of the MFDB and delivered to the central processing unit 1. The content
10 of the control data memory of the MFDB is transmitted over a line 7 to each terminal unit, and the content of the collected data memory of the LFDB in each of the terminal units is transmitted over a line 7 into the collected data memory of the MFDB. A corresponding device 4 is controlled on the basis of control data stored in the
15 LFDB. Data collected from a device 4 over a connector line 5 is written into a given address in the collected data memory of LFDB.

Timing for data transmission and request processing will now be described with reference to Figure 5, in which a unit time interval is represented by one second. The unit time interval is
20 divided into two portions, namely an earlier portion of 500 milliseconds serving as a transmission time interval T_a followed by a later portion T_b of 500 milliseconds serving as a request processing time interval T_b . During the transmission time interval T_a , all control data items stored in the MFDB are transmitted from the
25 control data memories OUT.1, OUT.2, OUT.3 successively over a

transmission line 7 in a bit serial transmission mode. Each terminal unit (LS.1, LS.2, LS.3) 6 takes in control data addressed to itself, and stores such control data in the control data memory of the LFDB thereof. Then, the terminal units deliver their own collected data items from the collected data memories successively in to a transmission line 7 in a bit serial transmission mode, and the delivered data items are stored in the collected data memories IN.1, IN.2, IN.3 of the MFDB. Accordingly, during the transmission time interval Ta, six frames of data OUT.1, OUT.2, OUT.3, IN.1, IN.2, IN.3 are transmitted over a transmission line 7 as shown in Figure 6.

During the next request processing time interval Tb, control data from the central processing unit 1 is stored in the MFDB, and requested collected data is delivered to the central processing unit 1. The data collected is updated data which was collected from each terminal unit 6 in the preceding 500 milliseconds, and is immediately supplied to the central processing unit 1. The control data as delivered at this time will be transmitted to the LFDB in each terminal unit 6 during the next following transmission time interval Ta. Assuming there are one hundred data devices connected to each terminal unit (there may be any number), and that there are ten terminal units connected in series by a transmission line 7, and that one element of input and output information is sent to and supplied from each device, ten frames OUT.1 to OUT.10 of 1000 items of control data and ten frames IN.1 to IN.10 of 1000 items of collected data will be transmitted during the transmission time

interval T_a . Such data transmission can be satisfactorily effected, with a margin of time to spare, in 500 milliseconds in a unit transmission time interval T_a of one second. If a greater amount of data is to be transmitted (as in a case in which there are more
5 than 1000 devices) the unit time interval may be selected at a larger value, e.g. 1.5 seconds, or the ratio between the transmission time interval T_a and the request processing time interval T_b may be selected at a value other than that of equality.

Operation with regard to the control of the data devices by
10 control data issued from the central processing unit and with regard to the supply to the central processing unit of data collected by said devices will now be explained with the aid of Figure 7.

Referring to Figure 7 assume that items A, B, C of control data for the devices 4 coupled to the terminal units 6 are delivered
15 from the central processing unit 1 through the request control interface 10 to the processor 9, and are written thereby at given address storage locations in the control data memories OUT.1, OUT.2, OUT.3 of the MFDB, during a request processing time interval T_b-1 . When the control data is thus written in, device number conversion
20 in accordance with this invention is effected. How this is done will be explained in detail later herein. The control data is then transmitted from the transmission control interface 11 during a next transmission time interval T_a-2 . The transmission control interface 14 of the terminal unit LS.1 picks up the control data A
25 from the control data memory OUT.1, and the received control data A

is stored by the processor 13 in a given address storage location in the LFDB. The control data items of the frames OUT.2, OUT.3 are allowed to pass through the terminal unit LS.1. During this time, the control data for the device 4 is delivered from the field interface 15, and data is collected from the device 4, thereby performing sampling. Likewise, the terminal units LS.3 successively receive the control data B, C from the control data memories OUT.2, OUT.3 and store the control data into their LFDBs. Sampling operation is performed between the terminals and their devices in a period other than their own data frames. In the frame IN.1 after the frame OUT.3, the transmission control interface 14 in the terminal unit LS.1 delivers the collected data from the LFDB thereof. Likewise, the terminal units LS.2, LS.3 deliver their own collected data successively during the frames IN.2, IN.3. The terminal units effect sampling with the devices 4 after all items of collected data have been delivered and before a request processing time interval T_b-2 and their own frames OUT in a following transmission time interval T_a-3 . During this time, the devices 4 are controlled by the control data items A, B, C, respectively, and newly collected data items A', B', C' are stored in the LFDBs of the terminal units LS.1, LS.2, LS.3. Thereafter, control data in the frames OUT.1, OUT.2, OUT.3 is collected by the LFDB of each terminal during the transmission time interval T_a-3 , and the collected data in the LFDB is delivered in the frames IN.1, IN.2, IN.3. The collected data A', B', C' is transmitted (which serves to confirm the control data A, B, C) and

is stored in the MFDB. In a next request processor time interval Tb-3, the collected data A', B', C' is collected to the central processing unit 1 in response to a request from the latter, thereby confirming the control data A, B, C. The period of time in which one set of control data is delivered and confirmed, that is, the processing time, is about 3 seconds as a maximum. For simply obtaining collected data, such updated data can be gathered in the request processing time interval Tb-1, or in the next request processing time interval Tb-2 at the latest, so that the processing time will be shorter, being one second as a maximum.

All items of data are transmitted between the transmission control unit 2 and the terminal units 6 in a certain order in a bit serial mode for storage at given addresses. Thus, the addresses in the data memory MFDB correspond respectively to the physical device numbers of the devices, and there is no need to attach a physical device number to each data, but to transmit only data in a certain order as described. This simplifies device number conversion as will now be further explained with reference to Figure 8.

Figure 8 shows the manner in which control data from a processing internal buffer 17 in the central processing unit 1 is sent, together with a logic device number, to the transmission control unit 1. As already described, the transmission control unit 2 is equipped with the device number converter 16. In the illustrated embodiment, logic device numbers are represented by four-figure numbers 0000 - 9999 each composed of a two-figure number indicative

of a particular device type and a two-figure number indicative of a particular device. The addresses in the converter 16 are constituted by coded numbers which are logic device numbers per se, and there are stored at such addresses those addresses in the data memory MFDB at which items of data on devices corresponding to the logic device numbers are to be written. Thus, if the processing internal buffer 17 is supplied with control data (C) for a logic device number 0100, a corresponding address am-1 is immediately found from the address 0100 in the converter 16, and the control data (C) is written in at the address am-1 in the data memory MFDB 8. Likewise, when control data (D) for a logic device number 0001 is given, a corresponding address am+1 is found from the address 0001 in the converter 16, and the data (D) is written in at the address am+1 in the MFDB. Accordingly, the need for locating a logic device number through the use of an index, as in known systems, is avoided and a corresponding address can be directly determined from a logic device number. This results in the advantage that the converter may be of considerably smaller storage capacity than that of the converter in a comparable known system and addresses therein can be simply arranged in order of logic device numbers. Further, if a new data device is required to be added in an already existing system and a corresponding new address has to be added to the converter, it is merely necessary to write the corresponding address at an address in the converter equal to a logic device number assigned to the newly added data device.

Although in the illustrated embodiment hereinbefore described, the invention is illustrated as applied to a system using bit series data transmission, the invention is not limited to its application to data transmission systems with bit series data transmission but is applicable to all data transmission systems in which items of data are sent and received between a transmission control unit and terminal units, and the transmission control unit and terminal units have predetermined addresses for storing data therein.

As will now be appreciated, in systems in accordance with the present invention, all data items are transmitted and received between a transmission control unit and terminal units to which a number of instruments, detectors or other data devices are connected, and the transmission control unit and the terminal units have predetermined addresses where data is to be written. No physical device number needs to be assigned to each data, and hence the time-consuming process of device number conversion is rendered unnecessary, with the result that transmission control can be effected simply and economically. Since corresponding addresses in the second data memory are written in addresses in the converter which correspond to logic device numbers, respectively, data can be directly read out and written in with a resulting increased speed of data processing in the central processing unit. Furthermore, because of the simple address arrangement in, and the relatively low storage capacity required in, the converter, data input operation and device number management is facilitated.

32

Although a preferred embodiment of the invention has been particularly described and illustrated the invention is not limited thereto and many changes and modifications may be made therein without departing from the scope of the said
5 invention as defined in the claims.

Attention is directed to the specification accompanying our co-pending Application No. 8230489 (corresponding to Japanese Application No. 172332/81) which describes related subject-matter.

CLAIMS

1. A data transmission and processing system including a central processing unit; a transmission control unit connected thereto;
5 a plurality of terminal units connected to said transmission control unit and each having an identifying physical number allotted thereto; a plurality of data devices coupled respectively to the terminal units and each having an identifying logic number allotted thereto; a data memory in each terminal unit for storing in predetermined
10 addresses in said memory control data supplied from the central processing unit and data from the data devices coupled to that terminal; a memory in the transmission control unit for storing at predetermined addresses in said memory the content of the data memories in the terminal units; and a device number converter for
15 bringing the physical device numbers into correspondence with the logic device numbers and for storing at addresses corresponding with the logic device numbers those addresses in the transmission control unit memory at which data with said logic device numbers is to be written.
- 20 2. A data transmission and processing system including a central processing unit; a transmission control unit connected thereto; a plurality of terminal units, to which identifying physical device numbers are allotted, connected to said transmission control unit; a plurality of data devices coupled respectively to said terminal
25 units and having identifying logic device numbers, respectively



34

allotted thereto; a first data memory in each terminal unit for storing at predetermined addresses therein control data supplied from said central processing unit and collected data from the associated data devices; a second memory in the transmission control unit for storing at predetermined addresses therein the content of said first data memories, and a device number converter also in said transmission control unit for bringing the physical device numbers into correspondence with the logic device numbers and storing at addresses corresponding to the logic device numbers those second memory addresses at which data on said logic device numbers is to be written; and means in said transmission control unit and said terminal units for communicating all stored data therebetween.

3. A system as claimed in claim 1 or 2 wherein the terminal units are in series and communication of data between the transmission control unit and the terminal units is effected in a bit serial transmission mode.

4. A system as claimed in claim 3 wherein data communicated between the transmission control unit and the terminal units is transmitted and received in a unit time interval which is divided into at least a transmission time interval and a request processing time interval, control data from the second data memory being sent to the terminal units and supplied data from the first data memories being transmitted to the transmission control unit in said transmission time interval, control data from said central processing



* C L M S *

unit being delivered to the transmission control unit and requested collected data being delivered from said transmission control unit in the request processing time interval.

- 5 5. A system as claimed in claim 4 wherein the unit time interval is one second.
6. A system as claimed in claim 4 or 5 wherein the unit time interval is divided into halves of which one is the transmission time interval and the other is the request processing time interval.
- 10 7. A system as claimed in any of the preceding claims and having a transmission control unit substantially as herein described with reference to Figure 2.
8. A system as claimed in any of the preceding claims and having terminal units substantially as herein described with reference to Figure 3.
- 15 9. A system as claimed in any of the preceding claims wherein the transmission control unit and the terminal units are constructed and arranged substantially as herein described with reference to Figure 4.
- 20 10. Data transmission and processing systems as claimed in any of the preceding claims and constructed to operate substantially as herein described with reference to Figure 8.

