

ABSTRACT OF THE DISCLOSURE

A memory system configured to support internal data (DQ) termination of a data buffer is provided. The memory system includes a first memory module, which is a target memory module accessed by an external device, and a second memory module, which is a non-target memory module not accessed by the external device. The second memory module performs the internal DQ termination on an internal data path during an internal operation mode in which data communication is performed by using the internal data path between internal memory chips. Signal reflection over the internal data path is reduced or prohibited due to the internal DQ termination, and thus, signal integrity is improved.

[FIG. 2]