

CLAIMS:

1. A semiconductor device, comprising:
a fin including silicon;
a layer including germanium over a portion of the fin, the layer having a thickness of 2 nanometers (nm) or less, wherein the portion of the fin includes tensile strain and has a width of 4 nm or less between two portions of the layer;
a gate structure over the layer, the gate structure including a gate electrode and a gate dielectric, the gate dielectric between the layer and the gate electrode;
a source region including semiconductor material and n-type dopant; and
a drain region including semiconductor material and n-type dopant, the portion of the fin between the source and drain regions.
2. The semiconductor device of claim 1, wherein the layer includes 10 atomic% to 90 atomic% germanium.
3. The semiconductor device of claim 1, wherein the layer includes compressive strain.
4. The semiconductor device of claim 1, wherein the fin also includes germanium.
5. The semiconductor device of claim 1, wherein another portion below the portion of the fin includes a width greater than 10 nm.
6. The semiconductor device of claim 1, wherein the source and drain regions include epitaxial silicon.
7. The semiconductor device of claim 1, wherein the portion of the fin has a width of 4 nm between the two portions of the layer and the layer has a thickness of 2 nm.
8. The semiconductor device of claim 1, wherein the layer also includes silicon.

9. An integrated circuit comprising the semiconductor device of claim 1.
10. A complementary metal oxide semiconductor (CMOS) circuit comprising the semiconductor device of claim 1.
11. The semiconductor device of claim 1, wherein the tensile strain included in the portion of the fin comprises at least 2.0 gigapascals (GPa) of stress.
12. The semiconductor device of claim 1, wherein the fin extends from a substrate, the substrate comprised of a silicon wafer in a (110) orientation, and wherein the fin includes a <110> channel orientation.
13. The semiconductor device of claim 12, wherein the fin is native to the substrate.
14. An integrated circuit including at least one transistor device, the integrated circuit comprising:
 - a fin consisting essentially of silicon;
 - a layer including germanium over a portion of the fin, the layer having a thickness of 2 nanometers (nm) or less, wherein the portion of the fin includes tensile strain and has a width of 4 nm or less between two portions of the layer;
 - a gate structure over the layer, the gate structure including a gate electrode and a gate dielectric, the gate dielectric between the layer and the gate electrode;
 - a source region including semiconductor material and n-type dopant; and
 - a drain region including semiconductor material and n-type dopant, the portion of the fin between the source and drain regions.
15. The integrated circuit of claim 14, wherein the layer includes 25 atomic % to 100 atomic % germanium.
16. The integrated circuit of claim 14, wherein the source and drain regions include epitaxial silicon.

17. The integrated circuit of claim 14, wherein the tensile strain included in the portion of the fin comprises at least 2.0 gigapascals (GPa) of stress.
18. The integrated circuit of claim 14, wherein the fin extends from a substrate, the substrate comprised of a silicon wafer in a (110) orientation, and wherein the fin includes a $\langle 110 \rangle$ channel orientation.
19. The integrated circuit of claim 18, wherein the fin is native to the substrate.
20. An integrated circuit including at least one transistor device, the integrated circuit comprising:
a fin including silicon;
a layer consisting essentially of silicon and germanium over a portion of the fin, the layer having a thickness of 2 nanometers (nm) or less, wherein the portion of the fin includes tensile strain and has a width of 4 nm or less between two portions of the layer;
a gate structure over the layer, the gate structure including a gate electrode and a gate dielectric, the gate dielectric between the layer and the gate electrode;
a source region including semiconductor material and n-type dopant; and
a drain region including semiconductor material and n-type dopant, the portion of the fin between the source and drain regions.
21. The integrated circuit of claim 20, wherein the fin consists essentially of silicon.
22. The integrated circuit of claim 20, wherein the source and drain regions include epitaxial silicon.
23. The integrated circuit of claim 20, wherein the tensile strain included in the portion of the fin comprises at least 2.0 gigapascals (GPa) of stress.

24. The integrated circuit of claim 20, wherein the fin extends from a substrate, the substrate comprised of a silicon wafer in a (110) orientation, and wherein the fin includes a <110> channel orientation.

25. The integrated circuit of claim 24, wherein the fin is native to the substrate.