

WHAT IS CLAIMED IS:

1. A three-dimensional (3D) memory device, comprising:
a substrate;
a memory stack comprising a plurality of interleaved conductor layers and dielectric layers on the substrate; and
a memory string extending vertically through the memory stack and comprising:
a semiconductor plug in a lower portion of the memory string;
a protective dielectric layer on the semiconductor plug; and
a memory film above the protective dielectric layer and along a sidewall of the memory string.
2. The 3D memory device of claim 1, wherein the protective dielectric layer is a native oxide layer of the semiconductor plug.
3. The 3D memory device of claim 1, wherein the semiconductor plug is an epitaxially-grown silicon plug.
4. The 3D memory device of claim 1, wherein a thickness of the protective dielectric layer is between about 1 nm and about 5 nm.
5. The 3D memory device of claim 1, wherein the protective dielectric layer is not disposed along the sidewall of the memory string.
6. The 3D memory device of claim 1, wherein the protective dielectric layer abuts the sidewall of the memory string.
7. A method for forming a three-dimensional (3D) memory device, comprising:
forming a first dielectric deck comprising a first plurality of interleaved sacrificial layers and dielectric layers on a substrate;
forming a first opening extending vertically through the first dielectric deck;

forming a semiconductor plug in a lower portion of the first opening;
forming a protective dielectric layer on the semiconductor plug;
forming a sacrificial layer on the protective dielectric layer in the first opening;
forming a second dielectric deck comprising a second plurality of interleaved sacrificial layers and dielectric layers on the first dielectric deck;
forming a second opening extending vertically through the second dielectric deck to expose the sacrificial layer in the first opening;
removing the sacrificial layer in the first opening;
forming a memory film on the protective dielectric layer and along sidewall of the first and second openings;
forming a third opening through the memory film and the protective dielectric layer in the lower portion of the first opening; and
forming a semiconductor channel over the memory film and in the third opening to contact the semiconductor plug.

8. The method of claim 7, wherein forming the protective dielectric layer comprises forming a native oxide layer of the semiconductor plug.

9. The method of claim 8, wherein the native oxide layer is formed by thermal oxidation.

10. The method of claim 8, wherein the native oxide layer is formed by wet chemical oxidation.

11. The method of claim 7, wherein forming the semiconductor plug comprises epitaxially growing a silicon plug from the substrate.

12. The method of claim 7, wherein a thickness of the protective dielectric layer is between about 1 nm and about 5 nm.

13. The method of claim 7, wherein the dielectric layer is not formed along the sidewall of the first opening.

14. The method of claim 7, wherein the protective dielectric layer is formed to completely cover the semiconductor plug.

15. The method of claim 7, wherein removing the sacrificial layer comprising etching the sacrificial layer until being stopped by the protective dielectric layer.

16. The method of claim 7, wherein
forming the memory film comprises subsequently depositing a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer on the sidewall of the first and second openings in this order; and

forming the semiconductor channel comprises depositing a polysilicon layer over the second silicon oxide layer and in the third opening.

17. A method for forming a three-dimensional (3D) memory device, comprising:
forming a first dielectric deck comprising a first plurality of interleaved sacrificial layers and dielectric layers on a substrate;
forming a first opening extending vertically through the first dielectric deck;
epitaxially growing a semiconductor plug from the substrate in a lower portion of the first opening;
oxidizing a top portion of the semiconductor plug to form a native oxide layer;
forming a sacrificial layer on the native oxide layer in the first opening;
forming a second dielectric deck comprising a second plurality of interleaved sacrificial layers and dielectric layers on the first dielectric deck;
forming a second opening extending vertically through the second dielectric deck to expose the sacrificial layer in the first opening; and
etching the sacrificial layer until being stopped by the native oxide layer.

18. The method of claim 17, wherein the native oxide layer is formed by thermal oxidation.

19. The method of claim 17, wherein the native oxide layer is formed by wet chemical oxidation.

20. The method of claim 17, wherein a thickness of the native oxide layer is between about 1 nm and about 5 nm.