

The invention is based on a device in accordance with the first part of claim 1. A device of this type is known from EP-A2-0 180 155.

It is known to control clocks by means of a central clock or by the information regarding the time which is radiated by a transmitter. Thus, a continuous synchronisation of a clock can be carried out, for example, by the signals received from a standard time transmitter DCF 77. It has also been suggested in an information leaflet from the Thomson Company, "Thomson Infrarot-VPV-System", that the date and time be accepted from the received video text data by issuing a command when first programming a video recorder. Thereby, the exact time and date are of course set but a continuous correction is not carried out.

The object of the invention is to accomplish a continuous synchronisation between the items of data emitted by a clock module and the items of data for the date and time received in the video text data when video text data is present.

This object is achieved in accordance with the invention by the features specified in claim 1. Further developments of the invention are characterised in the appendant claims.

When video text data is present, details regarding the time and date are transmitted in addition to the items of video text information. These details can be used in accordance with the invention for a continuous synchronisation of a clock module without any great outlay in a technical sense in consumer electronics devices which are equipped with a video text decoder. If these details are not present, i.e. at times when a video text signal is not being transmitted, or, the video text signal is subject to interference, then the signal emitted by the clock module, which, in dependence on the accuracy, may differ marginally from the actual time, is used for the display. The invention is also advantageous for the change over from summer time to winter time or vice versa since this change over occurs automatically immediately upon the reception of a video text signal.

The items of video text data are transmitted in ASCII code while the items of data for displaying in a display, which are emitted by an electronic clock module, are generally generated as items of binary data and are prepared for the display in a decoder circuit. By comparing the received items of data with those generated in the clock module in a logical comparison circuit, any deviations of the items of data from each other cause a signal to be emitted by the logical comparison circuit by virtue of which the items of data in the video text, which are converted into binary code, are transferred into the clock

module. The clock module is reset and restarted by means of these items of data. If there are large deviations due to errors in the cycle-accuracy of the items of data generated in the clock module, this process can be repeated at specific intervals, whereby the time intervals for an adjustment are kept as small as possible by the construction of the circuit so that, insofar as possible, there are no visible jumps in the display.

The invention will be explained in more detail hereinafter by way of example with the help of a Figure.

The Figure shows a video text decoder module 1 and a clock module 2 in the form of a block circuit diagram. Both modules are connected via a data bus 3, which is implemented as an I²C-Bus, to a decoding and comparator circuit 4 from which signals for the display of the date and time in a display 5 are emitted. The signals generated by the clock module 2 are entered as binary coded signals into the clock register 7 and the items of data for the time and date which are received from the video text module 1 are entered as ASCII signals into the VT data register 6 over the common I²C-Bus 3. The outputs of the data registers 6, 7 are connected to a logical comparison circuit 8. It is checked in this circuit as to whether a video text signal is present and, if there is, as to whether the received items of data for the time and the date are utilisable. If these criteria are not fulfilled, the items of data generated by the clock module 2 continue to be emitted to the display 5 via a data conversion circuit 11. If items of data from the video text signal are present and if these are the same as those from the clock module 2, then the items of data generated by the clock module 2 are likewise emitted to the display 5. Only when there are deviations of the items of data from each other is a signal for actuating a switch 9 emitted from the logical comparison circuit 8 whereby the items of video text data which are present in ASCII code and located in the register 6 supplied to the clock register 7 via a data conversion circuit 10 in which the ASCII code is converted into a binary code. These items of data are transferred from the clock register via the I²C-Bus 3 into the clock module 2. The latter is set by the items of data and restarted so that, following on this process, the corrected items of data are available both for the display 5 and in the logical comparison circuit 8 so that the switch 9 is re-opened. The process described is repeated at specific intervals if there are data deviations whereby this adjustment process is effected such as to be unremarked by someone observing the display by virtue of the construction of the circuit.

In one circuit that has been implemented, a microprocessor HMSCS 400 from the firm Hitachi was utilised for the decoding and logical comparison circuit 4, circuit arrangements SAA 5231 and SAA 5243 from the firm Valvo were utilised for the video text

decoder module 1 and a circuit arrangement PCF 8583 from the firm Valvo was utilised for the clock module 2.

A further variant of the circuit is possible if the clock module 2 is also integrated into the circuit 4 as a software clock. A solution of this type offers the advantage that the items of data do not have to be read in from the clock module since they are already present in the clock register 7. This solution may be implemented by a microprocessor HD 404709.



Claims

1. Device for correcting the time of a clock module (2), which generates signals for a display device (5) for displaying the time, by means of first items of data for the time which are received from a radio signal, wherein a comparison of the first items of data with second items of data for the time, which are generated by the clock module (2), is carried out in a comparator circuit and, when there is a deviation of the two clock times from each other, a control signal, which triggers-off a correction process, is generated by the comparator circuit, characterised in that, this device is suitable for processing radio signals transmitted as video text signals, that - when video text signals contained in the radio signal are present - a continuous comparison of first items of data for the date and the time, which are contained in the video text signals, with the second items of data, which are generated in the clock module (2), is carried out in a comparator circuit which is constructed as a logical comparison circuit (8) and that, when there is a deviation of the first and second items of data from each other, a control signal, which triggers-off a correction of the second items of data for the date and the time which are emitted by the clock module (2) by the first items of data for the date and the time which are contained in the items of video text data, is generated by the logical comparison circuit (8), that for effecting this, the first items of data for the date and the time are read into a first data register (6) over a common data bus (I²C Bus 3) from a video text decoder module (1) and the second items of data for the date and the time generated by the clock module (2) are read into a second data register (7), that the outputs of the data registers (6, 7) are connected to the logical comparison circuit (8) and that, when there is a deviation of the said items of data from each other, a signal is emitted by the logical comparison circuit (8) for actuating a switch (9) via which the items of data from the first data register (6) are supplied to the second data register (7) after a conversion in a data conversion circuit (10) whereby an adjustment of the clock module (2) to the items of data in accordance with the first data register (6) is initiated over the data bus (I²C Bus 3).
2. Device in accordance with Claim 1, characterised in that, when video text signals are not being received or if the received video text signals are incomplete, the second items of data for the date and the time, which are generated by the clock module (2), are supplied to the display device (5).



3. Device in accordance with Claim 1, characterised in that, the correction of the date and time is effected selectively, either automatically or by actuation of a key.

4. Device in accordance with Claim 1, characterised in that, when multi-lingual items of data having different clock times are present in the received video text signals, selection means are provided for selecting one clock time.

5. Circuit in accordance with any of the preceding Claims, characterised in that, the data registers (6, 7), the logical comparison circuit (8), the switch (9) and the data converting circuit (10) are comprised in an integrated circuit (4).

6. Method for correcting the time of a clock module (2), which generates signals for a display device (5) for displaying the time, by means of first items of data for the time which are received from a radio signal, wherein a comparison of the first items of data with second items of data for the time, which are generated by the clock module (2), is carried out in a comparator circuit and, when there is a deviation of the two clock times from each other, a control signal, which triggers-off a correction process, is generated by the comparator circuit, characterised in that, this method is suitable for processing radio signals transmitted as video text signals, that - when video text signals contained in the radio signal are present - a continuous comparison of first items of data for the date and the time, which are contained in the video text signals, with the second items of data, which are generated in the clock module (2), is carried out in a comparator circuit which is constructed as a logical comparison circuit (8) and that, when there is a deviation of the first and second items of data from each other, a control signal, which triggers-off a correction of the second items of data for the date and the time which are emitted by the clock module (2) by the first items of data for the date and the time which are contained in the video text signals, is generated by the logical comparison circuit (8), that for effecting this, the first items of data for the date and the time are read into a first data register (6) over a common data bus (I²C Bus 3) from a video text decoder module (1) and the second items of data for the date and the time generated by the clock module (2) are read into a second data register (7), that the outputs of the data registers (6, 7) are connected to the logical comparison circuit (8) and that, when there is a deviation of the said items of data from each other, a signal is emitted by the logical comparison circuit (8) for actuating a switch (9) via which the items of data from the first data register (6) are supplied to the second

data register (7) after a conversion in a data conversion circuit (10) whereby an adjustment of the clock module (2) to the items of data in accordance with the first data register (6) is initiated over the data bus (I²C Bus 3).

