

Description

A method and device for processing an analog signal.

Technical field.

The present invention according to a first aspect relates to a device for processing an analog input signal varying widely in amplitude, such as speech, and having a first ratio of maximum to minimum amplitude variations, comprising means for reducing said first ratio into a second ratio being the square root of said first ratio, and for delivering an analog output signal having said second ratio.

Also according to the first aspect the invention furthermore relates to a method for processing an analog input signal varying widely in amplitude, such as speech, and having a first ratio of maximum to minimum amplitude variations, comprising the steps of reducing said first ratio into a second ratio being the square root of said first ratio, and delivering an analog output signal having said second ratio.

More particularly, said processing aims at reducing the ratio of maximum to minimum amplitude variations at the output of the processing to the square root of the ratio existing before processing in order better to transmit said signal through a channel of restricted dynamic range in the presence of additive noise.

According to a second aspect the invention also relates to a device and a method for processing an input signal having a compressed amplitude range in order to produce an output signal having an amplitude range being the square of the compressed range. More particularly, said input signal can be one as produced as the output signal in accordance with the first aspect.

State of the art.

The quality of voice transmission over a communications network that suffers from transmission noise, such as exemplified by a radio link, may be described and measured in terms of signal-to-noise ratio (SNR). Because a real voice signal is not of constant amplitude, but varies more or less randomly over a wide dynamic range, it is not a convenient test signal with which to carry out SNR measurements. Instead, constant-level tones of various frequencies in the audio range are usually employed for this purpose, and the resulting measurement is called TTNR (Test Tone to Noise Ratio).

The subjectively perceived quality of speech is, however, better described by the ratio of peak speech loudness to noise during silence periods, a measure which is not described by TTNR. A better measure of subjective quality would be the ratio of the switched

on test tone level to residual noise with the test tone switched off. It is in order to optimise this more subjectively important quality aspect a technique known as companding is often employed.

Companding comprises a variable gain control at the transmit end arranged either to increase the transmitted level during quiet periods and/or to reduce the level during loud periods, so that the total dynamic range of the signal is compressed/companded towards a mean. At the receive end, a decompander or expander performs the inverse scaling, increasing the level during loud periods to restore the original dynamic signal excursion and likewise decreasing the level during quiet periods. In the latter case, any noise added in transmission is also reduced during the quiet periods, exactly as required to maximise the perceived quality.

A commonly used companding law is the so-called square-root law, in which the amplitude of the signal actually transmitted is proportional to the square-root of the amplitude at source. For example, during a period in which the speech source material momentarily had an amplitude of 1/100th of a unit the transmitted amplitude would be raised to 1/10th by the compander. Likewise, during a period of source amplitude 9 units, the transmitted amplitude would be reduced to 3 units, while unit amplitude by definition is that level which remains unchanged through the compander. Suppose now that the noise added in transmission corresponds to 1/100th of an amplitude unit. In the quiet period when 1/10th was transmitted, the received signal would consist of 1/10th of a unit of wanted signal plus 1/100th of a unit of noise. Upon the decompander reducing the 1/10th unit signal to its original 1/100th unit, the noise would be reduced by the same factor from 1/100th to 1/1000th. In the case of a zero level wanted signal, the compander would interpret the 1/100th unit received noise as a companded signal level, and restore it to what it believed the original signal level to have been, namely 1/10000th.

It can be seen therefore that the noise level during silence periods at the output of the decompander is the square of the value it otherwise would have been without the use of companding and decompanding.

SNR is often measured on the logarithmic scale of decibels, defined by

$$\text{dBs} = 20 \text{LOG} (\text{SIGNAL AMPLITUDE} / \text{NOISE AMPLITUDE})$$

If the mean signal amplitude during active speech is taken to be 1, and the noise amplitude in silence periods is equal to 1/100 without companding, then the SNR calculated by the above formula is 40dB.

With companding/decompanding, the noise in silence periods is reduced to 1/10000, giving an SNR of 80dB, a considerable improvement in subjective

quality.

In two prior methods for performing square-root companding, known as the feedforward and feedback methods, respectively, a respective companded output signal is obtained by dividing the input signal by a value obtained, in the feed forward case, through amplitude measurement, smoothing and square root processing of the input signal, and, in the feed back case, through amplitude measurement and smoothing of the companded output signal, respectively.

The feedback method has the advantage that the square-root function is not explicitly needed, and also that the amplitude measurement takes place on the companded output, halving the signal range in dBs that the measuring device need handle. The square root companding law arises because the output amplitude is the input amplitude divided by the output amplitude.

Two known implementations of a compander of the latter type exist. The first one is a fully analog circuit implementation in which the dividing circuit would most probably be implemented by using an analog multiplier in a feedback loop. The second one is a fully digital implementation in which the input signal is first digitised using an analog-to-digital converter, then fed into a digital signal processing circuit which would numerically implement a companding algorithm of either the feedback or feedforward variety. The result must then be converted back to an analog signal again using a digital-to-analog convertor.

The known implementations each have their own drawbacks. The drawback of the fully analog system is that some tight tolerance components are needed, which are difficult to fabricate in semiconductor integrated circuits. The drawback of the fully digital implementation is the need for quite complex A-to-D and D-to-A converters, plus a costly and power-consuming digital signal processor chip.

The invention.

It is an object of the present invention to provide a new way to implement square-root law companding which has the advantage of being more easily integrated into low-cost silicon integrated circuits using low-cost semiconductor processes. This object has been attained as follows by means of the devices and methods according to the first and second aspects of the invention:

The device according to the first aspect of the invention comprises

an analog-to-digital converter for changing said input signal into a stream of integer numbers representing in a proportional way the instantaneous value of the input signal divided by a first reference voltage,

means for generating said first reference voltage in proportion to the amplitude of said output sig-

nal,

a digital-to-analog converter for reconvertng said stream of numbers to an analog signal waveform in proportion to a constant reference voltage, said analog wave form forming said output signal.

The method according to the first aspect of the invention comprises the steps of

changing said input signal into a stream of integer numbers representing in a proportional way the instantaneous value of the input signal divided by a first reference voltage generated in proportion to the amplitude of said output signal,

reconvertng said stream of numbers to an analog signal waveform in proportion to a constant reference voltage, said analog wave form forming said output signal.

The device according to the second aspect of the invention comprises

an analog-to-digital converter having means for changing said input signal into a sequence of integer numbers, said sequence in a proportional way representing said input signal,

a digital-to-analog converter for converting back said sequence of numbers to an analog signal forming said output signal, said converter having means for scaling said output signal in proportion to a reference voltage,

means for deriving said reference voltage in response to the amplitude of said input signal.

The method according to the second aspect of the invention comprises the steps of

changing said input signal into a sequence of integer numbers, said sequence in a proportional way representing said input signal,

converting back said sequence of numbers to an analog signal forming said output signal, while scaling said output signal in proportion to a reference voltage derived in response to the amplitude of said input signal.

Description of the drawings.

Embodiments of the invention will now be described more closely below with reference to the accompanying schematical drawings, on which,

Figures 1 and 2 are generic block diagrams of two aspects of the present invention,

Figures 3-8 schematically illustrate different circuit solutions for the blocks included in Figures 1 and 2, and more particularly,

Figures 3 and 4 illustrate a Delta modulation encoder and decoder, respectively,

Figures 5 and 6 illustrate a Delta-Sigma or Sigma-Delta encoder and decoder, respectively,

Figure 7 illustrates companding by use of variable stepsize Delta or Delta-Sigma modulation, and

Figure 8 illustrates decompanding by encoding

with constant stepsize and decoding with variable stepsize.

Preferred embodiments.

Figure 1 in block diagram form illustrates a device for processing an analog input signal S which varies widely in amplitude, such as speech. The purpose of this device is to reduce the ratio of maximum to minimum amplitude variations of an output signal P, after the processing, to the square root of the ratio existing before processing in order better to transmit said signal through a channel of restricted dynamic range in the presence of additive noise.

The device comprises an analog-to-digital converter 2 arranged to change, as will be described more closely below, the signal S into a stream of integer numbers $N_1, N_2, N_3, \dots$. These numbers may in the limit consist of only two possible values, such as plus one and minus one. The numbers in the stream represent in some proportional way the instantaneous value of the input signal S divided by a reference voltage R. This reference voltage R is generated by a smoothed amplitude measuring device 4 in proportion to the amplitude of the output signal P that is produced, in a manner to be described more closely below, when the number stream is reconverted to an analog signal waveform by means of an digital-to-analog converter 6 working with a constant reference voltage.

Figure 2 schematically illustrates a device, complementary to that of Figure 1, for processing a signal U of compressed amplitude variation, such as might be produced by the device of Figure 1. The purpose of the device of Figure 2 is to produce a signal V of amplitude variation restored to the normal range, being the square of the compressed range.

The device comprises an analog-to-digital converter 8 that turns said compressed input signal U into a sequence of integer numbers $M_1, M_2, M_3, \dots$. These numbers may in the limit be restricted to only two possible values, such as plus one and minus one. The sequence in a proportional way represents the signal U, and is converted back to an analog signal V by means of a digital-to-analog converter 10. The converter 10 scales the output signal V in proportion to a reference voltage Q derived by determining the amplitude of input signal U with a measuring device 12, which may include smoothing of the measurement by means of a low-pass filter.

According to one important embodiment of the present invention the technique used for converters 2, 6, 8 and 10 may be of the type known as Delta modulation, Delta-Sigma modulation or one of their variants.

A Delta modulation encoder digitizes an analog signal into a sequence of 1-bit binary numbers, representing +1 or -1. The values are used to change the

direction of a ramp generator, or integrator, so that it ramps up if the previous value was lower than the input signal, or ramps down if the previous value was too high. The amount the integrator ramps up or down between samples is called the step size. If the 1-bit samples are generated at a high rate, the steps needed to follow a signal changing at a given rate will be smaller, and the step approximation to the signal waveform will thus be more accurate. The coarseness of 1-bit quantization may thus be compensated by raising the sample bit-rate sufficiently to obtain the desired accuracy.

Figure 3 shows an integrator 14, the output signal of which is compared with the input signal S in a comparator 16. The decision D is taken at a certain bit rate F_b by clocking into a latch or flip-flop 18 upon positive going edges of a clock of frequency F_b . The clocked decision is then fed to a switch 20 to effect selection of the direction in which the integrator 14 will change during the next sample period. The magnitude of the change is determined by the value STEPSIZE.

In another known system, the value of STEPSIZE is increased whenever the integrator is ramped in the same direction three times in succession, an event which hints that the rate of change of signal is greater than the integrator can follow with the present STEPSIZE. This known system is called "companded Delta modulation" and also CVSD (Continuously Variable Slope Delta).

With reference to Figure 4, Delta modulation is reconstructed to an analog signal by feeding it to an integrator 22 similar to that employed in the encoder. A difference between the encoder integrator 14 and the reconstruction integrator 22 is that the latter must include some form of leakage, e.g. a resistor 24 connected across the integration capacitor 26, to define the arbitrary constant of integration to be zero (i.e. to cause the arbitrary start-up charge state to decay with time).

After reconstruction by a leaky integrator, high frequency quantization noise may be further reduced by a low pass filter which passes the highest likely signal frequencies, but which attenuates noise frequencies in the region of the sample bit-rate and higher.

The use of a related algorithm known as Sigma-Delta or Delta-Sigma modulation is illustrated in Figures 5 and 6. The difference is that the input signal S is applied before the integrator, here designated 22', instead of afterwards. The signal suffers an extra integration in the encoder compared to Delta modulation, which is then removed at the decoder shown in Figure 6 by omitting the reconstruction integrator 22, and using only low-pass filtering at 28'. Delta-Sigma modulation represents values between + and - STEPSIZE by alternating between them in the correct mean ratio, and in this respect is similar to pulse width modulation.

Delta or Delta-Sigma modulation schemes may also include more than one integrator or other frequency response shaping in the feedback loop, and the signal may or may not pass through one or more of these components. It is also possible to construct Delta modulation encoders and decoders in which the error between the integrator value and the input signal value is quantized to more than one bit, and is then known as delta-PCM.

The design details of all such variants need not be described here since they may be found in the technical literature. Any scheme characterised by an encoder which digitizes the input signal with a scaling determined by the value of STEPSIZE or similar reference voltage, which can be allowed to vary in response to the signal, and which digitized signal may readily be converted back to an analog signal using either the same or different, constant or variable stepsize or reference voltage may be suitable for the implementation of the invention.

Both variable and constant stepsize can be used with the invention. If the signal is encoded using a small stepsize and decoded using a large stepsize, its amplitude will have been increased. If the encoding stepsize is larger than the decoding stepsize, the amplitude will be reduced. If therefore the encoding stepsize is varied while the decode stepsize is kept constant, the signal level output will bear an inverse relationship to the stepsize, thus realising a divide function, as required by the square-root compandor.

It is only necessary therefore to make the stepsize proportional to the companded output signal amplitude by deriving it from an amplitude measurement as shown in figure 7.

Figure 7 shows by way of example an encoder 30 of Delta or Delta-Sigma type and of 1-bit quantization. The constant-stepsize decoder is then simply a low-pass filter 32. The variable stepsize for the encoder is derived by measuring at 34 the amplitude of the companded signal reconstructed into analog form by the low-pass filter. The amplitude measurement is subject to a further low-pass filtering operation, or smoothing time constant at 36, called the companding time constant. This is defined in various international standards that employ companding for voice transmission.

The corresponding decompanding circuit is shown in figure 8. In this case, the companded input signal is encoded at 38 with constant step size to return it to digital form, then decoded at 40 back to analog form but using variable stepsize proportional to the smoothed input amplitude. For correct system performance, the low-pass filter or time constant used at 42 to smooth the amplitude measurement at 44 in the decompandor should be identical to that used in the compandor.

Claims

1. A device for processing an analog input signal (S) varying widely in amplitude, such as speech, and having a first ratio of maximum to minimum amplitude variations, comprising means for reducing said first ratio into a second ratio being the square root of said first ratio, and for delivering an analog output signal (P) having said second ratio, characterized by
 - an analog-to-digital converter (2) for changing said input signal into a stream of integer numbers (N1,N2,...) representing in a proportional way the instantaneous value of the input signal (S) divided by a first reference voltage (R),
 - means (4) for generating said first reference voltage in proportion to the amplitude of said output signal (P),
 - a digital-to-analog converter (6) for reconverting said stream of numbers to an analog signal waveform in proportion to a constant reference voltage, said analog wave form forming said output signal (P).
2. A device according to claim 1, characterized in that said integer numbers consist of only two possible values such as plus one and minus one.
3. A device according to claim 1 or 2, characterized in that said first reference voltage (R) is generated by a smoothed amplitude measuring device (4).
4. A device according to any of claims 1-3, characterized in that said analog-to-digital convertor (2) comprises an encoder (14-20; 30) working in accordance with a technique known as Delta modulation, Delta-Sigma modulation or variants thereof, said encoder having
 - means for quantizing said input signal (S) to only one binary bit resolution,
 - means for obtaining a desired accuracy by increasing the sample rate or bit rate,
 - means (20) for determining the stepsize of said encoder in response to said first reference voltage,
 - said digital-to-analog converter (6) having a decoder for the quantized signal operated with constant step size.
5. A device for processing an input signal (U) having a compressed amplitude range in order to produce an output signal (V) having an amplitude range being the square of the compressed range, characterized by
 - an analog-to-digital converter (8) having means for changing said input signal into a sequence of integer numbers (M1,M2...), said se-



Delta or Delta-Sigma modulation schemes may also include more than one integrator or other frequency response shaping in the feedback loop, and the signal may or may not pass through one or more of these components. It is also possible to construct Delta modulation encoders and decoders in which the error between the integrator value and the input signal value is quantized to more than one bit, and is then known as delta-PCM.

The design details of all such variants need not be described here since they may be found in the technical literature. Any scheme characterised by an encoder which digitizes the input signal with a scaling determined by the value of STEPSIZE or similar reference voltage, which can be allowed to vary in response to the signal, and which digitized signal may readily be converted back to an analog signal using either the same or different, constant or variable stepsize or reference voltage may be suitable for the implementation of the invention.

Both variable and constant stepsize can be used with the invention. If the signal is encoded using a small stepsize and decoded using a large stepsize, its amplitude will have been increased. If the encoding stepsize is larger than the decoding stepsize, the amplitude will be reduced. If therefore the encoding stepsize is varied while the decode stepsize is kept constant, the signal level output will bear an inverse relationship to the stepsize, thus realising a divide function, as required by the square-root compandor.

It is only necessary therefore to make the stepsize proportional to the companded output signal amplitude by deriving it from an amplitude measurement as shown in figure 7.

Figure 7 shows by way of example an encoder 30 of Delta or Delta-Sigma type and of 1-bit quantization. The constant-stepsize decoder is then simply a low-pass filter 32. The variable stepsize for the encoder is derived by measuring at 34 the amplitude of the companded signal reconstructed into analog form by the low-pass filter. The amplitude measurement is subject to a further low-pass filtering operation, or smoothing time constant at 36, called the companding time constant. This is defined in various international standards that employ companding for voice transmission.

The corresponding decompanding circuit is shown in figure 8. In this case, the companded input signal is encoded at 38 with constant step size to return it to digital form, then decoded at 40 back to analog form but using variable stepsize proportional to the smoothed input amplitude. For correct system performance, the low-pass filter or time constant used at 42 to smooth the amplitude measurement at 44 in the decompandor should be identical to that used in the compandor.

Claims

1. A device for processing an analog input signal (S) varying widely in amplitude, such as speech, and having a first ratio of maximum to minimum amplitude variations, comprising means for reducing said first ratio into a second ratio being the square root of said first ratio, and for delivering an analog output signal (P) having said second ratio, characterized by
 - an analog-to-digital converter (2) for changing said input signal into a stream of integer numbers (N1,N2,...) representing in a proportional way the instantaneous value of the input signal (S) divided by a first reference voltage (R),
 - means (4) for generating said first reference voltage in proportion to the amplitude of said output signal (P),
 - a digital-to-analog converter (6) for re-converting said stream of numbers to an analog signal waveform in proportion to a constant reference voltage, said analog wave form forming said output signal (P).
2. A device according to claim 1, characterized in that said integer numbers consist of only two possible values such as plus one and minus one.
3. A device according to claim 1 or 2, characterized in that said first reference voltage (R) is generated by a smoothed amplitude measuring device (4).
4. A device according to any of claims 1-3, characterized in that said analog-to-digital convertor (2) comprises an encoder (14-20; 30) working in accordance with a technique known as Delta modulation, Delta-Sigma modulation or variants thereof, said encoder having
 - means for quantizing said input signal (S) to only one binary bit resolution,
 - means for obtaining a desired accuracy by increasing the sample rate or bit rate,
 - means (20) for determining the stepsize of said encoder in response to said first reference voltage,
 - said digital-to-analog converter (6) having a decoder for the quantized signal operated with constant step size.
5. A device for processing an input signal (U) having a compressed amplitude range in order to produce an output signal (V) having an amplitude range being the square of the compressed range, characterized by
 - an analog-to-digital converter (8) having means for changing said input signal into a sequence of integer numbers (M1,M2...), said se-



quence in a proportional way representing said input signal,

a digital-to-analog converter (10) for converting back said sequence of numbers to an analog signal forming said output signal (V), said converter having means for scaling said output signal in proportion to a reference voltage (Q),

means for deriving said reference voltage in response to the amplitude of said input signal.

6. A device according to claim 5, characterized in that said sequence of integer numbers is restricted to only two possible values such as plus one and minus one.

7. A device according to claim 5 or 6, characterized in that the amplitude of said input signal is determined with a measuring device (12) including a low pass filter for smoothing the measurement.

8. A device according to any of claims 5-7, characterised in that said analog-to-digital converter (8) and said digital-to-analog converter (10) comprise an encoder and a decoder, respectively, working in accordance with a technique known as Delta modulation, Delta-Sigma modulation or variants thereof, said encoder having means for producing said output number sequence as containing single-bit binary numbers representing only two possible values, and in a proportional way representing the instantaneous value of said input signal (U),

means for compensating the coarse two-level quantization thereby obtained by increasing the sample conversion rate or bitrate to obtain a desired accuracy,

said decoder being designed to accept the same output bitstream as produced by the encoder and to convert it back to an analog signal waveform, and having means for producing said output signal by scaling said analog waveform in proportion to said reference signal by using the latter to determine the step size of said decoder.

9. A method for processing an analog input signal varying widely in amplitude, such as speech, and having a first ratio of maximum to minimum amplitude variations, comprising reducing said first ratio into a second ratio being the square root of said first ratio, and delivering an analog output signal having said second ratio, characterized by changing said input signal into a stream of integer numbers representing in a proportional way the instantaneous value of the input signal divided by a first reference voltage generated in proportion to the amplitude of said output signal, reconvertng said stream of numbers to an analog signal waveform in proportion to a con-

stant reference voltage, said analog wave form forming said output signal.

10. A method according to claim 9, characterized in that said integer numbers consist of only two possible values such as plus one and minus one.

11. A method for processing an input signal having a compressed amplitude range in order to produce an output signal having an amplitude range being the square of the compressed range, characterized by

changing said input signal into a sequence of integer numbers, said sequence in a proportional way representing said input signal, converting back said sequence of numbers to an analog signal forming said output signal, while scaling said output signal in proportion to a reference voltage derived in response to the amplitude of said input signal.

12. A method according to claim 12, characterized in that said sequence of integer numbers is restricted to only two possible values such as plus one and minus one.

Revendications

1. Un dispositif pour traiter un signal d'entrée analogique (S) dont l'amplitude varie considérablement, tel que de la parole, et ayant un premier rapport de variation entre l'amplitude maximale et l'amplitude minimale, comprenant des moyens pour réduire ce premier rapport à un second rapport qui est la racine carrée du premier rapport, et pour fournir un signal de sortie analogique (P) ayant le second rapport, caractérisé par un convertisseur analogique-numérique (2) pour transformer le signal d'entrée en un train de nombres entiers (N1, N2, ...) représentant d'une manière proportionnelle la valeur instantanée du signal d'entrée (S) divisée par une première tension de référence (R), des moyens (4) pour générer la première tension de référence en proportion de l'amplitude du signal de sortie (P), un convertisseur numérique-analogique (6) pour reconvertir le train de nombres en une forme d'onde de signal analogique en proportion d'une tension de référence constante, cette forme d'onde analogique formant le signal de sortie (P).
2. Un dispositif selon la revendication 1, caractérisé en ce que les nombres entiers comprennent seulement deux valeurs possibles telles que plus un et moins un.



3. Un dispositif selon la revendication 1 ou 2, caractérisé en ce que la première tension de référence (R) est générée par un dispositif de mesure d'amplitude lissée (4).
4. Un dispositif selon l'une quelconque des revendications 1-3, caractérisé en ce que le convertisseur analogique-numérique (2) comprend un codeur (14-20 ; 30) qui travaille conformément à une technique appelée modulation Delta ou modulation Delta-Sigma ou des variantes de celles-ci, ce codeur comprenant
 - des moyens pour quantifier le signal d'entrée (S) avec une résolution d'un seul bit,
 - des moyens pour obtenir une précision désirée par l'augmentation de la cadence d'échantillonnage ou du débit binaire,
 - des moyens (20) pour déterminer la taille de pas du codeur sous la dépendance de la première tension de référence, le convertisseur numérique-analogique (6) comportant un décodeur pour le signal quantifié qui travaille avec une taille de pas constante.
5. Un dispositif pour traiter un signal d'entrée (U) ayant une plage d'amplitude comprimée, dans le but de produire un signal de sortie (V) ayant une plage d'amplitude qui est le carré de la plage comprimée, caractérisé par
 - un convertisseur analogique-numérique (8) comportant des moyens pour transformer le signal d'entrée en une séquence de nombres entiers (M1, M2, ...), cette séquence représentant d'une manière proportionnelle le signal d'entrée,
 - un convertisseur numérique-analogique (10) pour reconvertir la séquence de nombres en un signal analogique qui forme le signal de sortie (V), ce convertisseur comportant des moyens pour multiplier le signal de sortie par un facteur en proportion d'une tension de référence (Q),
 - des moyens pour élaborer la tension de référence sous la dépendance de l'amplitude du signal d'entrée.
6. Un dispositif selon la revendication 5, caractérisé en ce que la séquence de nombres entiers est restreinte à seulement deux valeurs possibles, telles que plus un et moins un.
7. Un dispositif selon la revendication 5 ou 6, caractérisé en ce que l'amplitude du signal d'entrée est déterminée avec un dispositif de mesure (12) qui comprend un filtre passe-bas pour lisser la mesure.
8. Un dispositif selon l'une quelconque des revendications 5-7, caractérisé en ce que le convertisseur analogique-numérique (8) et le convertis-

seur numérique-analogique (10) comprennent respectivement un codeur et un décodeur, travaillant conformément à une technique appelée modulation Delta ou modulation Delta-Sigma ou des variantes de celles-ci, ce codeur comportant

des moyens pour produire la séquence de nombres de sortie sous une forme contenant des nombres binaires à un seul bit représentant seulement deux valeurs possibles, et représentant d'une manière proportionnelle la valeur instantanée du signal d'entrée (U),

des moyens pour compenser la quantification grossière à deux niveaux qui est ainsi obtenue, en augmentant la cadence de conversion d'échantillons ou le débit binaire, pour obtenir une précision désirée,

le décodeur étant conçu pour accepter le train de bits de sortie qui est produit par le codeur et pour le reconvertir en une forme d'onde de signal analogique, et comportant des moyens pour produire le signal de sortie en multipliant la forme d'onde analogique par un facteur en proportion du signal de référence, en utilisant ce dernier pour déterminer la taille de pas du décodeur.

9. Un procédé pour traiter un signal d'entrée analogique dont l'amplitude varie fortement, tel que de la parole, et ayant un premier rapport de variation entre l'amplitude maximale et l'amplitude minimale, comprenant la réduction du premier rapport à un second rapport qui est la racine carrée du premier rapport, et la fourniture d'un signal de sortie analogique ayant le second rapport, caractérisé en ce que

on transforme le signal d'entrée en un train de nombres entiers représentant d'une manière proportionnelle la valeur instantanée du signal d'entrée divisée par une première tension de référence qui est générée en proportion de l'amplitude du signal de sortie,

on reconvertit ce train de nombres en une forme d'onde de signal analogique en proportion d'une tension de référence constante, cette forme d'onde analogique formant le signal de sortie.

10. Un procédé selon la revendication 9, caractérisé en ce que les nombres entiers comprennent seulement deux valeurs possibles telles que plus un et moins un.

11. Un procédé de traitement d'un signal d'entrée ayant une plage d'amplitude comprimée, dans le but de produire un signal de sortie ayant une plage d'amplitude qui est le carré de la plage comprimée, caractérisé en ce que

on transforme le signal d'entrée en une séquence de nombres entiers, cette séquence représentant d'une manière proportionnelle le si-



gnal d'entrée,

on reconvertit la séquence de nombres en un signal analogique formant le signal de sortie, tout en multipliant le signal de sortie par un facteur en proportion d'une tension de référence qui est obtenue sous la dépendance de l'amplitude du signal d'entrée.

12. Un procédé selon la revendication 11, caractérisé en ce que la séquence de nombres entiers est restreinte à seulement deux valeurs possibles, telles que plus un et moins un.

Patentansprüche

1. Schaltungsanordnung zur Behandlung eines analogen Eingangssignals (S), das eine grosse Amplitudenschwankung aufweist, wie bei Sprache, und ein erstes Verhältnis zwischen maximaler und minimaler Amplitude aufweist, mit Mitteln zur Verringerung dieses genannten ersten Verhältnisses in ein zweites Verhältnis, das der Quadratwurzel des ersten Verhältnisses entspricht, und zur Abgabe eines analogen Ausgangssignals (P), das das zweite Verhältnis aufweist, gekennzeichnet durch

einen analog-digital Wandler (2), um das genannte Eingangssignal in einen Strom ganzer Zahlen (N1, N2,...) umzuwandeln, die in proportionaler Art den momentanen Wert des Eingangssignals (S) geteilt durch eine erste Referenzspannung (R) darstellen,

Mittel (4) zur Erzeugung der genannten ersten Referenzspannung, die proportional zur Amplitude des genannten Ausgangssignals (P) ist,

einen digital-analog Wandler (6) zur Rückumwandlung des genannten Stromes von Zahlen in ein Analogsignal, das proportional zu einer konstanten Referenzspannung ist, welches Analogsignal das Ausgangssignal (P) ist.

2. Schaltungsanordnung nach Anspruch 1, dadurch gekennzeichnet, dass die genannten ganzen Zahlen aus nur zwei möglichen Werten bestehen, wie einen positiven und einen negativen Wert.
3. Schaltungsanordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, dass zur Erzeugung der genannten ersten Referenzspannung (R) eine glättende Amplitudenmessvorrichtung vorhanden ist.
4. Schaltungsanordnung nach einem der Ansprüche 1 - 3, dadurch gekennzeichnet, dass der analog-digital Wandler (2) einen Codierer (14-

20;30) umfasst, der mit Delta-Modulation, Delta-Sigma Modulation oder Varianten davon arbeitet, und

Mittel zur Quantisierung des genannten Eingangssignals (S) mit einer Auflösung mit nur einem binären Bit,

Mittel zur Erhaltung einer gewünschten Genauigkeit durch Erhöhung der Abtastfrequenz oder der Anzahl Bits,

Mittel (20) zur Bestimmung der Schrittgrösse des genannten Codierers in Abhängigkeit zu der genannten ersten Referenzspannung umfasst,

und welcher digital-analog Wandler (6) einen Decodierer für das quantisierte Signal mit konstanter Schrittgrösse umfasst.

5. Schaltungsanordnung zur Verarbeitung eines Eingangssignals (U) mit einem komprimierten Amplitudenbereich, zwecks Erzeugung eines Ausgangssignals (V) mit einem Amplitudenbereich, der das Quadrat des komprimierten Bereichs ist, gekennzeichnet durch

einen analog-digital Wandler (8) mit Mitteln zur Änderung des Eingangssignals in eine Sequenz ganzer Zahlen (M1, M2,...), welche Sequenz das genannte Eingangssignal in proportionaler Art darstellt,

einen digital-analog Wandler (10) zur Rückumformung der genannten Zahlensequenz in ein das Ausgangssignal (V) bildendes Analogsignal, welcher Wandler Mittel zur Skalierung des Ausgangssignals proportional zu einer Referenzspannung (Q) umfasst,

Mittel zur Erzeugung der Referenzspannung in Abhängigkeit von der Amplitude des genannten Eingangssignals.

6. Schaltungsanordnung nach Anspruch 5, dadurch gekennzeichnet, dass die Sequenz ganzer Zahlen auf nur zwei mögliche Werte begrenzt ist wie ein positiver und ein negativer Wert.
7. Schaltungsanordnung nach Anspruch 5 oder 6, dadurch gekennzeichnet, dass die Amplitude des genannten Eingangssignals mittels einer ein Tiefpassfilter zur Glättung der Messung umfassenden Messvorrichtung (12) bestimmt ist.
8. Schaltungsanordnung nach einem der Ansprüche 5-7, dadurch gekennzeichnet, dass der analog-digital Wandler (8) und der digitalanalog Wandler (10) je einen Codierer und einen Decodierer umfassen, die nach Delta-Modulation, Delta-Sigma-Modulation oder Varianten davon arbeiten, wobei der Codierer

Mittel zur Erzeugung der abgegebenen Folge von Zahlen in Form von binären Zahlen mit



einem Bit das nur zwei mögliche Werte darstellt, und in proportionaler Weise den momentanen Wert des Eingangssignals (u) darstellt,

und Mittel zur Kompensation der groben Quantisierung mit zwei Pegeln um dadurch die Umwandlungsrate der Abtastung oder der Bitrate zwecks Erhaltens der gewünschten Genauigkeit zu erhöhen, umfasst,

welcher Decodierer dazu ausgebildet ist, um denselben Bitstrom anzunehmen, wie er vom Codierer erzeugt wurde und um diesen in ein Signal in analoger Form umzuwandeln, und der weiter Mittel aufweist, zur Erzeugung des genannten Ausgangssignals durch skalieren des analogen Signals proportional zu der genannten Referenzspannung durch Verwendung der letzteren zwecks Bestimmung der Schrittgrösse des Decodierers.

9. Verfahren zur Verarbeitung eines analogen Eingangssignals, das grosse Amplitudenunterschiede aufweist, wie bei der Sprache, und ein erstes Verhältnis zwischen maximaler und minimaler Amplitude aufweist, umfassend die Reduktion des ersten Verhältnisses in ein zweites Verhältnis, das die Quadratwurzel des ersten Verhältnisses ist und zur Abgabe eines Analogausgangssignals mit dem zweiten Verhältnis, gekennzeichnet durch

Umwandeln des Eingangssignals in einen Strom ganzer Zahlen, die in proportionaler Weise den momentanen Wert des Eingangssignals geteilt durch eine erste Referenzspannung, die proportional zur Amplitude des genannten Ausgangssignals ist, darstellt,

Rückumwandeln der Folge von Zahlen proportional zu einer konstanten Referenzspannung in ein analoges Signal, das das Ausgangssignal bildet.

10. Verfahren nach Anspruch 9, dadurch gekennzeichnet, dass die ganzen Zahlen aus zwei möglichen Werten, einem positiven und einem negativen, bestehen.

11. Verfahren zur Verarbeitung eines Eingangssignals mit komprimiertem Amplitudenbereich zwecks Erzeugung eines Ausgangssignals mit einem Amplitudenbereich, der das Quadrat des komprimierten Bereichs ist, gekennzeichnet durch Ändern des Eingangssignals in eine Folge von ganzen Zahlen, die in proportionaler Art das Eingangssignal darstellen.

Rückumwandeln der Folge von Zahlen in ein, das Ausgangssignal darstellendes Analogsignal, während das Ausgangssignal proportional zu einer in Abhängigkeit von der Amplitude des Eingangssignals abgeleiteten Referenzspannung

skaliert wird.

12. Verfahren nach Anspruch 12, dadurch gekennzeichnet, dass die Folge der ganzen Zahlen auf nur zwei mögliche Werte eingeschränkt ist, wie einen positiven und einen negativen Wert.