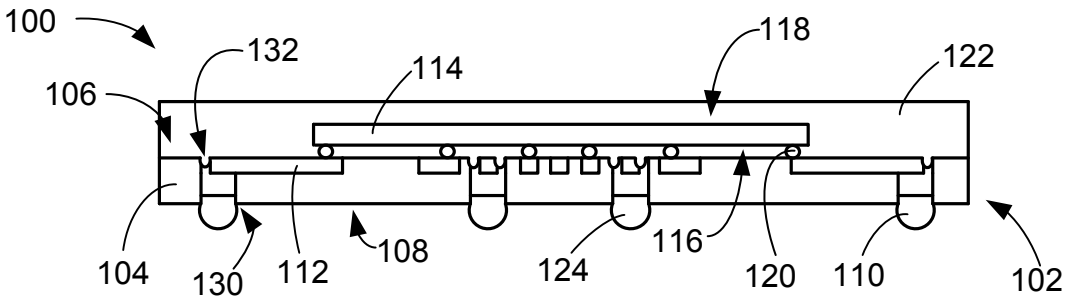


FIG. 1

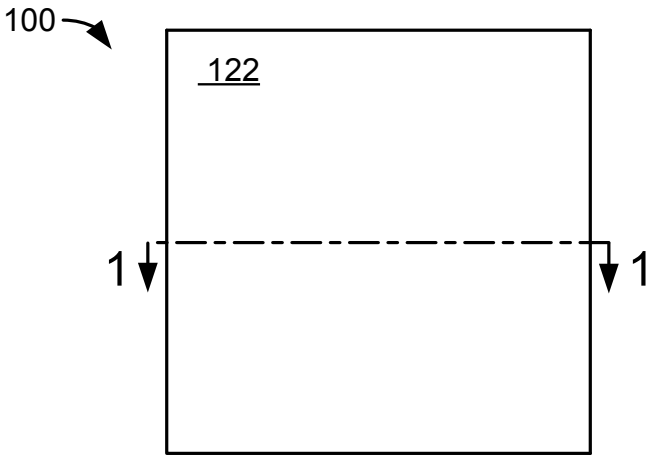


FIG. 2

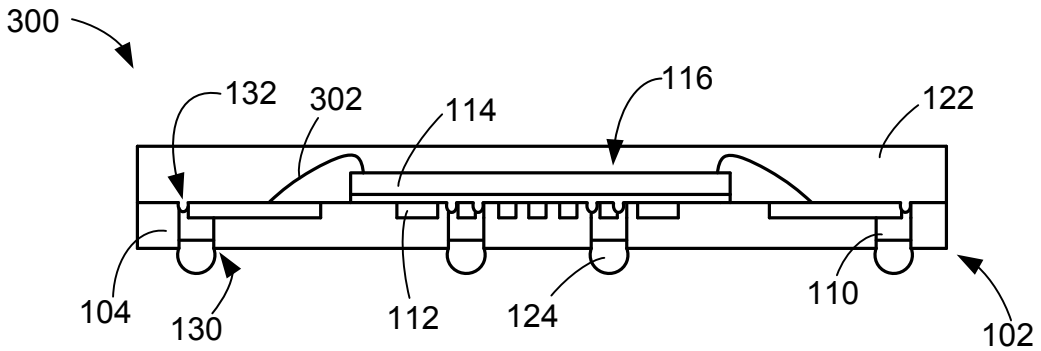


FIG. 3

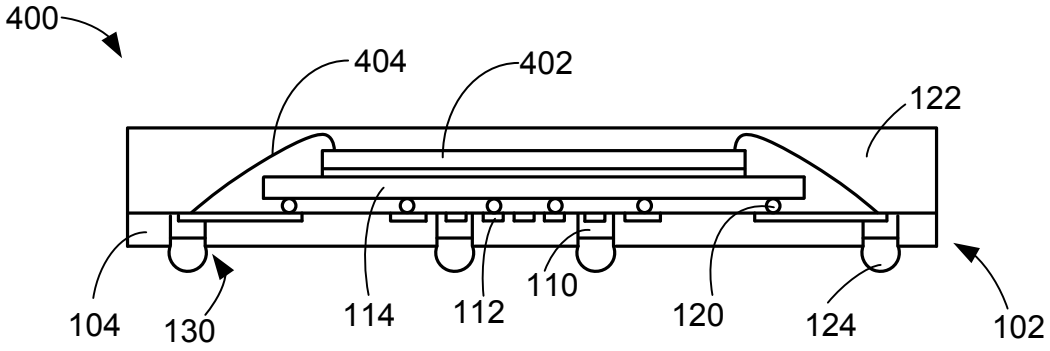


FIG. 4

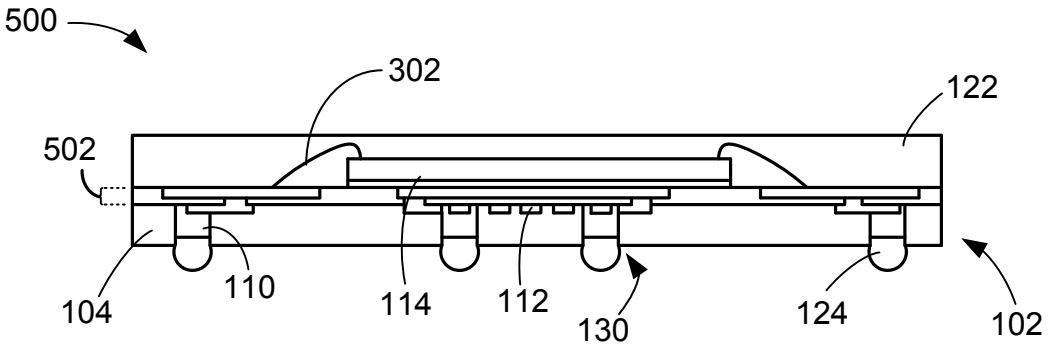


FIG. 5

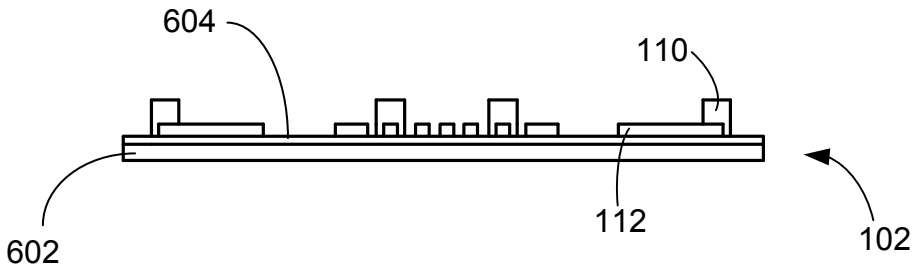


FIG. 6

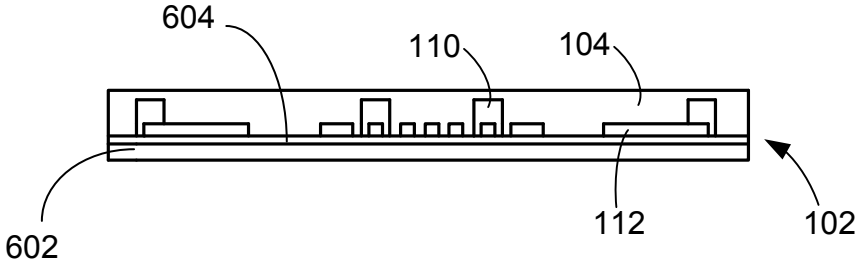


FIG. 7

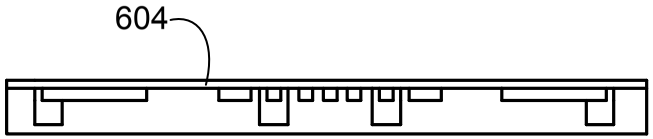


FIG. 8

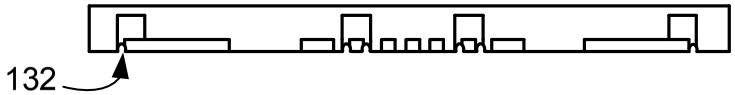


FIG. 9

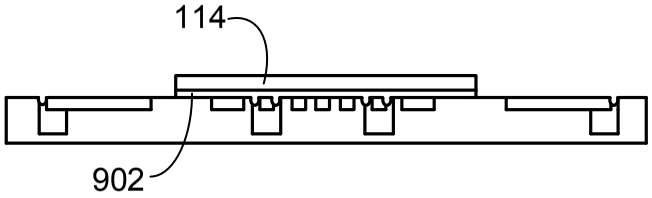


FIG. 10

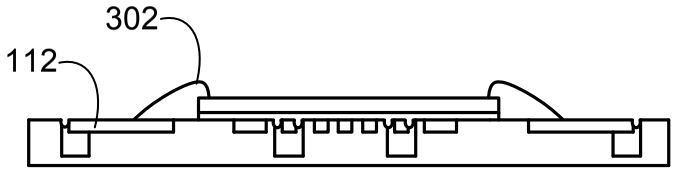


FIG. 11

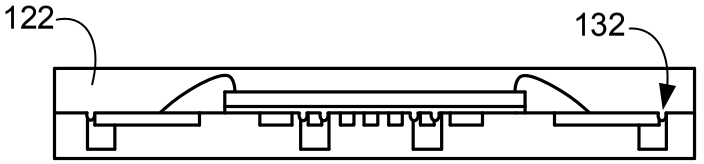


FIG. 12

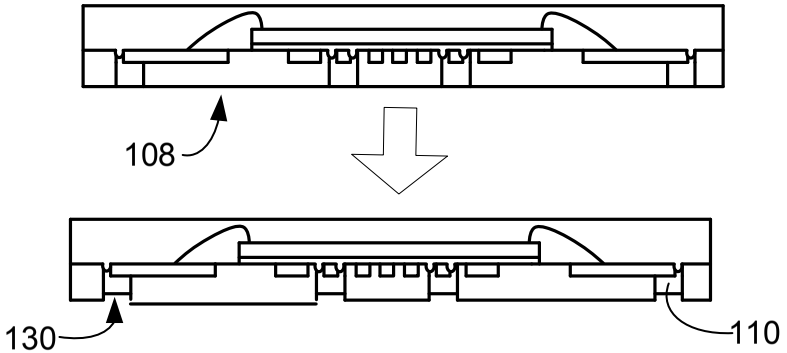


FIG. 13

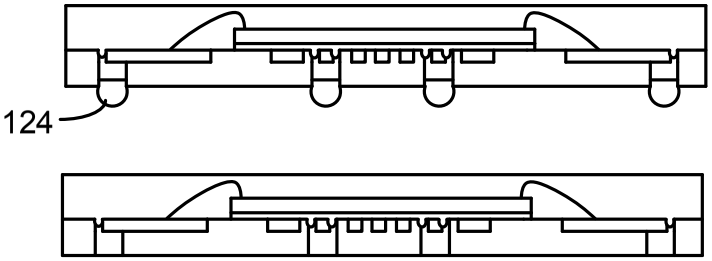


FIG. 14

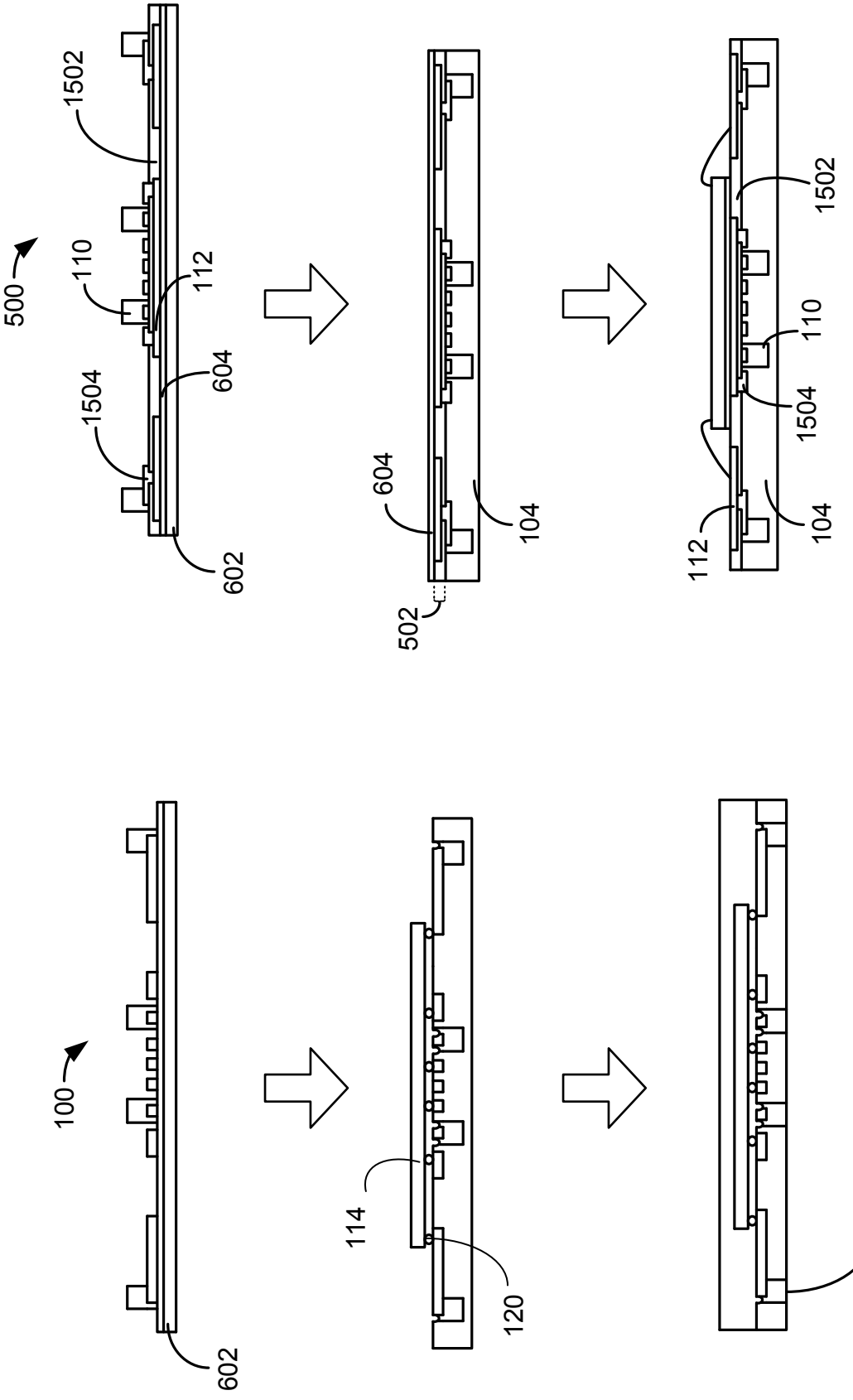


FIG. 15

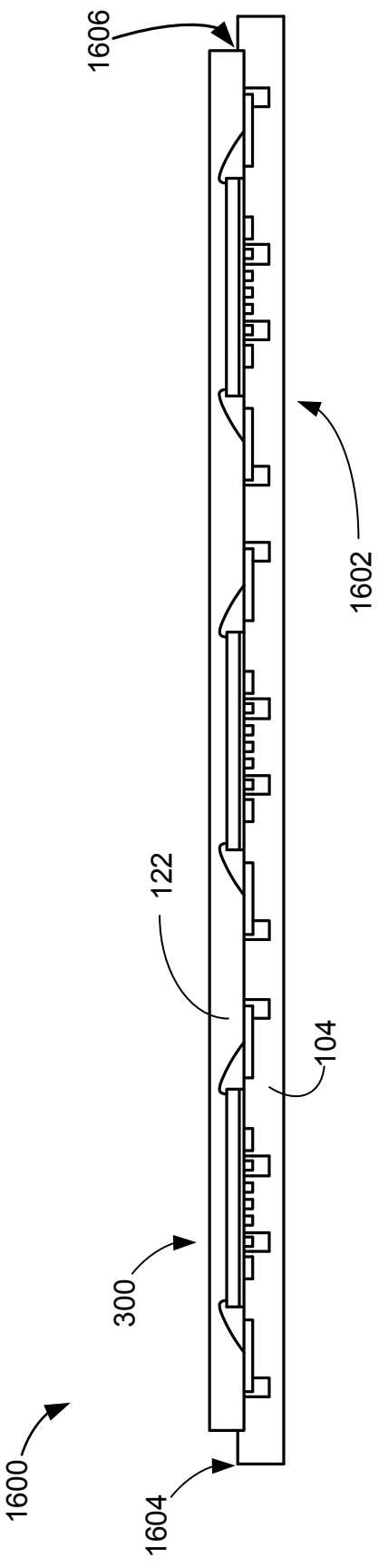

1606
1602
122
104
300
1600
1604

FIG. 16

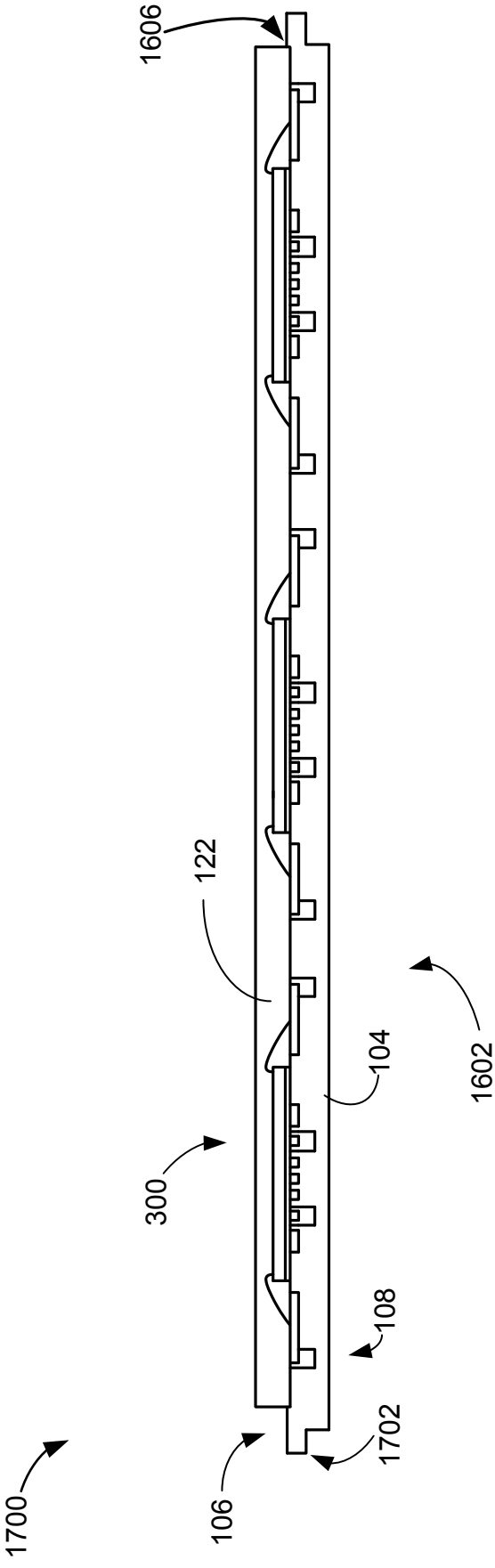

1606
122
104
1602
300
108
1700
1702
106

FIG. 17

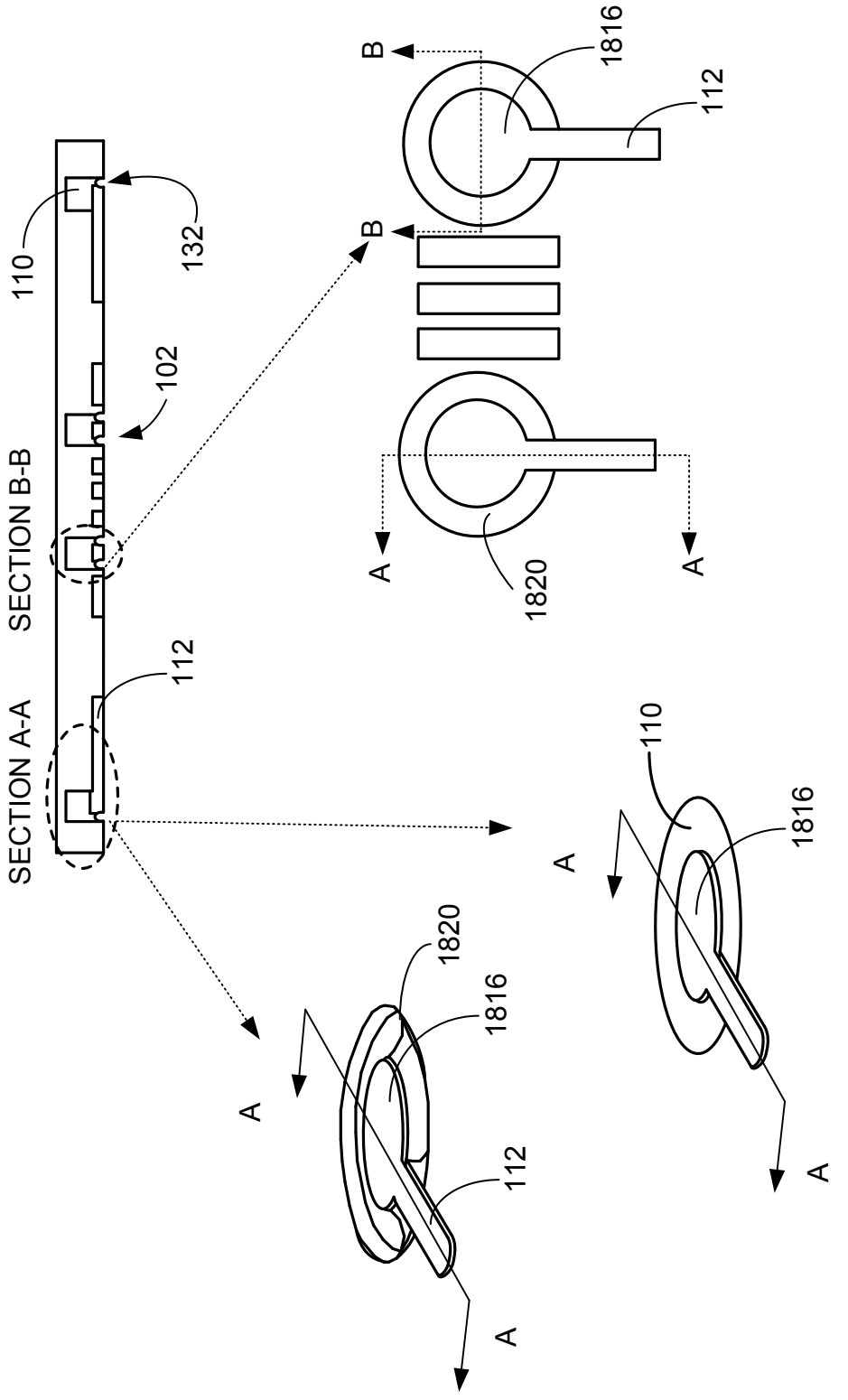

SECTION A-A
SECTION B-B
110
132
102
112
B
B
1816
112
A
A
1820
110
1816
A
A
1820
1816
112
A
A

FIG. 18

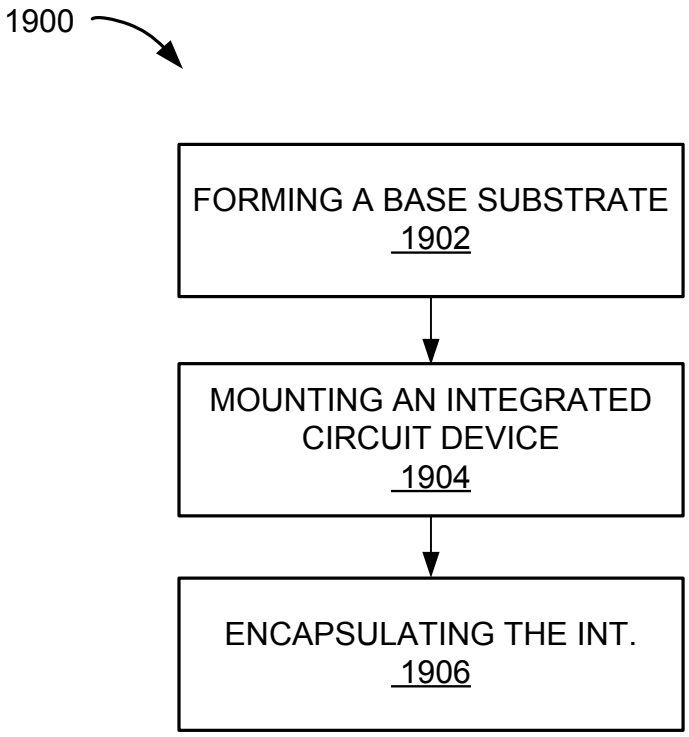

1900
FORMING A BASE SUBSTRATE
1902
MOUNTING AN INTEGRATED CIRCUIT DEVICE
1904
ENCAPSULATING THE INT.
1906

FIG. 19