

MEMORY DEVICE AND OPERATION METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to Korean Patent Application No. 10-2017-
5 0159995 filed on November 28, 2017, in the Korean Intellectual Property Office, and to
United States of America Patent Application No. 16/136,895 filed on September 20, 2018, in
the United States Patent and Trademark Office, the disclosure of which is incorporated by
reference herein in its entirety.

TECHNICAL FIELD

[0002] Embodiments of the inventive concept disclosed herein relate generally to a
semiconductor memory, and more particularly, to reducing data errors in a semiconductor
memory accessed through a serial data interface.

BACKGROUND

[0003] Semiconductor memory devices are classified into volatile memory devices,
which do not retain data stored therein at power-off, such as static random access memory
(SRAM), dynamic RAM (DRAM), synchronous DRAM (SDRAM), and the like, and
nonvolatile memory devices, which retain data stored therein even at power-off. Examples of
20 the latter type include read only memory (ROM), programmable ROM (PROM), electrically
programmable ROM (EPROM), electrically erasable and programmable ROM (EEPROM),
flash memory devices, phase-change RAM (PRAM), magnetic RAM (MRAM), resistive
RAM (RRAM), ferroelectric RAM (FRAM), and the like.

[0004] A DRAM device exchanges data with an external device (e.g., a host, a memory controller, or the like) through data lines (DQ). Since physical characteristics of the data lines may differ among data lines, signal characteristics of the data lines may vary. This may cause a reduction in reliability of the DRAM device.

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SUMMARY

[0005] Embodiments of the inventive concept provide a memory device that may have improved reliability and afford a reduction in bit errors when exchanging data with another device.

10 **[0006]** According to an exemplary embodiment, an operation method of a memory device configured to receive data from an external device through a plurality of data lines is provided. The method may involve generating a first internal code based on a first code and a second code, where the first code includes information of a first reference voltage associated with a first data line of the plurality of data lines and the second code includes information

15 about a decision feedback equalization (DFE) level associated with the first data line. A second internal code may be generated based on third and fourth codes, where the third code includes information of a second reference voltage associated with a second data line of the plurality of data lines and the fourth code includes information about a second decision

20 feedback equalization (DFE) level associated with the second data line. First and second reference voltage sets may be generated based on the first and second internal codes, respectively. First input data applied on the first data line may be sampled based on the first reference voltage set, and second input data applied on the second data line may be sampled based on the second reference voltage set.

[0007] According to an exemplary embodiment, a memory device includes a plurality of memory cells, and a data line driving circuit that generates a first reference voltage set based on a first code and a second code, determines first input data input through a first data line, based on the first reference voltage set, generates a second reference voltage set based on
5 a third code and a fourth code, and determines second input data input through a second data line, based on the second reference voltage set.

[0008] According to an exemplary embodiment, a memory system includes a plurality of memory devices, each including a memory cell array and a data line driver unit configured to drive the memory cell array and receive first input data via a respective first data line and
10 receive second input data via a respective second data line. Each data line driver unit may include a first data line driver circuit configured to generate a first reference voltage set based on a first code and a second code associated with the first data line, and to determine bit values of the first input data received through the first data line, based on the first reference voltage set. Each data line driver may further include a second data line driver circuit
15 configured to generate a second reference voltage set based on third and fourth codes associated with the second data line and to determine bit values of the second input data received through the second data line, based on the second reference voltage set.

BRIEF DESCRIPTION OF THE DRAWINGS

20 **[0009]** The above and other aspects and features of the inventive concept will become apparent by describing in detail exemplary embodiments thereof with reference to the accompanying drawings.

[0010] FIG. 1 is a block diagram illustrating a memory system according to an embodiment of the inventive concept.

[0011] FIG. 2 is a block diagram illustrating an example memory device of FIG. 1.

[0012] FIG. 3 is a flowchart illustrating an example operation of the memory system
5 of FIG. 1.

[0013] FIGS. 4A, 4B and 4C are each a graph for describing a reference voltage for each of a plurality of data lines.

[0014] FIG. 5 is a flowchart illustrating an example operation of the memory device of FIG. 2.

10 **[0015]** FIG. 6 is a block diagram illustrating an example DQ driving unit of FIG. 2.

[0016] FIG. 7 is a block diagram illustrating an example configuration for the first DQ driver of FIG. 6.

[0017] FIG. 8 is a view illustrating an example sampler of FIG. 7.

[0018] FIG. 9 is a block diagram illustrating another example of the first DQ driver of
15 FIG. 6.

[0019] FIG. 10 is a block diagram illustrating an example sampler of FIG. 9.

[0020] FIG. 11 is a block diagram for describing an example first DQ driver of FIG. 6.

[0021] FIG. 12 is a flowchart for describing an example operation of the memory device using the first DQ driver of FIG. 11.

20 **[0022]** FIG. 13 schematically illustrates a DQ driving unit according to an embodiment of the inventive concept.

[0023] FIG. 14 is a block diagram illustrating an example graphic system to which the memory device according to the inventive concept may be applied.

[0024] FIG. 15 is a block diagram illustrating an example memory module to which the memory device according to the inventive concept may be applied.

[0025] FIG. 16 is a block diagram illustrating an example computing system to which the memory device according to the inventive concept may be applied.

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DETAILED DESCRIPTION

[0026] Example embodiments of the inventive concept will now be described more fully with reference to the accompanying drawings, in which like reference numerals may refer to like elements. The inventive concept may, however, be embodied in many different
10 forms, and is not to be construed as limited to the example embodiments set forth herein.

[0027] An element which performs a specific function or includes a specific function, described herein with such terms as “block”, “unit”, “module”, “driver”, or the like, is implemented with hardware circuitry. The hardware may be dedicated hardware for the specific function or may be general purpose hardware that executes software instructions to
15 carry out the specific function.

[0028] In the description below, phrases such as “determine data”, “determine a data signal”, “recover a data signal” or the like refer to determining values of individual symbols (e.g. bit values “1” or “0”) of a data signal containing a stream of symbols. The symbols may be synchronized with a clock and the values they represent may be determined by periodically
20 sampling the data signal at the timing of the clock.

[0029] FIG. 1 is a block diagram illustrating a memory system 10 according to an embodiment of the inventive concept. Memory system 10 may include a host 11 and a memory device 100. To store data in the memory device 100 or to read data stored in the

memory device 100, the host 11 may transmit a clock signal CK, a command CMD, and an address ADDR to the memory device 100. The host 11 may exchange data with the memory device 100 through a plurality of data lines DQ1 to DQn. In an example embodiment, the host 11 may be a memory controller or a central processing unit (CPU).

5 **[0030]** In an example embodiment, the host 11 may communicate with the memory device 100 based on a double data rate (DDR) interface or other suitable interface. For example, the host 11 may communicate with the memory device 100 through at least one of various communication interfaces such as a universal serial bus (USB) interface, a multimedia card (MMC) interface, an embedded MMC (eMMC) interface, a peripheral component
10 interconnection (PCI) interface, a PCI-express (PCI-E) interface, an advanced technology attachment (ATA) interface, a serial-ATA interface, a parallel-ATA interface, a small computer small interface (SCSI), an enhanced small disk interface (ESDI), an integrated drive electronics (IDE) interface, a Firewire interface, a universal flash storage (UFS) interface, and a nonvolatile memory express (NVMe) interface.

15 **[0031]** Under control of the host 11, the memory device 100 may store data received through the plurality of data lines DQ1 to DQn or may transmit data stored therein to the host 11 through the plurality of data lines DQ1 to DQn. In an example embodiment, the memory device 100 may include a dynamic random access memory (DRAM). In other cases, the memory device 100 may include at least one of various memory devices such as a static
20 random access memory (SRAM), a synchronous DRAM (SDRAM), a read only memory (ROM), a programmable ROM (PROM), an electrically programmable ROM (EPROM), an electrically erasable and programmable ROM (EEPROM), a flash memory device, a phase-

change RAM (PRAM), a magnetic RAM (MRAM), a resistive RAM (RRAM), a ferroelectric RAM (FRAM), and the like.

[0032] In an example embodiment, the memory device 100 may include a data line driving unit 110 (hereinafter referred to as a “DQ driving unit”) that is configured to control the plurality of data lines DQ1 to DQn, individually. The DQ driving unit 110 may generate a reference voltage and/or a set of reference voltages (hereinafter referred to as a “reference voltage set”) for reading data provided through each of the plurality of data lines DQ1 to DQn. For example, the DQ driving unit 110 may determine whether a data signal provided through a first data line DQ1 is, at a particular sampling point, a “data 1” or “data 0” (bit value of 1 or bit value of 0), based on a comparison of the data signal voltage with the reference voltage at the sampling point. The data signal may change or maintain the previous bit value to provide binary information with every cycle of a clock, and the data signal may be sampled a short time after a rising and/or falling edge of the clock to determine a current bit value. When the data signal voltage is higher than the reference voltage, a “1” may be detected; and when the data signal voltage is below the reference voltage, a “0” may be detected. In other embodiments, the inventive concept may be utilized for detecting values of different types of symbols (non-binary symbols).

[0033] A set of reference voltages may be used to determine bit values of a data signal on any of the data lines DQ1 – DQn as follows: A set of reference voltages for a given data line DQi may be comprised of an “upper reference voltage” and a “lower reference voltage” concurrently provided. The upper reference voltage may be set slightly higher than a “main reference voltage” that has been established for that data line DQi. (Hereafter, the main reference voltage for a given data line may be referred to as just the “reference voltage” for

that data line.) The lower reference voltage may be set slightly lower than the main reference voltage. At any given sampling point to determine a bit value of the data signal, the signal voltage may be compared to either the upper reference voltage or the lower reference voltage. For any given sampling point, a selection of whether to use the upper reference voltage or the lower reference voltage may be made, where the selection may be based upon the bit value of the bit measured in the immediately previous clock cycle. In this manner, a filtering of the data stream is accomplished in which bit errors due to a phenomenon of Inter Symbol Interference (ISI) may be alleviated. As described below, the amount by which the upper reference voltage and the lower reference voltage each differ from the main reference voltage may be equal to a decision feedback equalization (DFE) level which has been established for that data line. A training process may be used to optimally set each of the main reference voltage and the DFE level for each data line.

[0034] In other cases, different types of noise reduction techniques and algorithms may use a set of adjusted reference voltages (e.g. upper and lower reference voltages)

determined in other ways. Two or more adjusted reference voltages may be concurrently provided in a set, where one of the adjusted voltages is selected for each symbol of a data signal. The selection may be decided every clock cycle, or every N clock cycles, depending on the type and implementation of the particular noise reduction / bit error reduction approach.

[0035] In some embodiments, a noise reduction technique may be dynamically

implemented. In the discussion below, phrases such as “using a reference voltage or reference voltage set” may refer to such dynamic implementation of the noise reduction scheme.

[0036] In an example embodiment, the reference voltage generated by the DQ driving unit 110 may be differently generated with respect to each of the plurality of data lines DQ1 to

DQn. For example, the DQ driving unit 110 may determine bit values of a data signal provided through the first data line DQ1 by using a first reference voltage or a first reference voltage set and may determine a data signal provided through the second data line DQ2 by using a second reference voltage different from the first reference voltage (or a second reference voltage set different from the first reference voltage set). That is, the DQ driving unit 110 may determine data signals of the plurality of data lines DQ1 to DQn, based on different reference voltages or different reference voltage sets.

[0037] In an example embodiment, information of a reference voltage associated with each of the plurality of data lines DQ1 to DQn may be stored in a separate storage circuit (e.g., a mode register) in the form of a code. As one example, the inventive concept may be applied to a serial data communication system compliant with the GDDR6 standard (JEDEC standard 250, i.e., GDDR standard, version 6), in which case the reference voltage may be stored in mode register MR6 and/or MR9, which are mode registers standardized for storing reference voltages and DFE voltages. (Various codes in mode register MR6 may each represent a reference voltage as a percentage of a supply voltage VDDQ. Various codes in mode register MR9 may each represent a DFE level as a percentage of the supply voltage VDDQ.) The DQ driving unit 110 may generate an internal code, based on the above-described code and may generate a reference voltage or a reference voltage set, based on the generated internal code. Codes associated with reference voltages of the plurality of data lines DQ1 to DQn may be determined in the training process for the memory device 100. Examples of training processes are also disclosed in the GDDR6 standard.

[0038] As described above, the memory device 100 according to the inventive concept may generate different reference voltages and/or different reference voltage sets with respect

to each of the plurality of data lines DQ1 to DQn and may determine data signals received through the plurality of data lines DQ1 to DQn, based on the generated reference voltages and/or reference voltage sets.

[0039] FIG. 2 is a block diagram illustrating an example of the memory device 100 of

5 FIG. 1. Referring to FIGS. 1 and 2, the memory device 100 may include a memory cell array 120, a row decoder 130, a column decoder 140, a sense amplifier/write driver 150, an input/output circuit 160, and a storage circuit 170.

[0040] The memory cell array 120 may include a plurality of memory cells. The memory cells may be connected with word lines WL and bit lines BL. Each of the memory
10 cells may be configured to store data by controlling the word lines WL and the bit lines BL. Each of the memory cells may be a DRAM cell that includes a storage capacitor and a “transmission transistor” (interface transistor).

[0041] The row decoder 130 may be connected with the memory cell array 120 through the word lines WL. The row decoder 130 may control voltages of the word lines WL
15 in response to an address ADDR and a command CMD. In an example embodiment, the address ADDR may be a row address, and the command CMD may be a row address strobe (RAS) signal.

[0042] The column decoder 140 may be connected with the memory cell array 120 through the bit lines BL. The column decoder 140 may receive the address ADDR and the
20 command CMD and may select at least one bit line of the bit lines BL in response to the received signals. In an example embodiment, the address ADDR may be a column address, and the command CMD may be a column address strobe (CAS) signal. The sense

amplifier/write driver 150 may sense or control a voltage of the bit line selected by the column decoder 140.

[0043] The input/output circuit 160 may be connected with the plurality of data lines DQ1 to DQn and may exchange data with an external device (e.g., the host 11) through the plurality of data lines DQ1 to DQn.

[0044] In an example embodiment, the input/output circuit 160 may include the DQ driving unit 110. As described with reference to FIG. 1, the DQ driving unit 110 may control voltages of the plurality of data lines DQ1 to DQn for the purpose of transmitting data to an external device (e.g., the host 11) through the plurality of data lines DQ1 to DQn. DQ driving unit 110 may also determine data signals received through the plurality of data lines DQ1 to DQn.

[0045] In an example embodiment, the DQ driving unit 110 may perform the above-described data determination operation on the plurality of data lines DQ1 to DQn, based on different reference voltages or different reference voltage sets. For example, the DQ driving unit 110 may receive a code “CODE” (hereafter, just “the CODE”) associated with each of the plurality of data lines DQ1 to DQn from the storage circuit 170. The DQ driving unit 110 may generate a different reference voltage set with respect to each of the plurality of data lines DQ1 to DQn, based on the CODE and may determine data signals received through the plurality of data lines DQ1 to DQn, based on the generated reference voltages sets.

[0046] In an example embodiment, the CODE may include information about a reference voltage and a decision feedback equalization (DFE) level of each of the plurality of data lines DQ1 to DQn, and the DQ driving unit 110 may generate an internal code, based on

the CODE associated with each of the plurality of data lines DQ1 to DQn. The internal code may be used for the DQ driving unit 110 to operate.

[0047] The storage circuit 170 may store various information needed for the memory device 100 to operate. In one example, storage circuit 170 may be embodied as one or more

5 mode registers (MR). The CODE, which is a part of the above-described various information, may be information stored within the above-discussed sixth mode register MR6 and/or ninth mode register MR9 in a memory device compliant with the GDDR6 standard. For example, the CODE may include information about a reference voltage or a decision feedback equalization (DFE) level of each of the plurality of data lines DQ1 to DQn. In an example
10 embodiment, the DFE level may be an offset voltage for adjusting a reference voltage to be used in a current data determination operation or for compensating a current data signal to be determined, based on a data bit previously determined.

[0048] In a GDDR6 compliant embodiment, storage circuit 170 may include mode registers MR6 and MR9, and seventh to eleventh opcodes stored in the sixth mode register

15 MR6 may respectively indicate the plurality of data lines DQ1 to DQn, and 0-th to sixth opcodes may respectively indicate levels of corresponding reference voltages. Further, seventh to eleventh opcodes of the ninth mode register MR9 of storage circuit 170 may respectively indicate the plurality of data lines DQ1 to DQn, and 0-th to third opcodes may respectively indicate corresponding DFE levels. The above-described information (i.e., the
20 information within the sixth and ninth mode registers MR6 and MR9) may be decided through a training operation of the memory device 100 and may be stored in the storage circuit 170 through a mode register set operation. In an example embodiment, the DQ driving unit 110

may generate the internal code, based on the above-described mode register values MR6 and MR9.

[0049] Other embodiments providing storage of the CODE may be intended for different types of memory devices (which may not be compliant with GDDR6). The CODE
5 may be alternatively stored in different mode registers, in a vendor-specific area of a mode register, or in a separate storage circuit.

[0050] As described above, the memory device 100 according to the inventive concept may generate different reference voltage sets with respect to each of the plurality of data lines DQ1 to DQn and may determine data signals of the plurality of data lines DQ1 to DQn, based
10 on the different reference voltage sets.

[0051] FIG. 3 is a flowchart illustrating an operation of the memory system 10 of FIG. 1. FIGS. 4A to 4C are graphs for describing a reference voltage for each of the plurality of data lines DQ1 to DQn. An initialization operation of the memory system 10 will be described with reference to FIG. 3. In an example embodiment, in a portion of the initialization
15 operation, a reference voltage and a DFE level for each of the plurality of data lines DQ1 to DQn may be decided. Graphs of FIGS. 4A to 4C show a data-eye of a signal received through each data line DQ. In the graphs of FIGS. 4A to 4C, the X-axis denotes time, and the Y-axis denotes a level of a reference voltage.

[0052] Referring to FIGS. 1 and 3, in operation S11, the memory system 10 may
20 perform an initialization operation. For example, when the memory system 10 is powered up, the host 11 and the memory device 100 may perform the initialization operation depending on a predefined manner. During the initialization operation, the host 11 may provide a power supply voltage to the memory device 100, may perform various initial setting operations, and

may read necessary information from the memory device 100 or may set necessary information.

[0053] In operation S12, the memory system 10 may perform a command address training operation. For example, the host 11 and the memory device 100 may perform the command address training operation for the purpose of improving a timing margin of the command CMD and the address ADDR. In an example embodiment, the command address training operation may be selectively performed or omitted.

[0054] In operation S13, the memory system 10 may perform a clock alignment training operation. For example, the memory device 100 may receive a clock signal CK from the host 11 and may generate a data clock signal WCK, based on the received clock signal CK. In an example embodiment, a frequency of the data clock signal WCK may be “N” times a frequency (N being a natural number) of the clock signal CK. In a GDDR6 compliant embodiment, the clock alignment training operation may be a WCK2CK alignment training (an alignment of WCK to CK). The clock signal CK may be used to process the command CMD and the address ADDR, and the data clock signal WCK may be used to process data. The memory device 100 may perform the WCK2CK alignment training operation such that transition edges of the clock signal CK and the data clock signal WCK are synchronously aligned.

[0055] Due to variation in physical characteristics of the data lines DQ1 to DQn, each of the data lines may optimally supply data at a different voltage level. For this reason, it may be desirable to individually set a reference voltage for data signal determination for each of the data lines. Read and write training may be performed to determine such an optimum reference voltage level for each of the data lines DQ1 to DQn. In operation S14, the memory

system 10 may perform a read training operation. For example, the host 11 may adjust settings values (e.g., reference voltage and/or a DFE value read from mode registers, etc.) of the memory device 100 such that the signal integrity or data-eye of data read from the memory device 100 is optimized. In an example embodiment, the read training operation may be
5 independently performed on each of the plurality of data lines DQ1 to DQn.

[0056] In operation S15, the memory system 10 may perform a write training operation. For example, the host 11 may transmit data to the memory device 100 and may adjust settings values (e.g., reference voltage and/or a DFE value read from mode registers, etc.) of the memory device 100 such that the signal integrity or data-eye of the transmitted
10 data is optimized. In an example embodiment, the write training operation may be independently performed on each of the plurality of data lines DQ1 to DQn. After the above-described initialization and training operation are performed in operation S11 to operation S15, in operation S16, the memory system 10 may perform a normal operation.

[0057] In an example embodiment, in operation S14 or S15, a reference voltage and
15 DFE level for each of the plurality of data lines DQ1 to DQn may be decided. For example, as illustrated in FIG. 4A, when a reference voltage of the first data line DQ1 is set to a first reference voltage VREFD1, the first data line DQ1 may have a first signal integrity SI1. The upper and lower levels of the data eye may represent an average logic “1” and “0” level, respectively, of the data signal on that data line. If these levels are too close, the bit error rate
20 may be unsuitably high. Therefore, a wider opening for the data eye is generally desirable. Varying the reference voltage VREF within a specified range may vary loading of the data line and produce different results for the data eyes. In the example of FIG., 4A, when the reference voltage of the first data line DQ1 is set to a second reference voltage VREFD2 or a

third reference voltage VREFD3, the first data line DQ1 may have a second signal integrity SI2 smaller than the first signal integrity SI1 or a third signal integrity SI3 smaller than the first signal integrity SI1.

[0058] The signal integrity SI may indicate the size, a vertical height, or a width of a

5 data-eye of a signal received through a data line DQ. That is, as the signal integrity SI becomes greater, data may be identified more accurately, with a lower bit error rate. In the illustrated example, when the reference voltage of the first data line DQ1 is set to the first reference voltage VREFD1, the first data line DQ1 may have optimal signal integrity.

[0059] Referring to FIG. 4B, when a reference voltage for the first to third data lines

10 DQ1 to DQ3 is set to the first reference voltage VREFD1, the first to third data lines DQ1 to DQ3 may have first to third signal integrities SI1 to SI3, respectively. The reason is that physical characteristics of the first to third data lines DQ1 to DQ3 are different from each other. In other words, even though reference voltages of data lines are the same, the data lines may have different signal integrities due to locations or physical characteristics of the data

15 lines. That is, when the reference voltage for the first to third data lines DQ1 to DQ3 is set to the first reference voltage VREFD1, the first data line DQ1 may have the optimal signal integrity, but the second and third data lines DQ2 and DQ3 may not have optimal signal integrities. For instance, the variation in characteristics may cause logic voltage levels to fluctuate between data lines, causing an increase in bit errors when sampling input data to

20 determine bit values. Such bit errors may be particularly apparent in a DRAM device accessed by a high speed serial data bus (e.g. > 1 GHz) that operates with relatively low logic voltages to conserve power.

[0060] Referring to FIG. 4C, a reference voltage of the first data line DQ1 may be set to the first reference voltage VREFD1, a reference voltage of the second data line DQ2 may be set to the second reference voltage VREFD2, and a reference voltage of the third data line DQ3 may be set to the third reference voltage VREFD3. In this case, each of the first to third data lines DQ1 to DQ3 may have an optimal signal integrity. In other words, each data line may have an optimal signal integrity by setting reference voltages of the first to third data lines DQ1 to DQ3 differently.

[0061] The above-described reference voltage of each data line may be decided through operation S14 or operation S15 (i.e., a read training operation or a write training operation), and information about the reference voltage of each data line may be stored in the storage circuit 170 as a portion of the CODE.

[0062] Although not illustrated in FIGS. 3 to 4C, in operation S14 or operation S15 (i.e., a read training operation or a write training operation), a DFE level may also be decided in a similar manner, and information about the DFE level may be stored in the storage circuit 170 as another portion of the CODE.

[0063] FIG. 5 is a flowchart illustrating an operation of the memory device 100 of FIG. 2. Referring to FIGS. 2 and 5, in operation S110, the memory device 100 may perform a training operation to decide a reference voltage VREFD and a DFE level for each data line DQ. For example, as in the description given with reference to FIGS. 3 to 4C, the memory device 100 may decide the reference voltage VREFD and the DFE level for each data line DQ. The determined information may be stored in the storage circuit 170 as the CODE.

[0064] In operation S120, the memory device 100 may generate a reference voltage set including an upper reference voltage VREFD_p and a lower reference voltage VREFD_n,

based on the reference voltage VREFD and the DFE level. In an example embodiment, a level of the upper reference voltage VREFD_p may be a level corresponding to a sum (VREFD + DFE) of the reference voltage VREFD and the DFE level, and a level of the lower reference voltage VREFD_n may be a level corresponding to a difference (VREFD - DFE) of the reference voltage VREFD and the DFE level.

[0065] In operation S130, the memory device 100 may sample data DIN input through each data line DQ, based on a reference voltage set including the upper reference voltage VREFD_p and the lower reference voltage VREFD_n. For example, the memory device 100 may determine any given data bit of a bit stream signal input through each data line DQ, based on a selected one of the upper reference voltage VREFD_p or the lower reference voltage VREFD_n.

[0066] FIG. 6 is a block diagram illustrating an example of the DQ driving unit 110 of FIG. 2. Below, for brevity, a DQ driving unit 110 is described as a receiver determining input data DIN. DQ driving unit 110 may also include a transmitter controlling each data line DQ, for the purpose of transmitting data to an external device (e.g., the host 11); and the transmission operations may be analogous to the receive operations discussed below.

[0067] Referring to FIGS. 2 and 6, the DQ driving unit 110 may include a plurality of data line drivers 111-1 to 111-n (hereinafter referred to as “DQ drivers”). The plurality of DQ drivers 111-1 to 111-n may respectively receive input data DIN1 to DINn through the plurality of data lines DQ1 to DQn. For example, the first DQ driver 111-1 may receive the first input data DIN1 through the first data line DQ1, and the second DQ driver 111-2 may receive the second input data DIN2 through the second data line DQ2. Likewise, the third to

n-th DQ drivers 111-3 to 111-n may respectively receive third to n-th input data DIN3 to DINn through the third to n-th data lines DQ3 to DQn.

[0068] The plurality of DQ drivers 111-1 to 111-n may respectively receive a plurality of codes CODE1 to CODEn from the storage circuit 170 and may respectively generate

5 reference voltage sets based on the received codes CODE1 to CODEn. For example, the first DQ driver 111-1 may receive the first code CODE1 from the storage circuit 170 and may generate a reference voltage set based on the received first code CODE1. The second DQ driver 112 may receive the second code CODE2 from the storage circuit 170 and may generate a reference voltage set based on the received second code CODE2. Likewise, the
10 third to n-th DQ drivers 111-3 to 111-n may respectively receive the third to n-th codes CODE3 to CODEn from the storage circuit 170 and may respectively generate reference voltage sets based on the received third to n-th codes CODE3 to CODEn.

[0069] In this case, the reference voltage sets generated in the first to n-th DQ drivers 111-1 to 111-n may be different from each other. Alternatively, a reference voltage set

15 generated in at least one of the first to n-th DQ drivers 111-1 to 111-n may be different from reference voltage sets generated in the remaining DQ drivers.

[0070] The plurality of DQ drivers 111-1 to 111-n may respectively sample the plurality of input data DIN1 to DINn input through the plurality of data lines DQ1 to DQn,

based on generated reference voltages and may identify first to n-th data D1 to Dn as the
20 sampling result. For example, the first DQ driver 111-1 may sample the first input data DIN1, based on the generated reference voltage and may output the first data D1 as the sampling result. The second DQ driver 111-2 may sample the second input data DIN2, based on the generated reference voltage and may output the second data D2 as the sampling result.

Likewise, the third to n-th DQ drivers 111-3 to 111-n may respectively sample the third to n-th input data DIN3 to DINn, based on the generated reference voltages and may respectively output the third to n-th data D3 to Dn as the sampling result.

[0071] As described above, the DQ driving unit 110 may sample the input data DIN by using different reference voltages, with respect to the plurality of data lines DQ1 to DQn. Accordingly, since the optimal signal integrity for each of the plurality of data lines DQ1 to DQn is obtainable, the integrity of the input data DIN is improved and a bit error rate may be reduced.

[0072] FIG. 7 is a block diagram illustrating an example configuration for the first DQ driver 111-1 of FIG. 6. Note that the same configuration may be used for any of the other DQ drivers 111-2 to 111-n.

[0073] The first DQ driver 111-1 may include a reference voltage generator 1111 and a sampler 1112. The reference voltage generator 1111 may generate a first upper reference voltage VREFD1_p and a first lower reference voltage VREFD1_n. For example, the reference voltage generator 1111 may include a resistor ladder 1111a, an adder 111b, a first decoding unit 1111c, an upper reference voltage selector 1111d, a subtractor 1111e, a second decoding unit 1111f, and a lower reference voltage selector 1111g.

[0074] The resistor ladder 1111a may include a plurality of resistors connected in series or in parallel. The resistor ladder 1111a may divide a power supply voltage VDDQ applied thereto to generate various voltages. Resistor ladder 1111a may concurrently provide the first upper reference voltage VREFD1_p and the first lower reference voltage VREFD1_n to the upper reference voltage selector 1111d and the lower reference voltage selector 1111g, respectively.

[0075] The adder 1111b may be configured to receive the first code CODE1 and to add a first reference voltage VREFD1 and a first DFE level included in the received first code CODE1. For example, as described above, the first code CODE1 may be decided in a read training or write training operation, and may include a first bit sequence representing the first reference voltage VREFD1 and a second bit sequence representing the first DFE level associated with the first data line DQ1. The adder 1111b may add the first reference voltage VREFD1 and the first DFE level (i.e., $VREFD1 + DFE1$) and may output the addition result in the form of a digital code.

[0076] The first decoding unit 1111c may decode the addition result from the adder 1111b. The upper reference voltage selector 1111d may output one of a plurality of voltages from the resistor ladder 1111a as the first upper reference voltage VREFD1_p, based on the decoding result of the first decoding unit 1111c.

[0077] The subtractor 1111e may be configured to receive the first code CODE1 and to perform a subtraction operation on the first reference voltage VREFD1 and the first DFE level included in the received first code CODE1. For example, as described above, the first code CODE1 may be decided in a read training or write training operation, and may include bit sequences representing the first reference voltage VREFD1 and the first DFE level, respectively, associated with the first data line DQ1. The subtractor 1111e may subtract the first DFE level from the first reference voltage VREFD1 (i.e., $VREFD1 - DFE1$) and may output the subtraction result in the form of a digital code.

[0078] The second decoding unit 1111f may decode the subtraction result from the subtractor 1111e. The lower reference voltage selector 1111f may output one of the plurality

of voltages from the resistor ladder 1111a as the first lower reference voltage VREFD1_n, based on the decoding result of the second decoding unit 1111f.

[0079] As described above, the reference voltage generator 1111 may generate the first upper reference voltage VREFD1_p and the first lower reference voltage VREFD1_n,

5 based on the first code CODE1. Here, the first upper reference voltage VREFD1_p may be a sum (i.e., $VREFD1 + DFE1$) of the first reference voltage VREFD1 and the first DFE level, and the first lower reference voltage VREFD1_n may be a difference (i.e., $VREFD1 - DFE1$) of the first reference voltage VREFD1 and the first DFE level.

[0080] The sampler 1112 may sample the first input data DIN1 (a bit stream) received

10 through the first data line DQ1, based on the first upper reference voltage VREFD1_p (for some of the bits in the bit stream) and the first lower reference voltage VREFD1_n (for other bits of the bit stream) and may output the first data D1 as the sampling result. In particular, a feedback path FP may be provided from the output of sampler 1112 back to an internal circuit selection circuit of sampler 1112. In accordance with a DFE scheme for reducing Inter

15 Symbol Interference, when the previous bit value of the first data D1 was determined to be a “1”, the internal selection circuit causes sampler 1112 to sample the current bit of the first input data DIN1 by comparing the current bit’s voltage level with the upper reference voltage VREF_p. When the previous bit value of the first data D1 was determined to be a “0”, the internal selection circuit causes sampler 1112 to sample the current bit of the first input data

20 DIN1 by comparing the current bit’s voltage level with the lower reference voltage VREF_n.

This technique may effectively amount to a filtering mechanism by which bit errors are reduced. FIG. 8 schematically illustrates an example sampler 1112, which may include a comparator 1112b and a multiplexer 1112a. The comparator 1112b may compare one of the

first upper reference voltage VREFD1_p and the first lower reference voltage VREFD1_n with the first input data DIN1 and may output the first data D1 as the sampling result.

[0081] In detail, in the first input data DIN1, it is assumed that bit “1” is a signal corresponding to a high level and bit “0” is a signal corresponding to a low level. The

5 comparator 1112b may output bit “1” as the first data D1 when a voltage of a signal of the first data line DQ1 is higher than one of the first upper reference voltage VREFD1_p and the first lower reference voltage VREFD1_n and may output bit “0” as the first data D1 when the voltage of the signal of the first data line DQ1 is lower than one of the first upper reference voltage VREFD1_p and the first lower reference voltage VREFD1_n

10 **[0082]** The multiplexer 1112a may select one of the first upper reference voltage VREFD1_p and the first lower reference voltage VREFD1_n depending on a selection signal SEL and may provide the selected reference voltage to the comparator 1112b. In an example embodiment, the selection signal SEL may be provided from the feedback path FP or a buffer circuit (not shown) coupled to the feedback path FP. That is, the selection signal SEL may be

15 based on a previous output signal of the comparator 1112b. For example, when bit “1” is output as the first data D1, the first upper reference voltage VREFD1_p may be selected to determine a next data bit; when bit “0” is output as the first data D1, the first lower reference voltage VREFD1_n may be selected to determine a next data bit. For this reason, even though a signal corresponding to the first input data DIN1 received through the first data line DQ1

20 does not fully swing (due to inter symbol interference), data may be determined with a satisfactorily low bit error rate because one of the first upper reference voltage VREFD1_p and the first lower reference voltage VREFD1_n is selected based on a previously determined bit value. More specifically, if the previous data bit was a “1”, ISI tends to increase the

voltage of the current data bit, whereby an increase in the reference voltage to VREF1_p leads to less bit errors. Conversely, if the previous data bit was a “0”, ISI tends to reduce the voltage of the current data bit, so that a decrease in the reference voltage to VREF1_n may reduce the occurrence of bit errors.

5 **[0083]** As described above, a DQ driver according to the inventive concept may generate an upper reference voltage and a lower reference voltage for each of a plurality of data lines individually, based on a reference voltage and a DFE level decided through a read or write training operation and may determine input data received through the respective data line, based on the generated upper and lower reference voltages for that data line, thereby
10 improving the integrity of data. In addition, the concurrent provision of both the upper and lower voltages VREFD1_p and VREFD1_n based on the CODE1 may allow for a faster response to the output data D1 in the feedback path FP, and therefore, a reduced bit error rate, as compared to conventional approaches that generate a single DFE-adjusted reference voltage from a resistor ladder based on the output data D1.

15 **[0084]** In an example embodiment, upper reference voltages generated in the plurality of DQ drivers 111-1 to 111-n may be different from each other, and lower reference voltages generated in the plurality of DQ drivers 111-1 to 111-n may be different from each other. That is, the integrity of data may be secured with respect to each of the plurality of data lines DQ1 to DQn, by differently setting reference voltages (i.e., upper and lower reference voltages, or a
20 reference voltage and a DFE level) for the plurality of data lines DQ1 to DQn.

[0085] FIG. 9 is a block diagram illustrating another example of the first DQ driver 111-1 of FIG. 6. The shown configuration may likewise be used for any one of the other DQ drivers 111-2 to 111-n. FIG. 10 is a block diagram illustrating an example sampler 1113' of

FIG. 9. Referring to FIGS. 9 and 10, the first DQ driver 111'-1 may include a reference voltage generator 1111', a DFE level generator 1112', and a sampler 1113'. The reference voltage generator 1111' may receive the first code CODE1 and may generate a first reference voltage VREFD1, based on the received first code CODE1. The DFE level generator 1112' may receive the first code CODE1 and may generate a first DFE positive level DFE1_p and a first DFE negative level DEF1_n, based on the received first code CODE1. In an example embodiment, the first DFE positive level DFE1_p may be a positive value, and the first DFE negative level DEF1_n may be a negative value. It is noted here that the first DFE positive level DFE1_p and a first DFE negative level DEF1_n may together constitute another example of a reference voltage set.

[0086] The sampler 1113' may sample the first input data DIN1 received through the first data line DQ1, based on the first reference voltage VREFD1, the first DFE positive level DFE1_p, and the first DFE negative level DEF1_n and may output the first data D1 as the sampling result. For example, as illustrated in FIG. 10, the sampler 1113' may include a first sub-sampler 1113a', a second sub-sampler 1113b', and a multiplexer 1113c'.

[0087] The first sub-sampler 1113a' may sample the first input data DIN1 received through the first data line DQ1, based on the first reference voltage VREFD1 the first DFE positive level DFE1_p. The second sub-sampler 1113b' may sample the first input data DIN1 received through the first data line DQ1, based on the first reference voltage VREFD1 the first DFE negative level DEF1_n.

[0088] The multiplexer 1113c' may select one of outputs of the first and second sub-samplers 1113a' and 1113b' depending on the selection signal SEL and may output the selected output as the first data D1. In an example embodiment, the selection signal SEL may

be decided according to a value or level of the first data D1. As in the above description, when the first data D1 currently determined is bit “1” (i.e., in a high level), in a next bit determination operation, the selection signal SEL may be decided such that the output of the first sub-sampler 1113a’ is selected. In contrast, when the first data D1 currently determined is bit “0” (i.e., in a low level), in a next bit determination operation, the selection signal SEL may be decided such that the output of the second sub-sampler 1113b’ is selected.

[0089] As described above, a plurality of DQ drivers may generate different reference voltages with respect to a plurality of data lines and may sample input data, based on the generated reference voltages. Accordingly, optimal integrity of data for each of the plurality of data lines DQ1 to DQn may be obtained.

[0090] FIG. 11 is a block diagram illustrating an example DQ driver, 111’’. DQ driver 111’’ is explained below as an example of the first DQ driver 111-1 of FIG. 6, but the configuration may be used for any of the DQ drivers 111-1 to 111-n.

[0091] DQ driver 111’’ may include a code generator 1113’’, a reference voltage generator 1111’’, and a sampler 1112’’. The code generator 1113’’ may receive a relevant code (i.e., the first code CODE1) from the storage circuit 170 and may generate a first internal code CD1_int based on the received first code CODE1. For example, the first code CODE1 may include a first sub-code CD1 indicating reference voltage information for the first data line DQ1 and a second sub-code CD2 indicating a DFE level for the first data line DQ1. The code generator 1113’’ may combine the first and second sub-codes CD1 and CD2 included in the first code CODE1 to generate the first internal code CD1_int.

[0092] The first internal code CD1_int may include an addition code obtained by adding the first sub-code CD1 and the second sub-code CD2 and a subtraction code obtained

by subtracting the second sub-code CD2 from the first sub-code CD1. In an example embodiment, the first sub-code CD1 may be a code stored in mode register MR6 (defined in the GDDR6 standard), and the second sub-code CD2 may be a code stored in mode register MR9. In this case, a portion of the first internal code CD1_int may represent a voltage

5 addition of voltages represented in mode registers MR6 and MR9, and another portion of the first internal code CD1 may represent a subtraction of voltage represented by the code in mode register MR9 from that in MR6.

[0093] The reference voltage generator 1111” may generate a first reference voltage set (VREF1_p, VREF1_n), based on the first internal code CD1_int. The sampler 1112” may
10 determine the first input data DIN1 received through the first data line DQ1, based on the first reference voltage set (VREF1_p, VREF1_n).

[0094] FIG. 12 is a flowchart for describing an operation of the memory device 100 using the first DQ driver 111” of FIG. 11. Referring to FIGS. 11 and 12, in operation S210, the memory device 100 may perform a training operation to decide the first and second sub-
15 codes CD1 and CD2 for each data line DQ. For example, as described above, the memory device 100 may generate the first sub-code CD1 indicating information about a reference voltage of each data line DQ and the second sub-code CD2 indicating information about a DFE level, through a read or write training operation. In an example embodiment, as
described above, the first sub-codes CD1 of data lines DQ may be different from each other,
20 and the second sub-codes CD2 of the data lines DQ may be different from each other.

[0095] In operation S210, the memory device 100 may generate an internal code CD_int, based on the first and second sub-codes CD1 and CD2 for each data line DQ. For

example, the memory device 100 may differently generate the internal code CD_int for each data line DQ, based on the first and second sub-codes CD1 and CD2 for each data line DQ.

[0096] In operation S230, the memory device 100 may determine data received through each data line DQ, based on the internal code CD_int. For example, as described

5 above, the memory device 100 may generate a reference voltage set for each data line DQ, based on the internal code CD_int and may determine data received through each data line, based on the generated reference voltage set.

[0097] As described above, a memory device according to an embodiment of the inventive concept may generate an internal code for each data line DQ, based on a different

10 code and may determine data, based on the generated internal code.

[0098] FIG. 13 is a block diagram illustrating an example DQ driving unit 210 according to an embodiment of the inventive concept. In this example, DQ driving unit 210 may include first to sixteenth DQ drivers DRV1 to DRV16. Each of the first to sixteenth DQ drivers DRV1 to DRV16 may include components described with reference to FIGS. 7 to 10.

15 For instance, DQ1 driver 111-1 may be an example of DQ driver DRV1; DQ2 driver 111-2 may be an example of DQ driver DRV2; etc. As described above, the first to sixteenth DQ drivers DRV1 to DRV16 may be respectively connected with a plurality of data lines (e.g., DQ1 to DQ16) and may be configured to control the plurality of data lines (e.g., DQ1 to DQ16).

20 **[0099]** The first to sixteenth DQ drivers DRV1 to DRV16 may respectively receive the first to sixteenth codes CODE1 to CODE16 from a storage circuit 270. Each of the first to sixteenth DQ drivers DRV1 to DRV16 may generate a reference voltage, a DFE level, an upper reference voltage, and/or a lower reference voltage, based on the received code. In this

case, the generated voltages may have different levels depending on characteristics of data lines. For example, each of the first to sixteenth DQ drivers DRV1 to DRV16 may include a reference voltage generator and a code generator. In each of the first to sixteenth DQ drivers DRV1 to DRV16, the code generator may receive the corresponding code and may generate
5 an internal code based on the received code. In each of the first to sixteenth DQ drivers DRV1 to DRV16, the reference voltage generator may generate a reference voltage set based on the generated internal code. For example, the “VREFD Generator” of the first DQ driver DRV1 may generate a first reference voltage set while the “VRFED Generator” of the thirteenth driver DRV13 may generate a thirteenth reference voltage set that differs from the first
10 reference voltage set.

[00100] Alternatively, the first to sixteenth DQ drivers DRV1 to DRV16 may be grouped, where each group receives a common code from storage circuit 270, and each DQ driver within the same group may generate the same reference voltages based on the common code. For example, the first and second DQ drivers DRV1 and DRV2 may constitute a first
15 group G11. The third and fourth DQ drivers DRV3 and DRV4 may constitute a second group G12. Likewise, the remaining DQ drivers may be grouped in units of two. In this case, a plurality of codes CODE_G11 to CODE_G18 may be respectively provided to a plurality of groups G11 to G18.

[00101] Alternatively, the first to fourth DQ drivers DRV1 to DRV4 may constitute a
20 first group G21. Likewise, the remaining DQ drivers may be grouped in units of four. In this case, a plurality of codes CODE_G21 to CODE_G24 may be respectively provided to a plurality of groups G21 to G24. Each DQ driver belonging to the same group may generate a

reference voltage, a DFE level, an upper reference voltage, and/or a lower reference voltage by using the same code.

[00102] In other words, the plurality of DQ drivers DRV1 to DRV16 may be grouped in units of 2^N or 2^{N+1} (N being a natural number), and each DQ driver belonging to the same group may generate a reference voltage, a DFE level, an upper reference voltage, or a lower reference voltage by using the same code.

[00103] Although the first to sixteenth DQ drivers DRV1 to DRV16 are illustrated in FIG. 13, the number of DQ drivers may vary with the number of data lines connected with a host. Also, DQ drivers may be grouped in other ways. For instance, DQ drivers that are physically adjacent may belong to the same group. In other words, DQ drivers may be grouped based on an adjacency criterion.

[00104] In the above-described embodiments of FIGS. 1-13, data receiving operations of a DQ driving unit for writing input data to memory device 100 have been described. For transmitting data read from memory device 100 to an external device such as host 11, a plurality of DQ drivers of a DQ driving unit may respectively control a plurality of data lines. In this case, the plurality of DQ drivers may respectively control the plurality of data lines by using different DFE levels.

[00105] FIG. 14 is a block diagram illustrating a graphic system, 1000, to which a memory device according to the inventive concept may be applied. Graphic system 1000 may include a graphic processor 1100 and a plurality of DRAM devices 1210-1 to 1210-i. The graphic processor 1100 may be configured to perform various operations for processing image information. The graphic processor 1100 may be connected with the plurality of DRAM devices 1210-1 to 1210-i through a plurality of channels CH1 to CHi. In an example

embodiment, each of the plurality of channels CH1 to CHi may be a communication channel that is based on a graphic double data rate (GDDR) interface such as a GDDR6 compliant interface.

[00106] Each of the plurality of DRAM devices 1210-1 to 1210-i may include the
5 memory device 100 described with reference to FIGS. 1 to 13. That is, each of the plurality of DRAM devices 1210-1 to 1210-i may include a memory cell array 120 and may determine data based on different reference voltages, with respect to a plurality of data lines.

[00107] FIG. 15 is a block diagram illustrating a memory module, 2000, to which a memory device according to the inventive concept may be applied. Memory module 2000
10 may be a memory system that may include a register clock driver (RCD) 2100, a plurality of DRAM devices 2210 to 2290, and a plurality of data buffers DB.

[00108] The RCD 2100 may receive a command/address CA and a clock signal CK from an external device (e.g., a host or a memory controller). Based on the received signals, the RCD 2100 may send the command/address CA to the plurality of DRAM devices 2210 to
15 2290 and may control the plurality of data buffers DB.

[00109] The plurality of DRAM devices 2210 to 2290 may be respectively connected with the plurality of data buffers DB through memory data lines MDQ. In an example embodiment, the plurality of DRAM devices 2210 to 2290 may each include a memory cell array 120 and a DQ driving unit 110 described with reference to FIGS. 1 to 11. That is, each
20 of the plurality of DRAM devices 2210 to 2290 may determine or transmit data based on different reference voltages, with respect to relevant memory data lines MDQ.

[00110] The plurality of data buffers DB may transmit and receive data to and from an external device (e.g., a host or a memory controller) through a plurality of data lines DQ.

[00111] In an example embodiment, the memory module 2000 illustrated in FIG. 15 may have the form factor of a load reduced dual in-line memory module (LRDIMM). In other embodiments, the memory module 2000 illustrated in FIG. 15 may have the form factor of a registered DIMM (RDIMM) in which the plurality of data buffers DB are not included.

5 **[00112]** FIG. 16 is a block diagram illustrating a computing system 3000 to which a memory device according to the inventive concept is applied. Computing system 3000 may include one of a computer, a portable computer, a ultra-mobile personal computer (UMPC), a workstation, a server computer, a net-book, a personal digital assistant (PDA), a portable
10 computer, a web tablet, a wireless phone, a mobile phone, a smartphone, a digital camera, a digital audio recorder, a digital audio player, a digital picture recorder, a digital picture player, a digital video recorder, a digital video player, a device capable of transmitting or receiving information in a wireless environment, a wearable device, or various electronic devices including a home network.

[00113] The computing system 3000 may include a processor 3100, a memory module
15 3200, a chipset 3300, a graphic processing unit (GPU) (or a graphic module) 3400, an input/output device 3500, and a storage device 3600. The processor 3100 may perform overall operations of the computing system 3000. The processor 3100 may perform various operations in the computing system 3000.

[00114] The memory module 3200 may be directly connected with the processor 3100.
20 For example, the memory module 3200 may have a form of a dual in-line memory module (DIMM), and the memory module 3200 may be installed in a DIMM socket directly connected with the processor 3100 and may communicate with the processor 3100. In an example embodiment, the memory module 3200 may include any of the memory devices

described with reference to FIGS. 1 to 14. That is, the memory module 3200 may individually control a plurality of data lines DQ, based on different reference voltages and/or different reference voltage sets.

[00115] The chipset 3300 may be electrically connected to the processor 3100 and may control hardware of the computing system 3000 under control of the processor 3100. For example, the chipset 3300 may be connected with each of the GPU 3400, the input/output device 3500, and the storage device 3600 through main buses, and may perform a bridge operation with respect to the main buses.

[00116] The GPU 3400 may perform a series of arithmetic operations for outputting image data of the computing system 3000. In an example embodiment, the GPU 3400 may be embedded in the processor 3100 in the form of a system-on-chip. In an example embodiment, the GPU 3400 may include any of the memory devices described with reference to FIGS. 1 to 14. That is, a memory device included in the GPU 3400 may control a plurality of data lines DQ, based on different reference voltages and/or different reference voltage sets.

[00117] The input/output device 3500 may include various devices that make it possible to input data or an instruction to the computing system 3000 or to output data to an external device. The storage device 3600 may be used as a mass storage medium of the computing system 3000. The storage device 3600 may include mass storage media such as a hard disk drive (HDD), a solid state drive (SSD), a memory card, and a memory stick.

[00118] As described above, a memory device according to the inventive concept may exchange data with an external device (e.g., a host or a memory controller) through a plurality of data lines. In this case, the memory device may individually control a plurality of data lines

DQ, based on different reference voltages. Accordingly, since an optimal data integrity for each data line is secured, a memory device having improved reliability is provided.

[00119] According to the inventive concept, a memory device may individually control a plurality of data lines, based on different reference voltages. Accordingly, since an optimal

5 data integrity or data-eye for each data line is secured, a memory device having improved reliability and an operation method thereof are provided. The memory device may individually control a plurality of data lines DQ based on different reference voltage sets, where each set contains a plurality of concurrently provided voltages, and where the value of each symbol of an input data stream may be determined based on a selected one of the
10 plurality of voltages. When using one of the plurality of voltages in conjunction with a noise / error reduction scheme such as DFE, a fast response time may be achievable, which may result in a bit error rate reduction.

[00120] As mentioned earlier, an element which performs a specific function or includes a specific function, described herein with such terms as “block”, “unit”, “module”,

15 “driver”, or the like, is implemented with hardware circuitry. Any such element may be alternatively called a “circuit”, “circuitry” or the like. For instance, a driver, a data line driving unit, a generator, a sampler, a selector, a decoder, an adder, or a subtractor, as described above, may be alternatively referred to interchangeably as a driver circuit, a data line driving circuit, a generator circuit, a sampler circuit, a selector circuit, a decoder circuit, an adder
20 circuit, and a subtractor circuit, respectively.

[00121] While the inventive concept has been described with reference to exemplary embodiments thereof, it will be apparent to those of ordinary skill in the art that various

changes and modifications may be made thereto without departing from the spirit and scope of the inventive concept as set forth in the following claims.

WHAT IS CLAIMED IS:

1. An operation method of a memory device which is configured to receive data from an external device through a plurality of data lines, the method comprising:

5 generating a first internal code based on a first code and a second code, wherein the first code includes information of a first reference voltage associated with a first data line of the plurality of data lines and the second code includes information about a first decision feedback equalization (DFE) level associated with the first data line;

10 generating a second internal code based on a third code and a fourth code, wherein the third code includes information of a second reference voltage associated with a second data line of the plurality of data lines and the fourth code includes information about a second decision feedback equalization (DFE) level associated with the second data line;

generating a first reference voltage set and a second reference voltage set based on the first internal code and the second internal code, respectively; and

15 sampling first input data applied on the first data line based on the first reference voltage set and second input data applied on the second data line based on the second reference voltage set.

2. The operation method of claim 1, wherein:

20 the first reference voltage set comprises a first upper reference level voltage equaling a sum of the first reference voltage and the first DFE level, and a first lower reference voltage equaling the first reference voltage minus the first DFE level; and

25 the second reference voltage set comprises a second upper reference level voltage equaling a sum of the second reference voltage and the second DFE level, and a second lower reference voltage equaling the second reference voltage minus the second DFE level.

3. The operation method of claim 2, wherein the sampling of the first input data comprises:

30 concurrently applying the first upper reference voltage and the first lower reference voltage as inputs to a multiplexer;

applying a selection signal to the multiplexer to select the first upper reference voltage or the first lower reference voltage;

outputting the selected one of the first upper reference voltage and the first lower reference voltage to one input of a comparator; and

5 receiving the first input data at a second input of the comparator, and outputting a comparison result at a sampling point, indicative of a bit value of the first input data at the sampling point.

10 4. The operation method of any one of claims 1 to 3, wherein the first internal code and the first reference voltage set are generated by a first data line driver circuit associated with the first data line, based on the first and second codes obtained by the first data line driver circuit, and the method further comprising:

15 grouping at least one further data line driver circuit, associated with at least one further data line, with the first data line driver circuit and obtaining, by the at least one further data line driver circuit, the first and second codes;

20 wherein the at least one further driver circuit generates the same first reference voltage set as that generated by first data line driver circuit, based on the first and second internal codes, and determines bit values of further data by sampling the further data using the same first reference voltage set.

5. The operation method of claim 4, wherein the first and further driver circuits are grouped based on a criterion of physical adjacency therebetween.

25 6. The operation method of any one of claims 1 to 5, wherein levels of the first and second reference voltages are different from each other, and the first and second DFE levels are different from each other.

30 7. The operation method of any one of claims 1 to 6, wherein the first to fourth codes are stored in at least one mode register of the memory device.

8. The operation method of claim 7, wherein each of the first to fourth codes is stored in the at least one mode register in a training operation of the memory device.

5 9. The operation method of any one of claims 1 to 8, wherein the memory device communicates with an external device, based on a graphic double data rate (GDDR) interface.

10. A memory system comprising:
a plurality of memory devices, each comprising:
a memory cell array; and
10 a data line driver unit configured to drive the memory cell array and receive first input data via a respective first data line and receive second input data via a respective second data line;
wherein each data line driver unit comprises:
a first data line driver circuit configured to generate a first reference voltage set based
15 on a first code and a second code associated with the first data line, and to determine bit values of the first input data received through the first data line, based on the first reference voltage set; and
a second data line driver circuit configured to generate a second reference voltage set
20 based on a third and a fourth code associated with the second data line and to determine bit values of the second input data received through the second data line, based on the second reference voltage set.

11. The memory system of claim 10, wherein for each memory device, the first code includes information of a first reference voltage level associated with the first data line,
25 the second code includes information of a first decision feedback equalization (DFE) level associated with the first data line, the third code includes information of a second reference voltage level associated with the second data line, and the fourth code includes information of a second DFE level associated with the second data line.

12. The memory system of claim 11, wherein the first and second reference voltage levels are different from each other, and the first and second DFE levels are different from each other.

5 13. The memory system of claim 11 or claim 12, further comprising:
at least one mode register configured to store the first to fourth codes.

10 14. The memory system of claim 13, wherein, for each memory device, the first to fourth codes are stored in the at least one mode register in a training operation of the memory device.

15 15. The memory system of claim 13 or claim 14, wherein the first reference voltage generator includes:

an adder circuit that adds the first code and the second code to generate a first sub-
15 code for the first upper reference voltage;

a first decoder circuit configured to decode the first sub-code;

an upper reference voltage selector circuit configured to output the first upper
reference voltage, based on the decoding result of the first decoder circuit;

20 a subtractor circuit that performs a subtraction operation on the first code and the second code to generate a second sub-code for the first lower reference voltage;

a second decoder circuit configured to decode the second sub-code; and

a lower reference voltage selector circuit configured to output the first lower reference
voltage, based on the decoding result of the second decoder.

25 16. The memory system of claim 15, wherein each data line driver unit further comprises a resistive ladder coupled to each of the upper reference voltage selector circuit and the lower reference voltage selector circuit, wherein the resistive ladder concurrently provides the upper and lower reference voltages.

30 17. The memory system of any one of claims 10 to 16, wherein each data line driver unit further comprises at least one third data line driver circuit, associated with at least

one third data line that receives third input data, and which is grouped with the first data line driver circuit for receiving the same first and second codes,

wherein the at least one third data line driver circuit outputs the same first reference voltage set as the first data line driver circuit, and determines bit values of the third input data
5 by sampling the third input data using the voltages of the same first reference voltage set.

18. The memory system of any one of claims 10 to 17, wherein:
each memory device is a dynamic random access memory (DRAM) device; and
the memory system further comprising a register clock driver (RCD) configured to
10 send a command/address signal received from an external device to each DRAM device.

19. The memory system of claim 10, wherein:
the first code includes information of a first reference voltage level associated with
the first data line;
15 the second code includes information of a first decision feedback equalization (DFE)
level associated with the first data line;
the first data line driver circuit comprises a reference voltage generator that generates
a first reference voltage, a DFE generator circuit, and a sampler circuit, wherein the DFE
generator circuit outputs a first DFE positive level and a first DFE negative level based on the
20 information of the DFE level, and the first reference voltage set comprises the first reference
voltage, the first DFE positive level and the first DFE negative level; and
the sampler circuit samples the first input data to determine bit values thereof based
on a comparison with a sum of either the first reference voltage with the DFE positive level or
the first reference voltage with the first DFE negative level.

20. The memory system of claim 19, wherein each data line driver unit further comprises
first and second sub-sampler circuits, each receiving the first input data, the first sub-sampler
circuit configured to sample the first input data based on the sum of the first reference voltage
with the DFE positive level, and the second sub-sampler circuit configured to sample the first
30 input data based on the sum of the first reference voltage with the DFE negative level.