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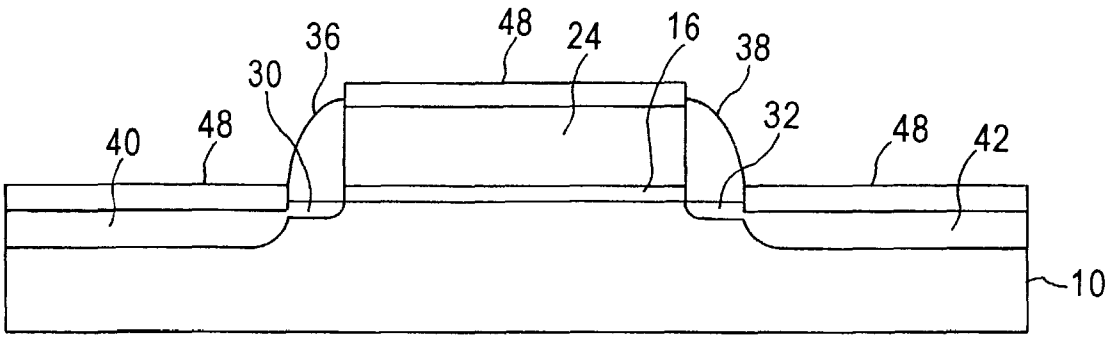
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(54) Title: LOW-TEMPERATURE POST-DOPANT ACTIVATION PROCESS



(57) Abstract: A method of manufacturing a MOSFET semiconductor device comprises forming a gate electrode (24) over a substrate (10) and a gate oxide (16) between the gate electrode (24) and the substrate (10); forming source/drain extensions (30, 32) in the substrate (10); forming first and second sidewall spacers (36, 38); implanting dopants (44) within the substrate (10) to form source/drain regions (40, 42) in the substrate (10) adjacent to the sidewalls spacers (36, 38); laser thermal annealing to activate the source/drain regions (40, 42); depositing a layer of nickel (46) over the source/drain regions (40, 42); and annealing to form a nickel silicide layer (46) disposed on the source/drain regions (40, 42). The source/drain extensions (30, 32) and sidewall spacers (36, 38) are adjacent to the gate electrode (24). The source/drain extensions (30, 32) can have a depth of about 5 to 30 nanometers, and the source/drain regions (40, 42) can have a depth of about 40 to 100 nanometers. The annealing is at temperatures from about 350 to 500 °C.

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