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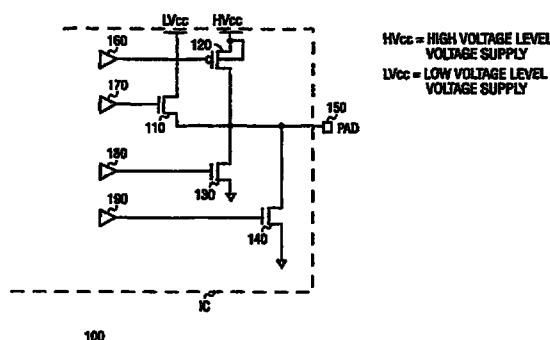
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(54) Title: OUTPUT BUFFER FOR HIGH AND LOW VOLTAGE BUS



(57) Abstract: Briefly, in accordance with one embodiment of the invention, an integrated circuit includes: an output buffer. The output buffer includes semiconductor devices coupled to provide alternately activateable circuit configurations. The output buffer is adapted to couple to separate voltage supply voltage level ports and is further adapted to switch between the alternately activateable circuit configurations. The respective alternately activateable circuit configurations are respectively specifically adapted for inter-operating with other integrated circuit chips, the respective threshold voltage levels of the semiconductor devices of different other integrated circuit chips being different. Briefly, in accordance with another embodiment of the invention, an output buffer includes: a plurality of thick gate metal-oxide semiconductor (MOS) transistors coupled in a circuit configuration. The plurality includes, as pull-up transistors, at least a thick gate P-channel MOS (PMOS) transistor and a thick gate N-channel MOS (NMOS) transistor, both respectively being coupled between separate voltage supply voltage level ports and an output port of the output buffer. The plurality further includes, as pull-down transistors, at least two more thick gate NMOS transistors, both respectively being coupled between ground and the output port. At least one of the pull-up transistors and one of the pull-down transistors is coupled in the circuit configuration to be driven on hard and to deliver a high voltage swing. Furthermore, at least one of the pull-up transistors and one of the pull-down transistors is coupled in the circuit configuration to be driven on less hard and to deliver a reduced voltage swing.

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