What is claimed is:

1. A method of forming a memory cell, comprising:

providing a lower line stack extending in a first direction, the lower line stack comprising a sacrificial line over a lower conductive line; and

forming a chalcogenide line extending in the first direction by selectively removing sacrificial material of the sacrificial line and replacing the removed sacrificial material with a stack of materials including a chalcogenide material and another material.

2. The method of claim **1**, wherein providing the lower line stack comprises subtractively patterning the lower line stack, subtractively patterning the lower line stack comprising:

providing a lower stack including a lower conductive material and the sacrificial material over the lower conductive material; and

etching the lower sacrificial material and the lower conductive material to form the lower line stack.

3. The method of claim **2**, further comprising:

subtractively patterning an upper line stack over the lower line stack and extending in a second direction crossing the first direction, subtractively patterning the upper line stack comprising:

providing an upper stack comprising an upper conductive material over the lower line stack; and

etching the upper conductive material to form the upper line stack comprising an upper conductive line.

4. The method of claim **3**, wherein at least one of the lower conductive line and the upper conductive line is subtractively patterned using a pitch-multiplication process.

5. The method of claim **3**, wherein subtractively patterning the upper line stack further comprises etching the chalcogenide line to form a chalcogenide element electrically isolated in both first and second directions.

6. The method of claim **5**, wherein subtractively patterning the lower line stack further includes providing and etching a lower chalcogenide material between the lower conductive material and the sacrificial material to form a lower chalcogenide line over the lower conductive line.

7. The method of claim **6**, wherein the lower chalcogenide line serves as a selector element of the memory device.

8. The method of claim **6**, wherein subtractively patterning the lower line stack further includes providing and etching a lower electrode material between the lower conductive material and the lower chalcogenide material to form a lower electrode line on the lower conductive line.

9. The method of claim **6**, wherein subtractively patterning the lower line stack further includes providing and etching a middle electrode material between the lower chalcogenide material and the sacrificial material to form a middle electrode line on the lower chalcogenide line.

10. The method of claim **9**, wherein subtractively patterning the lower line stack further includes forming spaces adjacent the lower line stack, and filling the spaces with a dielectric material.

11. The method of claim **10**, wherein subtractively patterning the upper line stack further comprises etching the middle electrode line to form a middle electrode electrically isolated in both first and second directions.

12. The method of claim **10**, wherein forming the chalcogenide line includes selectively removing the sacrificial material to form a gap between two adjacent spaces filled with the dielectric material, filling the gap with the chalcogenide material, and planarizing to form a surface comprising alternating chalcogenide lines and dielectric-filled spaces.

13. The method of claim **12**, wherein forming the chalcogenide line further includes selectively removing a portion of the chalcogenide material to form a second gap between two adjacent spaces filled with the dielectric material, filling the second gap with a third electrode material, and planarizing to form a surface comprising alternating third electrode lines and dielectric-filled spaces.

14. The method of claim **5**, wherein the chalcogenide element serves as a memory element of the memory device.

15. The method of claim **3**, wherein subtractively patterning the upper line stack further comprises providing and etching an upper chalcogenide material between the upper conductive line and the chalcogenide line to form an upper chalcogenide line extending in the second direction.

16. The method of claim **15**, wherein the upper chalcogenide line serves as the storage node of the memory device.

17. The method of claim **15**, wherein the lower chalcogenide line serves as the selector node of the memory device.

18. The method of claim **15**, wherein subtractively patterning the lower line stack comprises providing and etching a lower electrode layer between the lower conductive material and the sacrificial material to form a lower electrode line on the lower conductive line.

19. The method of claim **18**, wherein forming the chalcogenide line further includes selectively removing a portion of the chalcogenide material to form a second gap between two spaces filled with a dielectric, filling the second gap with a middle electrode material, and planarizing to form a surface comprising alternating middle electrode lines and chalcogenide lines.

20. The method of claim **19**, wherein subtractively patterning the upper line stack further comprises etching the middle electrode line to form a middle electrode electrically isolated in both first and second directions.

21. The method of claim **1**, wherein providing the sacrificial material includes providing at least one of graphitic carbon, polyimide, ALD silicon oxide, aluminum nitride, and silicon.

22. The method of claim **1**, wherein providing the sacrificial material includes providing graphitic carbon and a material chosen from a group consisting polyimide, ALD silicon oxide, aluminum nitride, and silicon.

23. The method of claim **1**, wherein the chalcogenide material comprises indium.

24. The method of claim **1**, wherein the lower conductive line comprises tungsten.

25. A method of forming a memory cell, comprising:

providing a lower line stack extending in a first direction, the lower line stack comprising a chalcogenide line over a lower conductive line;

providing an upper line stack over the lower line stack and extending in a second direction crossing the first direction, the upper line stack comprising a sacrificial line over the lower line stack; and

forming an upper conductive line extending in the second direction by selectively removing sacrificial material of the sacrificial line and replacing the removed sacrificial material with an upper conductive material.

26. The method of claim **25**, wherein providing the lower line stack comprises subtractively patterning the lower line stack, subtractively patterning comprising:

providing a lower stack including a lower conductive material and a chalcogenide material over the lower conductive material; and

etching the lower conductive material and the chalcogenide material to form the lower line stack.

27. The method of claim **26**, wherein providing the upper line stack comprises subtractively patterning the upper line stack, subtractively patterning comprising:

providing an upper stack including the sacrificial material over the chalcogenide line; and

etching the upper stack to form the upper line stack.

28. The method of claim **27**, wherein subtractively patterning the upper line further includes providing the sacrificial material over an upper chalcogenide material and etching the sacrificial material to form the upper line stack comprising a sacrificial line over a second chalcogenide line.

29. The method of claim **26**, wherein subtractively patterning the lower line stack further includes:

providing and etching an upper chalcogenide material over the chalcogenide material; and

etching to form an upper chalcogenide line over the chalcogenide line and extending in the first direction.

30. The method of claim **29**, wherein subtractively patterning the upper line stack further includes etching the upper chalcogenide line to form an upper chalcogenide element electrically isolated in both first and second directions.

31. The method of claim **30**, wherein subtractively patterning the lower line stack further includes providing and etching a middle electrode material interposed between the chalcogenide material and the upper chalcogenide material to form a middle electrode line on the chalcogenide line and extending in the first direction.

32. The method of claim **31**, wherein subtractively patterning the upper line stack includes etching the middle electrode line to form a middle electrode electrically isolated in both first and second directions.

33. The method of claim **25**, wherein the sacrificial material includes at least one of graphitic carbon, polyimide, ALD silicon oxide, aluminum nitride, and silicon.

34. The method of claim **25**, wherein the sacrificial material includes graphitic carbon and a material chosen from a group consisting polyimide, ALD silicon oxide, aluminum nitride, and silicon.

35. A method of forming a memory cell, comprising:

providing a lower line stack extending in a first direction, the lower line stack comprising a first sacrificial line over a lower conductive line;

forming a chalcogenide line extending in the first direction by selectively removing first sacrificial material of the first sacrificial line and replacing the removed first sacrificial material with a chalcogenide material;

providing an upper line stack extending in a second direction different from the first direction, the upper line stack comprising a second sacrificial line; and

forming an upper conductive line extending in the second direction by selectively removing second sacrificial material of the second sacrificial line and replacing the removed second sacrificial material with an upper conductive material.

36. The method of claim **35**, wherein providing the lower line stack comprises subtractively patterning the lower line stack, subtractively patterning comprising:

providing a lower stack including a lower conductive material and the first sacrificial material over the lower conductive material; and

etching the lower conductive material and the first sacrificial material to form the lower line stack.

37. The method of claim **35**, wherein providing the upper line stack comprises subtractively patterning the upper line stack, subtractively patterning comprising:

providing an upper stack including the second sacrificial material over the chalcogenide line; and

etching the second sacrificial material to form the upper line stack.

38. A method of forming a cross-point memory cell, comprising:

providing a lower line stack extending in a first direction, the lower line stack comprising a first sacrificial line over a first conductive line;

forming a lower chalcogenide line extending in the first direction by selectively removing first sacrificial material of the first sacrificial line and replacing the removed first sacrificial material with a lower chalcogenide material;

providing an upper line stack extending in a second direction different from the first direction, the upper line stack comprising a second sacrificial line over an upper chalcogenide line; and

forming an upper conductive line extending in the second direction by selectively removing second sacrificial material of the second sacrificial line and replacing the removed second sacrificial material with an upper conductive material.

39. The method of claim **38**, wherein providing the lower line stack comprises subtractively patterning the lower line stack, subtractively patterning comprising:

providing a lower stack including a first conductive material and a first sacrificial material over the lower conductive material; and

etching the first conductive material and the first sacrificial material to form the lower line stack.

40. The method of claim **38**, wherein providing the upper line stack comprises subtractively patterning the upper line stack, subtractively patterning comprising:

providing an upper stack including a second sacrificial material over an upper chalcogenide material; and

etching the second sacrificial material to form the upper line stack.

41. The method of claim **40**, wherein subtractively patterning the upper line stack further comprises etching the middle electrode line to form a middle electrode electrically isolated in both first and second directions.

42. The method of claim **38**, wherein forming the lower chalcogenide line further includes selectively removing a portion of the lower chalcogenide material to form a gap between two spaces adjacent to the first sacrificial line filled with a dielectric, filling the gap with a middle electrode material, and planarizing to form a surface comprising alternating middle electrode lines and chalcogenide lines.

43. A method of forming a memory cell, comprising:

providing a material stack including a conductive material and a sacrificial material over the conductive material;

etching the sacrificial material and the conductive material to form a stack of lines, each stack separated by spaces and comprising a line of sacrificial material over a line of conductive material;

filling the spaces with a dielectric material;

selectively removing the sacrificial material to form a gap interposed between the adjacent spaces filled with the dielectric material; and

forming a chalcogenide line by sequentially filling the gap with a chalcogenide material followed by another material.

44. The method of claim **43**, wherein the chalcogenide material comprises a phase change material, and the chalcogenide line forms a storage element of the memory cell.

45. The method of claim **43**, wherein the chalcogenide material comprises an Ovonic threshold material and the chalcogenide line forms a selector element of the memory cell.

46. A method of forming a memory cell, comprising:

providing a first plurality of stacks of lines of material extending in a first direction, each of the stacks of the first plurality comprising a chalcogenide line over a first conductive line;

providing a sacrificial material over the first plurality of stacks;

etching the sacrificial material to form a plurality of lines of sacrificial material separated by spaces and extending in a second direction crossing the first direction;

filling the spaces between the lines of sacrificial material with a dielectric material;

selectively removing the lines of sacrificial material to form gaps interposed between the dielectric material; and

forming a second conductive line by filling the gap with a conductive material.